# PIOC-101

Ver 0.5

Ampere

# HISTORY

| Ver. | Date | Description | Prepared by |
|---|---|---|---|
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| | | | |

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# ◆ 1 OVERVIEW

The PIOC-101 is a device incorporating 32-bit digital input/output ports which operates under the MWSC-101, and two timers/counters which can be variously programmed. It is designed to control remote digital input/output with relatively slow response speed and counting of high-speed input pulse sequences. It includes the UART equipped with an exclusive 9-bit asynchronous communication function which is capable of polling through high-speed binary communication of up to 125 kbps.

When mixing with the PPMC-112, etc. on the identical circuit of the MWSC-101, a total of 16 devices can be connected.

In addition to the binary communication mode, the PIOC-101 also supports communication by the ASCII codes and can be controlled through a personal computer's communication port.

## ● 1-1 Digital Input/Output Function

The digital input/output function is composed of four ports which can freely program input/output by 8 bits. At output, it outputs a strobe signal corresponding to each port.

## ● 1-2 Timer/Counter Function

There are two built-in timers/counters. One of them is a 24-bit counter which can receives and counts 2-phase pulse input such as a rotary encoder converted into a direction signal and pulse sequence, and use it for detecting the position of a servo motor, etc. Used together with a pulse generator such as the PPMC-112, it is designed to provide feedback control. This timer/counter is also available for counting pulse input or measuring the time.

The other timer/counter, 24-bit long as well, has a simple timer or counter function.

# ● *1-3 Outline of Instruction System*

The following outlines the instruction system of the PIOC-101. It consists of six types of instructions; initialize, start, output, input, extend, and status read.

## ■ 1-3.1 Initialize Instruction

The initialize instruction assign input/output to four 8-bit ports of the PIOC-101 and specifies the operating mode of the timer/counter A.

## ■ 1-3.2 Start Instruction and Input/Output Instruction

The start instruction starts the timer/counter and initiates sampling of the input/output data. The input instruction reads the input port and he current value of the timer/counter A, and the output instruction sets the preset value(and current value) of the timer/counter A and outputs the data to the output port.

## ■ 1-3.3 Extend Instruction

The extend instruction includes five kinds of instructions such as stopping the timer/counter, setting the operating mode and preset value of the timer/counter B, reading the communication error counter.

## ■ 1-3.4 Polling

If the input status of the input port changes corresponding to polling from the host(status read instruction) or if the timer/counter reaches the preset value, the data is returned. If the status of the input port does not change, the Busy or Ready frame is returned to reduce the traffic.
If the status of the input port changes, the data for that port is returned, and its flag is returned at the time of reaching the preset value of the timer/counter.
After initialization, the host sends the output instruction and extend instruction for setting the data required for the timer/counter. Then, the PIOC is activated by issuing the start instruction. Thereafter, the host always issue this poll instruction to wait for the PIOC to change the status, except in case of the data output instruction to the output port.

# ◆ 2 OPERATING MODES FOR BUILT-IN DEVICES

This section describes functioning and controls of two timers/counters and four 8-bit input/output ports.

## ● 2-1 Timer/Counter A

The timer/counter A is 24-bit long and has three operating modes; counter mode, timer mode, and encoder mode. The counter performs counting at a rise of the pulse input signal CPIA. The current value of the timer/counter A can be always read by the Input signal from the host.

### ■ 2-1.1 Counter Mode

This mode is to count input pulse sequences from the CPIA input pin. If the start instruction has been given to the counter and the count value reaches the preset value, the count-up signal ENDA/ is output. The counter is reset and reports count-up to polling from the host.
Thereafter, the counter keeps operating to count input pulses again from zero. If the preset value is reached again, ENDA/ is output, setting the end status again. The ENDA/ signal is reset by the first input pulse after resetting the counter.
If the preset value is zero, the counter keeps counting until it reaches the maximum value, 16,777,216.

### ■ 2-1.2 Timer Mode

In this mode, if the start instruction has been given to the timer and the preset time passes after inputting the start signal STA, the time-up signal ENDA/ is output. The timer is reset and reports time-up to polling from the host. The ENDA/ signal is held until the next STA signal is input.
In the timer mode, clocking is not performed until the start signal is newly given, but the preset value is held. Then, if STA is input, ENDA/ is reset to start clocking, and END/ is output after a lapse of the specified time.
The timer performs clocking in increments of 8 μseconds, allowing to set up to 134 seconds at longest.
If the preset value is zero, the timer keeps clocking until it reaches the maximum value, 134,218 seconds.

### ■ 2-1.3 Encoder Mode

This mode performs counting up or down, depending on the input pulse sequence from the CPIA input pin, and the direction input signal DIR and direction change pulse signal CDIR. It can also set an initial value and preset value with the output instruction. If the start instruction is given to the counter and th counter reaches the preset value, the ENDA/ signal is output and count-up is reported to polling from the host, but the counter is not reset. Although the preset value is overridden, but it is possible to continue monitoring of the current position.
This mode requires an external circuit which separates regular encoder output, 2-phase pulses, into a pulse sequence and direction signal and direction change pulse signal.
An error results if the difference between the preset value and current value is smaller than 100 at the time of start.

## ● 2-2 Timer/Counter B

Unlike the timer/counter A, the timer/counter B cannot read the current value.
In the counter mode, it counts input CPIBs, outputs ENDB/ upon reaching the preset value, and then, stops until the Start signal is received again. In the timer mode, it outputs ENDB/ at intervals given by the preset value.
If the preset value is zero, it is assumed that the maximum value, 16,777.216 has been given.

## ● 2-3 Input/Output Ports

There are four 8-bit input/output ports P0 to P3. Each port can be programmed for either input or output. If the ports are programmed for output, the strobe signals STR0/ to STR3/ are assigned to them to indicate that output has been settled.
The input status of the strobe signals are checked so that the ports cannot be set to output, which have been hardware-wise programmed for input by erroneous initial setting. If the port has the strobe signal set to "L", it is judged the input port. If the port has the strobe signal set to "H" because of a pull-up resistor, etc., it can be programmed for either input or output.
If the port is programmed for input, an incorporated noise eliminating function reads the it every 100µs and settles the data when it is consistent for two times running. The strobe signal RST/ is also provided, which represents a reading timing.

# ◆ 3 INSTRUCTION STRUCTURE

The instructions to the PIOC-101 are given through a serial communication circuit and the return values to them are also returned through the communication circuit. Communication is made through a circuit where multiple devices have been connected in a multidrop manner. Each PIOC has a 4-bit address unique to that circuit and the instructions are prefixed with a code including this address. The communication data is suffixed with a checksum code to avoid a communication error. In short, the instruction generally consist of a control code, instruction code, instruction data, and checksum.

## ● 3-1 Communication Protocol

The PIOC-101 has employed an 8-bit ASCII or 9-bit binary communication system. The physical layer of communication consists of circuits such as RS-485, connected in a multidrop manner. Logical control of communication is a half-duplex polling system and always activated from the master side.

The 9-bit binary mode supports the communication rates, 125 kbps, 62.5 kbps, and 31.25 kbps, and the 8-bit ASCII mode 83.33 kbps, 41.67 kbps, and 19.2 kbps, respectively. Those communication modes and baud rates are set by the PIOC-101 communication mode setting input signals MOD0 to MOD2.

## ● 3-2 Frame Structure

The communication frame consists of three parts. The first byte is a control code including an address, followed by a variable-length data portion, and 1-byte checksum at the end. A special frame having no data portion is used for the frame like Busy Check(polling frame) which requires high speed.

The control code has a special internal structure to realize multidrop communication at high speed. In the 9-bit binary mode, the Bit-8 is set to "1" in the control code and "0" in the data portion and checksum code. In the 8-bit ASCII mode, the Bit-7 is "1" in the control code and "0" in the data portion and checksum code. This structure allows the PIOC-101 to easily detect the head of the frame.

# ● *3-3 Frame Structure for 9-bit Binary Mode*

This communication mode is the protocol depending on the PIOC-101's special hardware. For this reason, the generally used 8-bit UART cannot be utilized. We provide the system controller MWSC-101 to realize this high-speed communication protocol. This device incorporates a physical layer to process this special protocol, and Layers-1 and -2. Communication can be made much faster than when the general ASCII code is used, by transmitting/receiving the binary data as it is.

## ■ 3-3.1 Control Code Structure

Only the control code has the Bit-8 set to "1", being structured as shown in the table below. This protocol takes into account a possibility of supporting other devices. The Bits-7 and -6 are set to "01" when selecting the PIOC-101. The Bits-5 and -4 represent a frame type. The frame type varies from the master side to the slave side. The Bits-3 to -0 specify a slave address.

| Bit | Value | Meaning | |
|---|---|---|---|
| | | Master sending frame | Slave reply frame |
| 7, 6 | 01 | Device selection bit (01 for PIOC-101) | |
| 5, 4 Frame type | 00 | Polling frame | No-status-change(operating) reply |
| | 01 | Instruction data frame | Acknowledge reply(stopping) |
| | 10 | Undefined | Reply with data |
| | 11 | Undefined | Reply with special data |
| 3,2,1,0 | | Device address (Select with DEVADR3 to DEVADR0) | |

## ■ 3-3.2 Data Portion Structure

The data portion has variable length and consists of an instruction code, followed by the data accompanying the instruction. Some frames have no data accompanying the instruction or no data portion.

## ■ 3-3.3 Checksum Calculation

Checksum is created by reversing all the bits after 8-bit binary addition of the control code through the end of the data portion.

## ■ 3-3.4 Control Protocol

For both master and slave frames, the Bits-5 and -4 of the control code represent the frame type. The following describes the communication procedure.

## ■ 3-3.5 Transmission Frame Activated by Master

There are two types of frames sent from the master side; they are a polling frame and an instruction data frame which gives the instructions to the PIOC-101.

**Polling frame:** This frame does not have the data portion and consists of only two bytes; the control code and checksum. Since the multidrop communication system does not allow the slave side to transmit the data without knowing the status of the transmission line, the master side always needs polling to monitor the status of the PIOC.

**Instruction data frame:** This frame includes the instruction code and data to the PIOC-101 in the data portion.

### Frames Returned by Slave

The PIOC-101(slave) returns four types of frames.

**Reply to Polling Frame:** When the timer/counter terminates, a special data frame is returned. If there is a change to the input data of the slave having input ports, the slave returns the special data frame to the polling frame. If there is no change to the status of the PIOC-101, it will return a no-status-change frame.

**Reply to Input Instruction:** A reply frame with data is used for replying to the input instruction which requests the data and the current value read instruction to the timer/counter A.

**Replay to Start and Output Instructions:** The PIOC-101 determines whether that instruction is correct and acceptable, and returns an acknowledge frame if the instruction is correct and executable, and an error code through the special data frame if not.

# ● *3-4 Frame Structure for 8-bit ASCII Mode*

This section describes the communication protocol for the 8-bit ASCII mode of the PIOC-101. This protocol can utilize general UART hardware used for personal computers, dispensing with any special hardware.

## ■ 3-4.1 Control Code Structure

Only the control code has the Bit-7(MSB) set to "1", being structured as shown in the table below. The Bit-6 is set to "1" when selecting the PIOC-101. The Bits-3 to -0 specify a slave address. The Bits-5 and -4 represent a frame type.

| Bit | Value | Meaning | |
|---|---|---|---|
| | | Master sending frame | Slave reply frame |
| 7, 6 | 11 | Device selection bit (11 for PIOC-101) | |
| 5, 4 Frame type | 00 | Polling frame | No-status-change (operating) reply |
| | 01 | Instruction data frame | Acknowledge reply (stopping) |
| | 10 | Undefined | Reply with data |
| | 11 | Undefined | Reply with special data |
| 3,2,1,0 | | Device address (Select with DEVADR3 to DEVADR0) | |

## ■ 3-4.2 Data Portion Structure

The data portion has variable length. Some frames have no data portion. Normal data represents 1-byte binary data in 2-byte ASCII code.
The ASCII code is sent as it is for the special data which can be represented only with one byte(convertible into 7 bits), that is, an error code and version code.

## ■ 3-4.3 Checksum Calculation

Checksum is created by reversing all the bits to set the MSB(Bit-7) to "0" after binary addition of the control code through the end of the data portion.

## ■ 3-4.4 Control Protocol

For both master and slave frames, the Bits-5 and -4 of the control code represent the frame type. The following describes the communication procedure.

### 1. Transmission frame activated by the master

There are two types of frames sent from the master side; they are a polling frame and an instruction data frame which gives the instructions to the PIOC-101.

**Polling frame:** This frame does not have the data portion and consists of only two bytes; the control code and checksum. Since the multidrop communication system does not allow the slave side to transmit the data without knowing the status of the transmission line, the master side always needs polling to monitor the status of the PIOC.

**Instruction data frame:** This frame includes the instruction code and data to the PIOC-101 in the data portion.

### 2. Frames returned by the slave

The PIOC-101(slave) returns four types of frames.

**Reply to Polling Frame:** If there is no change to the input port of the PIOC, the slave returns no-status-change frame, and if there is any, it returns a frame with data. It returns a frame with special data frame to the polling frame received immediately after termination of the PIOC's timer/counter.

**Reply to Data Request Instruction:** A reply frame with data is used when replying to the input port read instruction to request the data and the current value read instruction to the timer/counter A.

**Reply to Start Instruction and Output Instruction:** The PIOC-101 determines whether that instruction is correct and acceptable, and returns an acknowledge frame if the instruction is correct and executable, and returns a reply frame with specific data(error code) if not.

### Remedy for Communication Error

The PIOC-101 adds the checksum to each frame in order to prevent communication errors. If the checksum of the received data is faulty, an error code("0x16" for the 9-bit binary mode, and "W" for the ASCII mode) is returned.

The incorporated UART detects a framing error and overrun error, but does not return any error code to these errors, storing it internally. This is because if multiple PIOCs are connected to an identical circuit and such a hardware-wise error is encountered, it is impossible to immediately determine whether it is directed to the said PIOC.

Therefore, the host needs to wait a sufficient time conceived necessary to receive a reply frame and deal with a timeout error. If this often happens, it may be necessary to improve the hardware or noise environment. It could be effective to slow down a communication rate, depending on the case, but may pose a problem in terms of system throughput.

# ◆ 4 DETAILS OF INSTRUCTIONS

There are four types of instructions. They are distinguished by the Bits-7 and -6 of the instruction code, respectively. The Bits-5 to -0 are used to specify a built-in device.

Instruction Code:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| C | C | Bits to specify the built-in device | | | | | |

CC: Instruction type designating bits

00 : Initialize instruction
01 : Input and extend instructions
10 : Output instruction
11 : Start instruction

## ● 4-1 Initialize Instruction

The initialize instruction is to specify the hardware configuration of the PIOC-101. It specify the input/output ports and the operating mode of the timers/counters. This instruction must be given first after the PIOC has been reset. All the ports of the PIOC have been set to the input mode until this instruction is given. Only the extend instruction can be given before initialization. Any non-extend instruction is ignored, returning an initialization incomplete error.

The instruction consists only of a 1-byte instruction code and the instruction data is included in the Bits-5 to -0 of the code. If the PIOC receives the instruction successfully, the acknowledge frame is returned.

The initialize instruction can be repeatedly executed by different setting. If the initialize instruction results in an error, the setting so far becomes valid.

Byte-1: Instruction code of the initialize instruction

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | TCMA | | P3 | P2 | P1 | P0 |

TCMA: Timer/counter A operating mode

00 : Counter mode
01 : Timer mode
10 : Encoder input counter mode
11 : TCMA holds the previously set mode.(Note 1)

P3, P2, P1, P0 : Setting of the port input/output status (Note 2)

1 : Output port
0 : Input port

If initial setting is "11," an error is returned.

The port with STR/Output set to "L" cannot be set for output.(Error 7)

## ● 4-2 Input Instruction

The input instruction is to specify the input port and timer/counter to be read. The instruction consists only of a 1-byte instruction code and the instruction data is included in the Bits-4 to -0 of the code. A return value has variable length. This is the frame with the data portion of up to 7 bytes.
If the timer/counter is specified, it refers to the timer/counter A and its 24-bit current value is initially output. If all the read designated bits are "0", an error is returned.

Byte-1: Instruction code of the input instruction

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | TC | P3 | P2 | P1 | P0 |

TC: Designation to read the timer/counter A current value

P3, P2, 1, 0: Designation of the input port to be read

Example of Input Instruction Return Value: (When the timer/counter A and Ports-2 and -0 are specified)

Byte-1: Current value of the timer/counter A (Lower 8 bits)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Current value of the timer/counter A (Lower 8 bits) | | | | | | | |

Byte-2: Current value of the timer/counter A (Middle 8 bits)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Current value of the timer/counter A (Middle 8 bits) | | | | | | | |

Byte-3: Current value of the timer/counter A (Upper 8 bits)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Current value of the timer/counter A (Upper 8 bits) | | | | | | | |

Byte-4: Port-2 status

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

Byte-5: Port-0 status

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

If the Bit-5 of the instruction code is "0", the instruction is treated as the extend instruction. If this is the case, its function differs depending on the values of the Bits-3 to -0.(See Section 4.5)

## ● *4-3 Output Instruction*

The data set with the output instruction include the initial value of the encoder, preset value of the encoder or timer/counter A, and set values of the output ports. The instruction specifies the data set with the Bits-5 to -0 of the instruction code. Therefore, this instruction always has the data portion accompanying it and its length is variable. The order of the data is the same as the return value for the input instruction. Designation of the encoder initial value comes first, if any, and is given the first 3 bytes starting from the lower 8 bits; if designation of the preset value of the timer/counter A follows, the next 3 bytes are given, and the third 3 bytes to designation of the output ports, sequentially from the Port-3. If the instruction is received successfully, the acknowledge frame is returned.
Setting of the timer/counter A is accepted only when it is stopping. If you attempt to set while it is operating, Error-5 is returned.

Byte-1: Instruction code of the output instruction

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | TS | TP | P3 | P2 | P1 | P0 |

TS : Designation to set the encoder initial value
TP : Designation of the timer/counter A preset value
P3, 2, 1, 0 : Designation of the output ports

Instruction Data of Output Instruction (When the preset value of the timer/counter A and the Ports-2 and -0 are specified)
Byte-2: Lower 8 bits of the timer/counter A set value

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Set value of the timer/counter A (Lower 8 bits) | | | | | | | |

Byte-3: Middle 8 bits of the timer/counter A

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Set value of the timer/counter A (Middle 8 bits) | | | | | | | |

Byte-4: Upper 8 bits of the timer/counter A

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Set value of the timer/counter A (Upper 8 bits) | | | | | | | |

Byte-5: Port-2 set value

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

Byte-6: Port-0 set value

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

The output instruction to the port set for input results in an error.(Error-6)

If this instruction has all the device designation bits set to "0", it is interpreted as the stop instruction. If this is the case, no data portion exists. The stop instruction stops both timers/counters A and B, plus sampling of the input ports.

## ● 4-4 Start Instruction

The start instruction has functions to start the timers/counters and sampling of the input ports. It starts the devices specified with the device designation bits of the instruction code. The timers/counters start operating only after receiving this instruction. They are reset to 0 at the time of start, but the preset value is stored. The timers/counters and sampling of input can be stopped by the extend or stop instruction. This instruction does not have the data portion and returns the acknowledge frame when successfully received.

Byte-1: Instruction code of the start instruction

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | TCB | TCA | P3 | P2 | P1 | P0 |

TCB : Designation to start the timer/counter B

TCA : Designation to start the timer/counter A

P3, 2, 1, 0 : Designation to start sampling the input ports

## ● 4-5 Extend Instruction

The extend instruction can be either input or output instruction, if the Bit-5 of the instruction code of the input instruction is "0". Its function is specified with the values in the Bits-3 to -0.

Byte-1: Instruction code of the extend instruction

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | x | Specifies the extend instruction's function | | | |

Function designation codes for the extend instruction:

0001 : Stops the timer/counter B.

0010 : Stops the timer/counter A.

0011 : Stops the timers/counters A and B.

0100 : Specifies the operating mode of the timer/counter.(Counter mode)

0101 : Specifies the operating mode of the timer/counter.(Timer mode in increments of 8 μs)

1000 : Error code read instruction

1010 : Version code read instruction

1100 : Error counter read instruction

1111 : Status read instruction (Same as the poll instruction)

x: This bit is meaningless.

## ● 4-6 Timer/Counter Stop Instruction

The timer/counter stop instruction uses the Bits-1 and -0 to specify the counter you want to stop. Setting both bits to "1" stops the counters A and B. This instruction has no data portion.
If it is received successfully, it returns the acknowledge frame. If the timer/counter stops, its current value is reset to "0". To restart, issue the start instruction.
This instruction is classified as the output instruction under the control of the MWSC-101.

Byte-1: Instruction code of the extend instruction (Timer/counter stop instruction)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | x | 0 | 0 | TCB | TCA |

TCB : Specifies the timer/counter B.
TCA : Specifies the timer/counter A.

**Timer/Counter B Operating Mode Designation Mode**

The instruction to set the timer/counter B gives an instruction code to specify the timer/counter B's operating mode and clock source, and a 24-bit preset value. If it is received successfully, it will return the acknowledge frame. This instruction only specifies the operating mode and does not start the timer/counter B.
This instruction is classified as the output instruction under the control of the MWSC-101.

Byte-1: Instruction code of the extend instruction (When setting the timer/counter B to the counter mode)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | x | 0 | 1 | 0 | 0 |

Byte-2: Lower 8 bits of the timer/counter B preset value

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Timer/counter B preset value (Lower 8 bits) | | | | | | | |

Byte-3: Lower 8 bits of the timer/counter B preset value

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Timer/counter B preset value (Lower 8 bits) | | | | | | | |

Byte-4: Lower 8 bits of the timer/counter B preset value

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Timer/counter B preset value (Lower 8 bits) | | | | | | | |

## ● 4-7 Error Code Read Instruction

This instruction allows you to read the internal error information of the PIOC-101. This information is represented by 1-byte code; its meaning is as shown in 6. ERROR CODES LIST. A reply to the error code read instruction takes the form of regular data frame. Once the error code is read, it is cleared.
This instruction is classified as the input instruction under the control of the MWSC-101.

Byte-1: Instruction code of the extend instruction (Error code read)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | x | 1 | 0 | 0 | 0 |

Return Value to Version Code Read Instruction:
Byte-1: Error code

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Error code | | | | | | | |

## ● 4-8 Status Read Instruction

This instruction has the same function as the polling frame described in the next section.
Its return data is also identical. This instruction is classified as the input instruction under the control of the MWSC-101.

Byte-1: Instruction code of the extend instruction (Status read)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | x | 1 | 1 | 1 | 1 |

## ● 4-9 Version Code Read Instruction

This instruction allows you to confirm the version information of the PIOC-101. This information is represented by 1-byte code; the current version is "0x41."
This instruction is classified as the input instruction under the control of the MWSC-101.

Byte-1: Instruction code of the extend instruction (Version code read)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | x | 1 | 0 | 1 | 0 |

Return Value to Version Code Read Instruction:
Byte-1: Version code

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Version code (0x41) | | | | | | | |

## ● 4-10 Error Counter Read Instruction

The communication error counter is a 16-bit counter to count communication errors. The PIOC-101 has a register to hold the communication error status such as a framing error, overrun error, which is read with this error counter read instruction. The communication error status reports the last one of the recorded communication errors. In this case, therefore, the return value is of 3 bytes. The internal error counter is reset by executing this instruction.
This instruction is classified as the input instruction under the control of the MWSC-101.

Byte-1: Instruction code of the extend instruction (Error counter read)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | x | 1 | 1 | 0 | 0 |

Return Value to Error Counter Read Instruction:
Byte-1: Error counter value (Lower 8 bits)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Error counter value (Lower 8 bits) | | | | | | | |

Byte-2: Error counter value (Upper 8 bits)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Error counter value (Upper 8 bits) | | | | | | | |

Byte-3: Communication error status

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | OVR | 0 | FE | 0 | 0 |

OVR: Overrun error
FE: Framing error

## ● 4-11 Polling

The PIOC-101 is controlled by polling from the host. Once the PIOC-101 receives a polling frame, it checks the status change of the activated input ports and timer/counter, and returns the reply frame, "No Status Change," if there is no change. In this case, if there are no activated devices, the "Ready(Acknowledge)" frame is returned, and if the devices are operating, the "Busy(No Change)" frame is returned.(The Busy frame is the same as the polling frame given by the host.)

If there is any status change, a special frame with data is used to return the status byte and input port data(if the status of the input port changed). The following exemplifies the transmission/reception sequence for the 9-bit binary mode.

Master Transmission Frame:

Byte-0: Polling frame control mode

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | Device address | | | |

Byte-1: Checksum of the polling frame control code

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Checksum | | | | | | | |

Slave Reply Frame:

Byte-0: Special reply frame control code

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | Device address | | | |

Byte-1: Status byte

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | TCB | TCA | P3 | P2 | P1 | P0 |

TCB : Timer/counter B end

TCA : Timer/counter A end

P3, 2, 1, 0 : Input port status change

(The following data are applicable, for example, when P2 and P0 are "1" and their input status changes.)

Byte-2: P2 input

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

Byte-3: P0 input

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

Byte-4: Checksum of the Bytes-0 to -3

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Checksum of the Bytes-0 to -3 | | | | | | | |

There are no data portions corresponding to the termination of the timer/counter.

# ◆ 5 INPUT/OUTPUT SIGNALS

Table 5-1 lists the pin assignment and input/output signals of the PIOC-101, and their brief functions.

**Table 5-1 PIOC-101 Input/Output Signals List**

| Pin No. | Signal Name | I/O | Function |
|---|---|---|---|
| 1 | RST/ | O | Input strobe |
| 2 | MOD0 | I | Serial communication baud rate control Bit-0 |
| 3 | MOD1 | I | Serial communication baud rate control Bit-1 |
| 4 | MOD2 | I | Serial communication mode selection (Binary: L) |
| 5 | HSP/ | I | High-speed protocol designation (High speed: L) |
| 6 | RXD | I | Serial communication reception input signal |
| 7 | SEND | O | Transmission gate control output |
| 8 | TXD | O | Serial communication transmission output signal |
| 9 | P20 | I/O | Port-2 Bit-0 |
| 10 | P21 | I/O | Port-2 Bit-1 |
| 11 | P22 | I/O | Port-2 Bit-2 |
| 12 | P23 | I/O | Port-2 Bit-3 |
| 13 | P24 | I/O | Port-2 Bit-4 |
| 14 | P25 | I/O | Port-2 Bit-5 |
| 15 | P26 | I/O | Port-2 Bit-6 |
| 16 | P27 | I/O | Port-2 Bit-7 |
| 17 | P00 | I/O | Port-0 Bit-0 |
| 18 | P01 | I/O | Port-0 Bit-1 |
| 19 | P02 | I/O | Port-0 Bit-2 |
| 20 | P03 | I/O | Port-0 Bit-3 |
| 21 | P04 | I/O | Port-0 Bit-4 |
| 22 | P05 | I/O | Port-0 Bit-5 |
| 23 | P06 | I/O | Port-0 Bit-6 |
| 24 | P07 | I/O | Port-0 Bit-7 |
| 25 | NC | O | |
| 26 | GND | I | Power GND |
| 27 | X1 | I | Quartz oscillator pin-1 (16 MHz) |
| 28 | X2 | I | Quartz oscillator pin-2 (16 MHz) |
| 29 | EA | I | Connect to +5 V |
| 30 | P10 | I/O | Port-1 Bit-0 |
| 31 | P11 | I/O | Port-1 Bit-1 |
| 32 | P12 | I/O | Port-1 Bit-2 |
| 33 | P13 | I/O | Port-1 Bit-3 |
| 34 | P14 | I/O | Port-1 Bit-4 |
| 35 | P15 | I/O | Port-1 Bit-5 |
| 36 | P16 | I/O | Port-1 Bit-6 |
| 37 | P17 | I/O | Port-1 Bit-7 |
| 38 | CLK | O | System clock(4 MHz) output |

| | | | |
|---|---|---|---|
| 39 | ENDA/ | O | Timer/counter A end output |
| 40 | ENDB/ | O | Timer/counter B end output |
| 41 | RESET/ | I | Reset input |
| 42 | P30 | I/O | Port-3 Bit-0 |
| 43 | P31 | I/O | Port-3 Bit-1 |
| 44 | P32 | I/O | Port-3 Bit-2 |
| 45 | P33 | I/O | Port-3 Bit-3 |
| 46 | P34 | I/O | Port-3 Bit-4 |
| 47 | P35 | I/O | Port-3 Bit-5 |
| 48 | P36 | I/O | Port-3 Bit-6 |
| 49 | P37 | I/O | Port-3 Bit-7 |
| 50 | STR0/ | I/O | Port-0 output strobe or input port designation |
| 51 | STR1/ | I/O | Port-1 output strobe or input port designation |
| 52 | STR2/ | I/O | Port-2 output strobe or input port designation |
| 53 | STR3/ | I/O | Port-3 output strobe or input port designation |
| 54 | CPIB | I | Counter B pulse input |
| 55 | STA, DIR | I | Timer A start input or encoder direction signal input |
| 56 | CPIA | I | Counter A pulse input |
| 57 | CDIR | I | Encoder direction change signal input |
| 58 | Vcc | I | Power 5 V |
| 59 | NC | I | |
| 60 | GND | I | Power GND |
| 61 | DEVARD0 | I | Device address bit 0 |
| 62 | DEVARD1 | I | Device address bit 1 |
| 63 | DEVARD2 | I | Device address bit 2 |
| 64 | DEVARD3 | I | Device address bit 3 |

A slash "/" in the table represents negative logic. 0 = output, I = input, NC = Unused

Unused input pins should be pulled up or down with 10kΩ resistors.

# ● *5-1 System Setting Input*

The system setting input signals are to set the system baud rate and communication protocol.

## ■ 5-1.1 MOD2, MOD1, MOD0 (Communication Mode and Speed Setting Input)

MOD2, MOD1, and MOD0 are the input signals designed to set the mode and baud rate which are used to communicate with the slave. Table 6-1 shows their set values and the relations between the communication modes and baud rates. If they are set to "00," the PIOC are deactivated and does not run.

**Table 5-2 Communication Modes and Baud Rate Setting Table**

| MOD3 | MOD 1 | MOD0 | Baud Rate Setting |
|---|---|---|---|
| x | 0 | 0 | Undefined |
| 0 | 0 | 1 | Binary mode 31.25 kbps |
| 0 | 1 | 0 | Binary mode 62.5 kbps |
| 0 | 1 | 1 | Binary mode 125 kbps |
| 1 | 0 | 1 | ASCII mode 19.2 kbps |
| 1 | 1 | 0 | ASCII mode 41.67 kbps |
| 1 | 1 | 1 | ASCII mode 83.33 kbps |

## ■ 5-1.2 HSP/ (High-speed Protocol Setting Input)

HSP/ is a signal designed to specify whether a high-speed busy check mechanism should be used in communication with the MWSC-101. If HSP/ is "L", the PIOC-101 replies to the status check instruction from the MWSC without waiting for the checksum. A similar mechanism can be also specified on the MWSC side and use of this method allows you to almost double a polling rate.

## ■ 5-1.3 DEVADR3 to DEVADR0 (Device Address Setting Input)

The PIOC is identified by a 4-bit address on the multidrop communication circuit. It is set from the outside with a DIP switch, etc.

## ● *5-2 Host Communication Interface*

### ■ 5-2.1 TXD, RXD (Host Communication Interface Signals)

Communication with the PIOC is 9-bit or 8-bit asynchronous communication. The baud rate and communication mode are set with MOD2, MOD1, and MOD0 as previously described. TXD is a transmission output pin and RXD a reception input pin.
TXD is of open drain output and able to wired-OR multiple outputs.

### ■ 5-2.2 SEND (Transmission Gate Control Output Signal)

This signal is set to "H" while the PIOC-101 is sending the data. Normally, this signal is connected to a communication transceiver's transmission gate to secure and open a communication path.
In multidrop communication, the communication circuit is connected to all the slaves. The host starts communication and the slave, PIOC, replies to this. After receiving the reply from the slave, the host start communicating with other slaves. Therefore, the slave which has finished transmission needs to open the communication path.

## ● *5-3 System Hardware Related Signals*

### ■ 5-3.1 RESET/ (Reset)

This signal is to reset the PIOC-101 to the initial conditions. Normally, it is connected to the system's reset signal. After rising from the "L" level, the initialize instruction is given by an instruction from the host processor. The reset signal needs to hold the "L" level at least for 2μs or more when the supply voltage is within the operating range of the PIOC-101 and after the oscillations of an internal oscillator have been stabilized.

### ■ 5-3.2 X1, X2 (Quartz Oscillator)

The X1 and X2 pins the system clock inputs for the PIOC-101. Normally, they are connected to the 16 MHz quartz oscillators as shown in the left figure of Fig. 5-1, and can be also connected to 2-phase external clocks as shown in the right figure of Fig. 5-1.
X1 and X2 input frequency can input a clock ranging from 1 MHz to 16 MHz. The PIOC-101's operating speed is proportional to this clock. The time and other data prescribed in the following description are based on this reference clock. Particularly, unprescribed time, speed, data, etc. show the values applied when the reference clock is 16 MHz.

### ■ 5-3.3 Vcc, GND (Power Input)

Vcc is connected to +5 V +/- 10 % DC power supply and GND to 0 V, respectively. Connect a capacitor to between both pins with the shortest wiring in order to bypass a high frequency.

### ■ 5-3.4 CLK (System Clock Output)

This is a clock signal output equivalent to one fourth of the system clock frequency(4 MHz when the system clock is 16 MHz). It is available outside.

## ● *5-4 User Input/Output Signals*

These are the input/output signals available to the user. They include input/output port signals, output strobe signals, input strobe signals, counter input signals, timer start input signals, encoder direction input signals, and timer/counter end output signals.

### ■ 5-4.1 P00-P07, P10-P17, P20-P27, P30-P37 (Port Input/Output Signals)

These are 4 sets of 8-bit input/output signals for the input/output ports. Either input or output can be defined for each port, using the initialize instruction. All the ports are programmed for the input mode until the initialize instruction is given.
If they are programmed for the output mode, the strobe outputs corresponding to the respective output ports(see the next section) are activated.

### ■ 5-4.2 STR0/, STR2/, STR3/ (Output Strobe Signals or Input Setting)

These are the negative output strobe signals made effective to the input/output ports mentioned above when those ports are programmed for output. The pulse width is 100 μs or more. Be sure to pull them up if they are not used.
If these signal pins are set to "L", the corresponding ports are designated as input ports. This mechanism is designed to prevent the ports from being programmed for output when they have been hardware-wise programmed for input. When the signal pins are set to "H" through external pull-up, the ports can be programmed for either input or output.

### ■ 5-4.3 RST/ (Input Strobe Signal)

This signal is output immediately before the input port is read by the start instruction and set to "H" after reading is completed. It is an output of negative logic with the pulse width of 20 μs.

### ■ 5-4.4 STA (Timer Start Input Signal), DIR (Encoder Direction Signal)

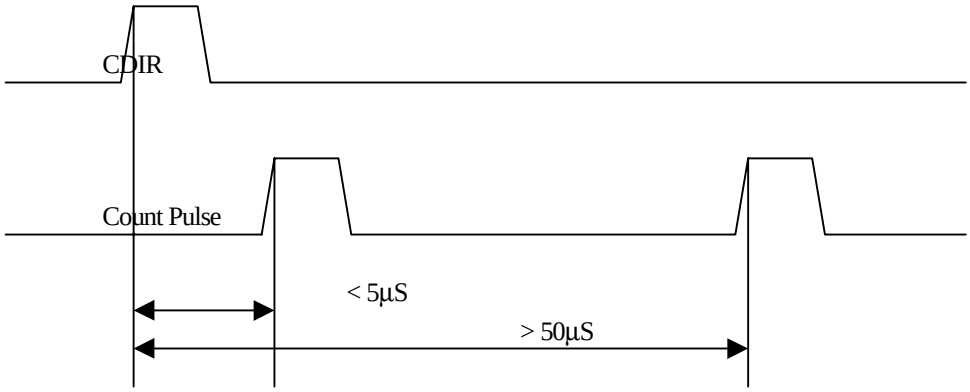
If the timer/counter A is in the timer mode and the timer A has been activated, counting starts at a rise of this signal. STA is of positive pulse and needs the pulse width of 600 ns or more when the system clock is 16 MHz.
If the timer/counter A is in the encoder mode, the signal is used as a DIR input. Connect it to an encoder rotating direction signal. "0" for CW and "1" for CCW.

## ■ 5-4.5 CDIR (Encoder Direction Change Pulse Input Signal)

When the timer/counter A is in the encoder mode, direction signal change pulses are input to this pin. This signal gives a rise or fall edge when the encoder direction signal mentioned in 5-4-4 changes. It gives positive pulses when the direction changes. These signals and the pulse inputs mentioned in the sections below enable functioning as an encoder counter.

External PLD is separately provided to convert the 2-phase clock from the encoder into the count pulses, and direction signal and direction change pulse signal. Required pulses are positive ones with the pulse width of 600 ns or more when the system clock is 16 MHz. Minimum required direction signal change interval is 100 µs. If the signal is changed at shorter intervals, the PIOC cannot count those pulses correctly.

See the figure below for the limitations on the timings of CDIR and count pulse.




## ■ 5-4.6 CPIA (Counter-A Pulse Input Signal)

This is a pulse input pin for the counter mode and encoder mode of the timer/counter A. The maximum input pulse rate is 1.5 MHz when the system clock is 16 MHz. The pulses are counted at a rise and require the minimum width of 300 ns at both "H" and "L" levels.

## ■ 5-4.7 CPIB (Counter-B Pulse Input Signal)

This is a pulse input pin for the counter mode the timer/counter B. The maximum input pulse rate is 1.5 MHz when the system clock is 16 MHz. The pulses are counted at a rise and require the minimum width of 300 ns at both "H" and "L" levels.

## ■ 5-4.8 ENDA/, ENDB/ (Timer/Counter End Signal)

These signals are output at time-up or count-up when the preset value of the timer/counter has been set. ENDA/ is a timer/counter A end output and ENDB/ a timer/counter B end output.

The ENDA/ output of the timer/counter A is held until the next start signal ST/ is input in case of the timer mode(rear edge of ST/), and until the next count pulse is input in case of the counter mode or encoder mode.

For the timer/counter B, the ENDB/ holding time is from 100µs to less than 250µs in both timer and counter modes.

# ◆ 6 ERROR CODES LIST

If an instruction from the host is free from any communication error, the PIOC-101 returns the acknowledge frame, but it returns the error codes listed below to the erroneous instructions.

**Table 6-1 PIOC-101 Error Codes List**

| Error Code | | Error Description |
|---|---|---|
| Binary | ASCII | |
| 0 | A | No error |
| 1 | B | Undefined instruction error |
| 2 | C | Incapable of processing due to incomplete initialization. |
| 3 | D | Timer/counter A mode setting error |
| 4 | E | Timer/counter A mode inconsistent |
| 5 | F | Gave the set or start instruction to the operating timer/counter. |
| 6 | G | Port designation error (Output to the input port or output port activated) |
| 7 | H | Programmed for output the port where STR/output had been set to "L". |
| 8 | I | All read designations were in the input instruction. |
| 9 | J | No device designation data in the start instruction. |
| 10 | K | Received the initialize instruction during operation. |
| 11 | L | Received the start instruction despite no mode had been set for the timer/counter B. |
| 12 | M | Preset position too close to detect at encoder start. |
| | | |
| 22 | W | Checksum error |
| 23 | X | Communication hardware error |

An error report frame to polling is a reply frame with special data.
A replay to the error code read instruction depends on the normal data frame.
In the ASCII mode, the error codes have been converted into the ASCII codes as shown in the table above and output in one byte without converting them by every 4 bits again.

# ◆ 7 RATINGS

## ● 7-1 Absolute Maximum Ratings

Table 1 "Absolute Maximum Ratings" shows the absolute ratings of the PIOC-101. If it is used beyond the absolute maximum ratings, it may be deteriorated or destroyed permanently.

**Table 1 Absolute Maximum Ratings**

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | Vcc | -0.5 - +6.5 | V |
| Input voltage | Vin | -0.5 - +Vcc +0.5 | V |
| Power consumption (Ta = 85°C) | Pd | 500 | MW |
| Operating temperature | Topr | -40 - +85 | °C |
| Storage temperature | Tstg | -65 - +150 | °C |
| Soldering temperature (10s) | Tsolder | 260 | °C |

## ● 7-2 DC Characteristics

Table 2 "DC Characteristics" shows the DC characteristics of the PIOC-101.

**Table 2 DC Characteristics**

| Item | | Symbol | Min | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Input "Low" level voltage | RESET | $V_{iL}$ | -0.3 | 0.25Vcc | V | |
| | X1 | | -0.3 | 0.2Vcc | | |
| | Others | | -0.3 | 0.3Vcc | | |
| Input "High" level voltage | RESET | $V_{iH}$ | **0.75Vcc** | Vcc +0.3 | V | |
| | X1 | | **0.8Vcc** | Vcc +0.3 | | |
| | Others | | **0.7Vcc** | Vcc +0.3 | | |
| Output "Low" level voltage | All output pins | $V_{OL}$ | | 0.45 | V | $I_{OL}$=1.6mA |
| Output "High" level voltage | AUXO0 ~ AUXO7 | $V_{OH}$ | 2.4 | | V | $I_{OH}$= -400µA |
| | Others | | 0.75Vcc | | | $I_{OH}$= -100µA |
| Darlington drive current (Sum of AUXO0 to AUXO7) | | $I_{DR}$ | -1.0 | -3.5 | mA | |
| Input leak current | | $I_{LI}$ | 0.02 (TYP) | ±5 | mA | |
| Output leak current | | $I_{LO}$ | 0.05 (TYP) | ±10 | mA | |
| Current consumption | | $I_{CC}$ | 35 (TYP) | 50 | mA | |
| Input capacity | input pins | $C_{IN}$ | | 10 | PF | |

Vcc = 5 V ± 10 %, Ta = -20 to 70 deg. C (1 to 16 MHz)

TYP values are applicable at Ta = 25 deg. C and Vcc = 5 V.

The Darlington drive current refers to an output allowable current used to drive a Darlington transistor, etc. with an auxiliary output signal.

## ● *7-3 AC Characteristics*

## ● *7-4 PIOC-101 Outer Dimensions Drawing*

[Unit: mm]

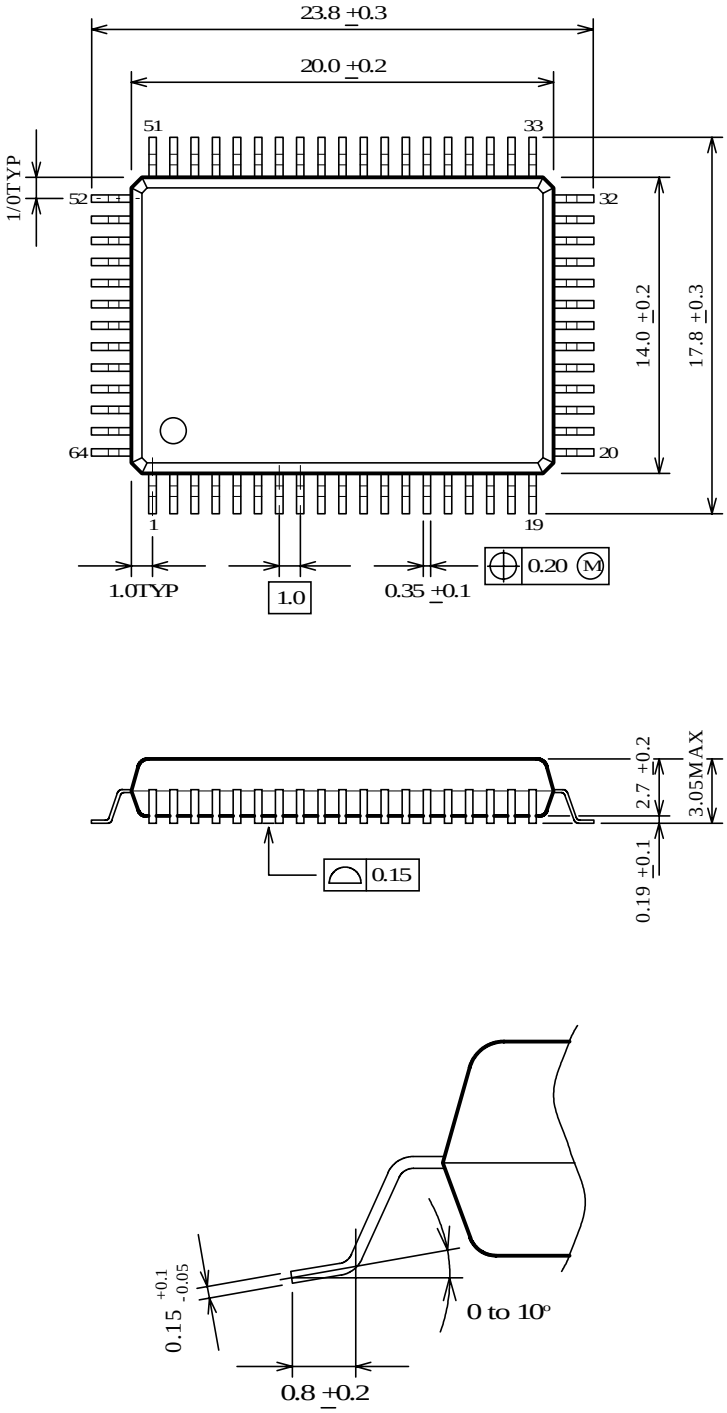



**Fig. 1 Outer Dimensions Drawing**

# ◆ 8 RECOMMENDED MOUNTING CONDITIONS AND PRECAUTIONS FOR HANDLING

The PIOC-101 AFP package is surface mounting. When mounting it onto a printed circuit board, contamination by flux, etc. and thermal stress by soldering are the most critical problems as effects on the reliability of the PIOC-101. The following describes a recommended temperature profile for each mounting method and general precautions.

## ● 8-1 Temperature Profile

### ■ 8-1.1 When Using the Soldering Iron

Solder the leads within 10 seconds at 260 deg. C or 3 seconds at 350 deg. C.

### ■ 8-1.2 When Performing Far/Medium Infrared Reflow

It is recommended to use a vertical heating method with far/medium infrared rays.
The maximum package surface temperature is 240 deg. C; perform within 30 seconds at 210 deg. C or higher.
Fig. 2 "Temperature Profile" shows a recommended temperature profile.
Note that near infrared reflow will cause thermal stress similar to solder dip.

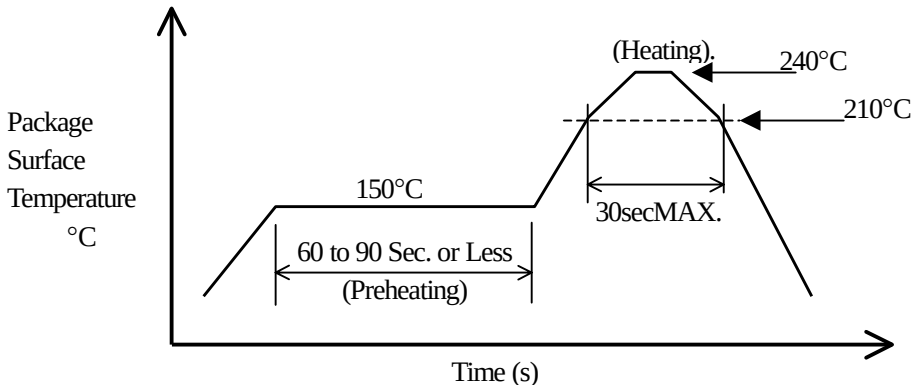



**Fig. 2 Temperature Profile**

### ■ 8-1.3 When Performing Hot Air Reflow

The maximum package surface temperature is 240 deg. C; perform within 30 seconds at 210 deg. C or higher.
See Fig. 2 "Temperature Profile" for a recommended temperature profile.

## ■ 8-1.4 When Performing Vapor Phase Reflow

Our recommended solvent is Florinate FC-70 or its equivalent.
Perform within 30 seconds at atmospheric temperature of 215 deg. C or 60 seconds at 200 deg. C.
Fig. 3 "Temperature Profile" shows a recommended temperature profile at V. P. S.

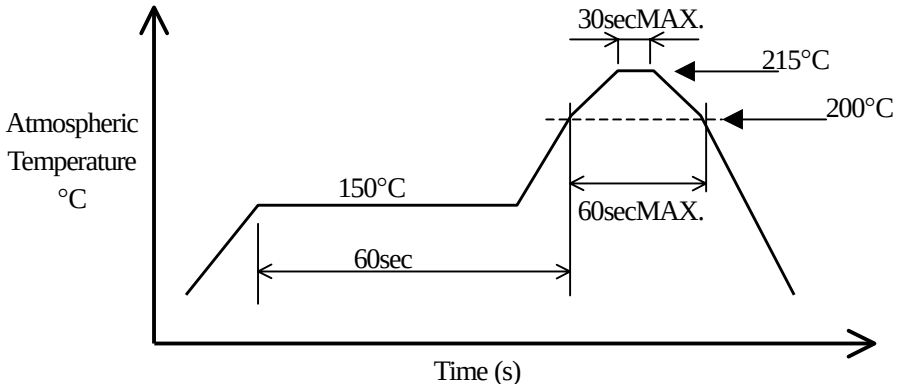



**Fig..3 Temperature Profile**

## ■ 8-1.5 When Performing Solder Dip

Perform preheating for 60 seconds or longer at 150 deg. C.
For solder flow of up to 260 deg. C, perform within 10 seconds.

## ■ 8-1.6 Flux Cleaning (Supersonic Cleaning)

Conduct flux cleaning so that no reactive ions such as Na, Cl will not remain. Organic solvents may react to water, produce a corrosive gas such as hydrogen chloride, thus deteriorating the PIOC-101.
During a cleaning process or with a cleaning agent adhered to the PIOC-101, do not rub the indication mark surface with a brush or hand. The indication mark may be defaced.
Immersion cleaning, shower cleaning, and steam cleaning depend on the chemical action of the solvent used. Be careful in choosing the solvent. The immersion time in the solvent or steam should be within one minute at liquid temperature of 50 deg. C or lower.
When employing supersonic cleaning which shows a cleaning effect in a short time, the following basic conditions are recommended. Float in the solvent so that a supersonic vibrator will not come into direct contact with the printed circuit board or PIOC-101.
Recommended Conditions for Supersonic Cleaning

| | |
|---|---|
| Frequency | : 27 kHz to 29 kHz |
| Supersonic output | : 300 W or less (0, 25 W/cm$^2$ or less) |
| Cleaning time | : 30 seconds or less |

## ■ 8-1.7 Board Coating

When using for the devices requiring high reliability or those used in the unfavorable environment(humidity, corrosive gas, dust, etc.), take into consideration the effects of stress,impurities, etc. as to use of damp-proof coating for the printed circuit board.
There are many different kinds of coating resin and they have been almost experientially chosen. It is not known what thermal and mechanical stresses will be applied to the PIOC-101. When you use the coating resin, review them fully.

## ■ 8-1.8 Deterioration and Destruction due to Static Discharge

When handling the PIOC-101 alone, the worker should wear electrification preventive clothes in the environment free from static electricity. For the containers, etc. which come into direct contact with the PIOC-101, use an electrification preventive material and earth them via a protective resistor of 0.5 to 1 MΩ.

## ■ 8-1.9 Management of Work Environment

If the humidity decreases in the work environment, a human body or insulator are subject to static electricity. It is recommended to keep the humidity at 40 to 60 %, considering absorption of humidity by the PIOC-101.
Earth the apparatuses and jigs which have been installed in a work area.
Spread a conductive mattress on the floor of the work area to protect the floor surface from generation of static electricity, and earth it.
Spread a conductive mattress, etc. on the work bench surface to diffuse static electricity, and earth it. The work bench surface must not be the metallic surface which may generate abrupt discharge at low resistance when the electrified PIOC-101 comes into direct contact with it.
Use a VDT filter, etc. to protect the CRT surface in the work area against electrification and avoid turning on/off during work as much as possible, because this may induce an electric field to the PIOC-101.
Cover a work chair with electrification preventive fiber and earth it to the floor with an earthing chain.
Spread a static electricity preventive mattress on the surface of the IPIC-101 storage shelf.
Use a static electricity dissipative material or static electric preventive material for the containers used for transportation and temporary storage of the PIOC-101.
The static electricity control area should be provided with an earthing conductor exclusively designed as a static electricity prevention. You can use an earthing conductor(Class-3) for a power transmission circuit, but it is not allowed share the earthing conductor used for the apparatuses.
When using an automated system, pay attention to the following.
When picking up the PIOC-101 package surface through vacuum, attach conductive rubber, etc. to the nose of the pickup to prevent electrification.
Minimize friction on the PIOC-101 package surface. If it is inevitable due to the mechanism, reduce the friction surface or use a material with lower friction factor or electrical resistance, and ionizer, etc.
Use a static electricity dissipative material for the contact area with the lead pins of the PIOC-101.
Do not allow any charged body(work uniform, human body, etc.) to come into contact with the PIOC-101.
The jigs/tools used in the processes should be kept away from the PIOC-101, so that they will not come into contact with it.

## ■ 8-1.10 Precautions for Work

The worker should wear static electricity preventive clothing and conductive shoes.
The worker should wear a wrist strap and earth it through a resistance of about 1 MΩ.
Use a low-voltage soldering iron and have its nose earthed.
use static electricity preventive tweezers which are more likely to come into contact with the lead pins of the PIOC-101. Avoid using metallic ones if possible, because they will cause the electrified PIOC-101 to abruptly discharge at low resistance. When using vacuum tweezers, attach a conductive adsorptive pad to their nose and earth them with an earthing conductor exclusively designed as a static electricity prevention.
Do not place the PIOC-101 or its storage container near any high-electric field source(on the CRT, etc.).
The printed circuit boards with mounted PIOC-101 should not be directly piled upon each other; space them out in a container with an electrification prevention. Otherwise, friction could cause electrification and discharge.
When someone has to touch the PIOC-101, wear finger sacks, gloves, etc. which have a static electricity prevention as much as possible.
If the wrist strap cannot be used or the PIOC-101 could be subject to friction, use the ionizer.

# ● *8-2 Precautions for Working Environment*

## ■ 8-2.1 Temperature Environment

Generally speaking, the semiconductor components are more sensitive to the temperature than other mechanical parts. Various electrical characteristics are restricted by the working temperature. It is necessary to grasp a temperature characteristic beforehand and design with derating taken into account. Use of them beyond their operation assured temperature range may not only assure the electrical characteristics, but quicken deterioration of the PIOC-101, shortening its service life.

## ■ 8-2.2 Humidity Environment

Airtightness of the molded PIOC-101 is not perfect. Long-term use of the PIOC-101 in the high-humidity environment, therefore, may deteriorate or damage the semiconductor chips due to the moisture entering inside. Apply a damp-proof treatment to the PIOC-101 surface. The low-humidity environment could lead to damages resulting from discharge of static electricity. Use it within a humidity range of 40 to 60 % unless any special measure is taken.

## ■ 8-2.3 Corrosive Gas

Note that the PIOC-101 may react to a corrosive gas and deteriorate the characteristics. For example, a sulfide gas including sulfur such as rubber may be generated near the PIOC-101, corrode the lead pins or cause a chemical reaction between them, form foreign substances, thus resulting in a leak.

## ■ 8-2.4 Radiation/Cosmic Rays

The PIOC-101 is not designed resistant to radiation or cosmic rays. In the spacecraft devices or the environment where radiation is generated, it is necessary to consider a shield designed to prevent them.

## ■ 8-2.5 Strong Electric Field/Magnetic Field

If the PIOC-101 is exposed to a strong electric field, polarization of plastic materials or inside IC chips may cause abnormal phenomena such as an impedance change, increased leak current. It is necessary to have an electric field/magnetic field shield. Particularly, the AC magnetic field environment requires the magnetic shield because an electromotive force is generated.

## ■ 8-2.6 Vibrations/Shock/Stress

The plastic-sealed PIOC-101 has internal wires secured by resin, providing a structure relatively resistant to vibrations and shocks. In the actual apparatuses, however, vibrations, shock, or stress may be applied to soldered parts, resulting in snapping. Care should be taken when using it for the vibrative apparatuses.
Also, pay attention to stress, because if it is applied to a semiconductor chip via the package, there may be a resistance change inside the chip due to a piezoeffect. Strong vibrations, shock, or stress causes cracks to the package or chip.

## ■ 8-2.7 Dust/Oil

As with a corrosive gas, the PIOC-101 may have a chemical reaction to dust or oil. Use it in the environment which does not allow adhesion of dust, oil, etc. which may affect the characteristics of the PIOC-101.

## ■ 8-2.8 Fuming/Ignition

The PIOC-101 is not incombustible. If it is baked or burnt, it may fume or catch fire, producing a toxic gas. Do not use near a flame, heating element, or inflammable substance.

## ■ 8-2.9 Precautions for Designing

To achieve the system reliability required by the client, it is necessary to use the PIOC-101 in compliance with its maximum ratings and recommended operating conditions. It is also necessary to observe the working environmental conditions such as ambient temperature, transitional noise, surge, paying full attention to their effects on the reliability of the PIOC-101.

## ■ 8-2.10 Observance of Maximum Ratings

The maximum ratings are the specifications which must not be exceeded even instantaneously; even any one of them must not be exceeded. The maximum ratings include the voltage, current, storage temperature, and temperature of each lead pin, and so on.

If the voltage/current of each lead pin exceeds the maximum rating, the PIOC-101 is internally deteriorated due to an overvoltage/overcurrent. Considerable deterioration may melt the wiring or destroy the inside of the semiconductor chip due to heat generation in an internal circuit.

If the storage temperature or soldering temperature exceeds the rating, the different coefficients of thermal expansion of various materials constituting the PIOC-101 may reduce airtightness or cause exfoliation of bonded parts.

## ■ 8-2.11 Observance of Guaranteed Operating Range

The recommended operating conditions are to assure functioning of the PIOC-101.

## ■ 8-2.12 Treatment of Unused Input/Output Terminals

If the unused input pins of the PIOC-101 are left open, input may become unstable. For the output pins, do not connect them to the supply voltage(VCC) or other output terminals.

If the PIOC-101 is used with the unused input pins left open, it tends to pick up more noise, becoming unstable. It is necessary to pull them up to the power supply(VCC9 or connect to Ground(GND), depending on their functions.

## ■ 8-2.13 Latch-up

Because of its CMOS structure, the PIOC-101 may fall into the latch-up state which allows a high current(several hundreds of mA) to run between VCC and GND, leading to destruction.

Latch-up takes place when an input/output voltage exceeds the rating and a high current runs to an internal element, or when the voltage of the power pin(VCC) exceeds the rating and the internal element yields.

In this case, even if a non-rated voltage is applied only instantaneously, a high current could be held between VCC and GND, resulting in heat generation or fuming, if the PIOC-101 latches up once. Note the following points:

Do not bring the voltage level of the input/output pins higher than VCC or lower than GND. Consider the power-on timing as well.

Take care that abnormal noise will not be applied to the PIOC-101.

Fix the unused input pins to VCC or GND.

Do not short-circuit the output pins.

## ■ 8-2.14 Input/Output Protection

Never connect a wired theoretical configuration where the output pins have been mutually connected, because it short-circuits the output of the PIOC-101. Also, do not connect the output pins directly to VCC or GND.

## ■ 8-2.15 Interface

When connecting to the PIOC-101 a device whose input/output conditions differ from it, malfunctioning results if the respective levels of input VIL/VIH and output VOL/VOH are consistent.

## ■ 8-2.16 External Noise

If an input/output signal line to the PIOC-101 mounted onto the printed circuit board is long and noise or surge is applied to the PIOC-101 through external induction, an overcurrent(overvoltage) could trigger malfunctioning or destruction. To reduce the noise, lower a signal line impedance or insert a noise eliminating circuit to protect against surge.

## ■ 8-2.17 Other Precautions

When designing the system, take appropriate measures such as fail-safe according to the application of the system and give shipment assurance to the system, including aging treatment.
If the PIOC-101 is placed in a high electric field, a surface leak may be caused by charging up, leading to malfunctioning. When using it in the high electric field, consider a remedy such as shielding the package surface with a conductive shielding plate.
Take care that any conductive material(metallic pin, etc.) will not fall onto the pins of the mounted PIOC-101 from the outside and short-circuit it.
The PIOC-101 has not been developed or intended for the systems where its troubles or malfunctioning may directly threaten the human life or harm the human body(nuclear power control, aeronautical and spacecraft devices, traffic devices, combustion control, various safety devices, and so on).

When using the PIOC-101 for the above-mentioned systems, we will not be responsible for any resulting damages