

PPMC-2104AFP

Dual-Axis Programmable Stepper **Motion Control LSI**

Rev 1.2

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The following shows the revision history of the PPMC-2104AFP Programmable Stepper Motion Control LSI Manual.

If you have any questions on this manual, please inquire our office.

Revision History

Rev. 1.0 on November 13, 2000

Rev. 1.1 on November 28, 2000

Rev. 1.2 on December 11, 2000

PPMC-2104AFP

PROGRAMMABLE STEPPER MOTION CONTROL LSI

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1. SPECIFICATIONS AND FUNCTIONS

1.1 Overview

The PPMC-2104AFP is the "programmable stepper motion control LSI" developed to meet different needs coming up these days. Having inherited the basic concept of our PPMC-100 series, it has a dual-axis control function in one package. The instruction sets are almost compatible with the PPMC-104 and have simple and easy-to-use functions condensed in them.

The most important objective of the stepper motor controller is to ensure accurate positioning control through smooth acceleration/deceleration. To realize it, it must be able to set an acceleration/deceleration curve suitable for the load and freely control high-speed and accurate drive pulse output. The PPMC-2104AFP is the control LSI which can give a very effective solution to the above-mentioned objective.

As the PPMC-2104AFP allows smooth acceleration/deceleration through linear acceleration/deceleration control, it can provide high-speed and accurate positioning control. It can also control output of up to 38 kpps pulses or that of phase excitation signals of up to 27 kpps.

The PPMC-2104AFP is controlled by its built-in program. An advanced stepper motor is controlled by giving a simple instruction code and data from a host processor, allowing you to greatly reduce the load of the host processor.

1.2 Functional Specifications

Initial Setting Instruction

Initial setting (Setting of acceleration/deceleration)

Operational Instructions

Acceleration/deceleration

Constant-speed operation

Single-step operation

Constant-speed origin search (Constant speed operation to the reference point)

Continuous constant-speed operation to the limit)

Continuous high-speed operation (High-speed operation to the high-speed limit)

Immediate stop, decelerated stop

Internal Register Read Instructions

End status read

Control input signal read

Output signal read

Remaining pulses read

Error code read

Auxiliary Instructions

Excitation OFF

Auxiliary Input

Auxiliary Output

Switching frequency setting

Hold signal delay time

Pulse Output Frequencies

Maximum speed at P-OUT mode 1-axis operation : 38 kpps

Maximum speed at phase excitation mode 1-axis operation : 27 kpps

Maximum speed at P-OUT mode 2-axis operation : 19 kpps

Maximum speed at phase excitation mode 2-axis operation : 15 kpps

Acceleration/Deceleration Pulses

4 to 11,220 pulses

Maximum Output Pulses

± 16,777,216 pulses

Package

64-pin QFP

1.3 Concept and Performance of PPMC-2104

1.3.1 Pulse Rate and Motor Speed

The PPMC-2104 uses a numerical value called a pulse rate as the data to determine a stepper motor speed. **Formula 1-1** shows the relations between the pulse rate and motor speed.

$$\text{Speed} = \frac{\text{Tclock}}{\text{Rate} + 1} (\text{pps}) \quad \text{---- Formula 1-1}$$

Speed : Motor speed (pps; pulses/sec.)

Tclock : Tclock: Reference clock (Select 500 kHz, 125 kHz, or external clock)

Rate : Rate: Pulse rate

1.3.2 Acceleration/Deceleration System

Acceleration/deceleration control of the PPMC-2104 is determined by the data given from the host processor and employs a linear acceleration/deceleration system.

1.3.2.1 Linear Acceleration/Deceleration System

The relations between the pulse output speed and time at acceleration/deceleration in the linear acceleration/deceleration system becomes "linear" (linear equation).

$$V = V_0 + K \times t \quad \text{---- Formula 1-1}$$

V : Speed

t : Time

V_0, K : Constants

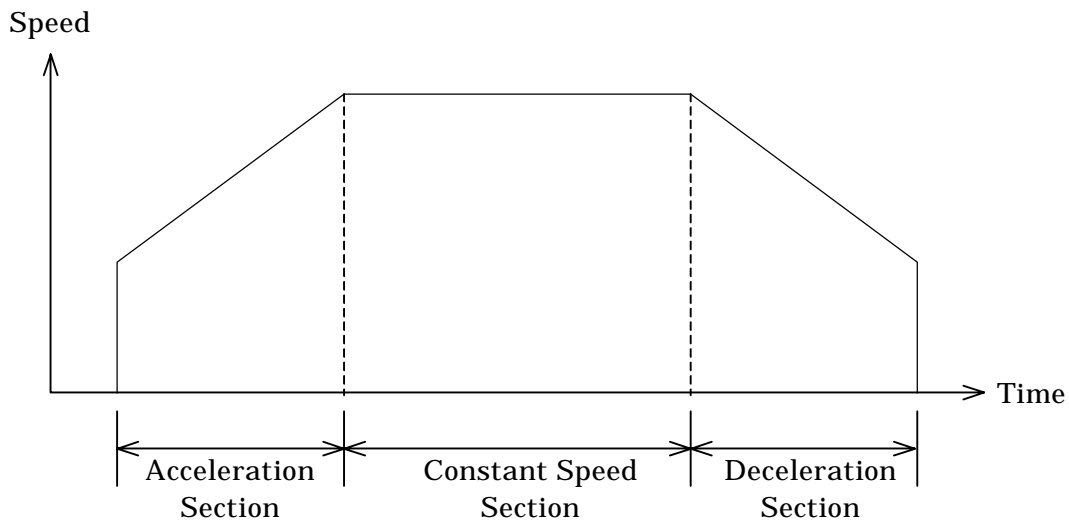


Fig. 1-1 Linear Acceleration System

1.4 Differences from PPMC-100 Series

The PPMC-2104 has inherited the basic concept of the conventional PPMC-100 series (PPMC-101C, -102A, -103A, and -104B) across the board. However, it does not have strict compatibility with the PPMC-100 series.

1.4.1 Two-axis Control

The PPMC-2104 has 2-axis pulse control and phase excitation output, and the respective axes have the functions almost equivalent to the PPMC-104. As internal control is provided through software, however, 2-axis operation can be only performed at half the speed of single axis operation.

1.4.2 Addition of Instructions

In order to ensure fine, detailed operation, the PPMC-2104 has an instruction added, which allows you to set the HOLD output delay time.

1.4.3 Addition of Error Codes

If there is any error in an instruction code or the data from the host processor, the PPMC-2104 will set an error flag in the status register to make it possible to read an error code with the "Instruction Error Read Instruction."

1.4.4 Addition of Status Register Bits

In order to allow the host processor to recognize the status of the PPMC-2104 more finely, some status register bits have been added.

2. TERMINAL SIGNAL FUNCTIONS

The PPMC-2104AFP is provided in a 64-pin QFP package. **Fig. 2-1** shows a terminal configuration for input and output signals, and Table 1 shows a terminal signals list, respectively. This chapter describes these signals in details.

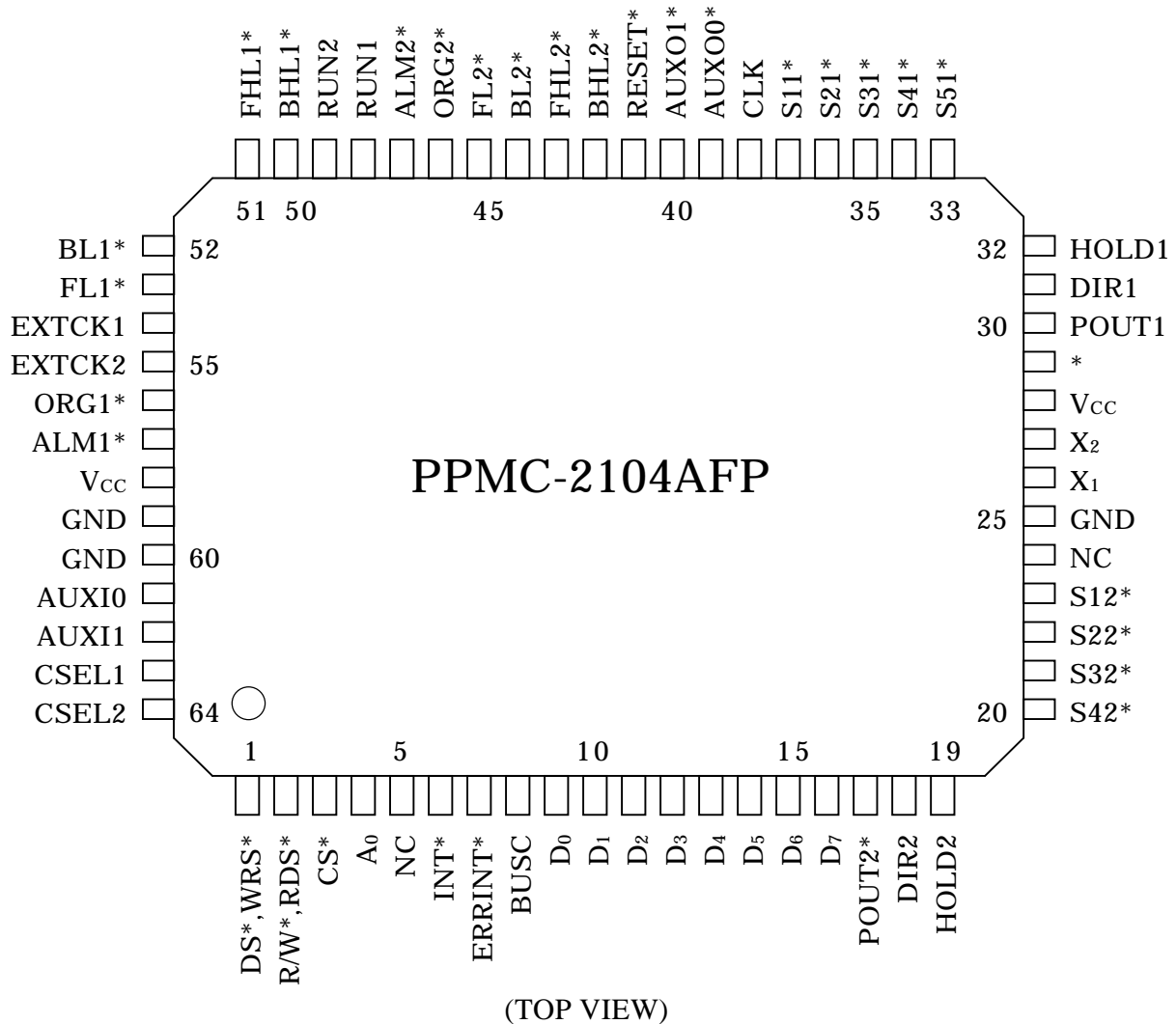


Fig. 2-1 PPMC-2104AFP Terminal Configuration

Table 1 Terminal Signals List

Terminal No. PPMC 2104AFP	Internal Pull-up	Signal Name	I/O	Function
1	⊙	DS*, WRS*	I	Data Strobe, Write Strobe
2	⊙	R/W*, RDS*	I	Read/Write, Read Strobe
3	⊙	CS*	I	Chip Select Input
4	⊙	A ₀	I	Address 0 Input
5	⊙	NC	NC	"L" at IBF = 0 or OBF = 1
6	⊙	INT*	O	Interrupt Output Signal
7	⊙	ERRINT*	I	Instruction Error Interrupt Enable Input
8	⊙	BUSC	I	Host Interface Select
9		D ₀	I/O	Host Interface Data Bus Bit-0
10		D ₁	I/O	Host Interface Data Bus Bit-1
11		D ₂	I/O	Host Interface Data Bus Bit-2
12		D ₃	I/O	Host Interface Data Bus Bit-3
13		D ₄	I/O	Host Interface Data Bus Bit-4
14		D ₅	I/O	Host Interface Data Bus Bit-5
15		D ₆	I/O	Host Interface Data Bus Bit-6
16		D ₇	I/O	Host Interface Data Bus Bit-7
17		POUT2*	O	#2 Pulse Output
18		DIR2	O	#2 Direction Signal Output
19		HOLD2	O	#2 HOLD Output
20		S52*	O	#2 Phase Excitation Output S5
21		S42*	O	#2 Phase Excitation Output S4
22		S32*	O	#2 Phase Excitation Output S3
23		S22*	O	#2 Phase Excitation Output S2
24		S12*	O	#2 Phase Excitation Output S1
25		NC	NC	
26		GND	I	Power Source 0 V
27		X ₁	I	Quartz Oscillator Terminal 1 (16 MHz)
28		X ₂	I	Quartz Oscillator Terminal 2 (16 MHz)
29		V _{CC}	I	Power Source 5 V
30		POUT1*	O	#1 Pulse Output
31		DIR1	O	#1 Direction Signal Output
32		HOLD1	O	#1 HOLD Output
33		S51*	O	#1 Phase Excitation Output S5
34		S41*	O	#1 Phase Excitation Output S4
35		S31*	O	#1 Phase Excitation Output S3
36		S21*	O	#1 Phase Excitation Output S2
37		S11*	O	#1 Phase Excitation Output S1
38		CLK	O	System Clock (4 MHz) Output
39		AUXO0*	O	Auxiliary Output Bit 0
40		AUXO1*	O	Auxiliary Output Bit 1

Terminal No. PPMC 2104AFP	Internal Pull-up	Signal Name	I/O	Function
41	⊙	RESET*	I	Reset Input
42		BHL2*	I	#2 CCW High Speed Limit Input
43		FHL2*	I	#2 CW High Speed Limit Input
44		BL2*	I	#2 CCW Limit Input
45		FL2*	I	#2 CW Limit Input
46		ORG2*	I	#2 Origin Input
47		ALM2*	I	#2 Alarm Input
48		RUN1	I	#1 Start Enable Input
49		RUN2	I	#2 Start Enable Input
50	⊙	BHL1*	I	#1 CCW High Speed Limit Input
51	⊙	FHL1*	I	#1 CW High Speed Limit Input
52	⊙	BL1*	I	#1 CCW Limit Input
53	⊙	FL1*	I	#1 CW Limit Input
54	⊙	EXTCK1	I	#1 External Clock Input
55	⊙	EXTCK2	I	#2 External Clock Input
56	⊙	ORG1*	I	#1 Origin Input
57	⊙	ALM1*	I	#1 Alarm Input
58		V _{CC}	I	Power Source 5 V
59		GND	I	Power Source 0 V
60		GND	I	Power Source 0 V
61		AUXI0	I	Auxiliary Input Bit 0
62		AUXI1	I	Auxiliary Input Bit 1
63		CSEL1	I	#1 Internal Clock Select; "H" = 500 kHz, "L" = 125 kHz
64		CSEL2	I	#2 Internal Clock Select; "H" = 500 kHz, "L" = 125 kHz

"*" suffixed to the signal name denotes negative logic.

"#" denotes the motor shaft number.

O = Output

I = Input

NC = OPEN

Pull up or pull down the unused input terminals with 10 K Ω resistors. The terminals marked with "⊙" in the InterⓈ Pull-up column are pulled up (about 3.2 k Ω) inside the CPU.

2.1 System Hardware Related Signals

2.1.1 RESET* (Reset)

This signal is to reset the PPMC-2104 to the initial state. Generally, connect it to the reset signal of the system. After rising from the "L" level, an instruction from the host processor issues and activates an initial setting or operational instruction. The reset signal requires that the supply voltage be within the operating range of the PPMC-2104, and that the "L" level be held at least for 2 μ s or more after the oscillations of system clock input have been stabilized.

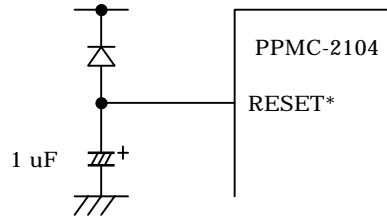


Fig. 2-1 Connection Example of Power-on Reset Circuit

2.1.2 X₁, X₂ (Quartz Oscillator)

The X₁ and X₂ terminals are the system clock input terminals for the PPMC-2104. Generally, connect 16 MHz quartz oscillators as shown in the left figure in Fig. 2-1. You can also connect a 2-phase external clock as shown in the right figure in Fig. 2-1.

The input frequency for X₁ and X₂ ranges from 1 to 16 MHz clock, and the PPMC-2104 operating speed is proportional to this clock. The time and other data prescribed hereinafter are based on this reference clock. The time, speed, and other data are based on the reference clock of 16 MHz, unless otherwise specified.

When activating multiple PPMC-2104s with a single system clock oscillation circuit, design the circuit, seeing Fig. 2-2. Observe the precautions mentioned on Page 2-5.

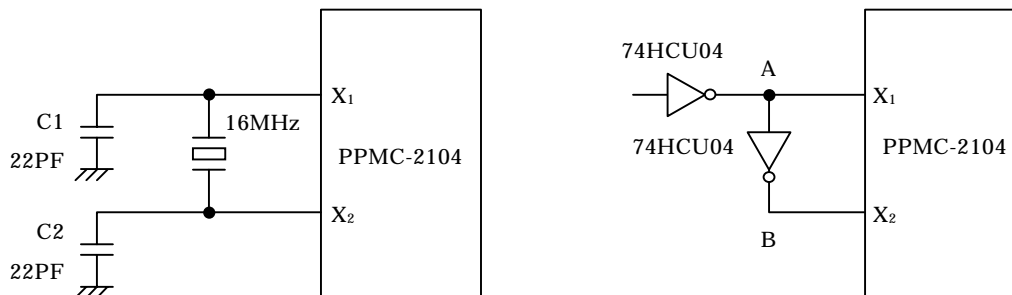


Fig. 2-1 Connection Example of System Clock Input

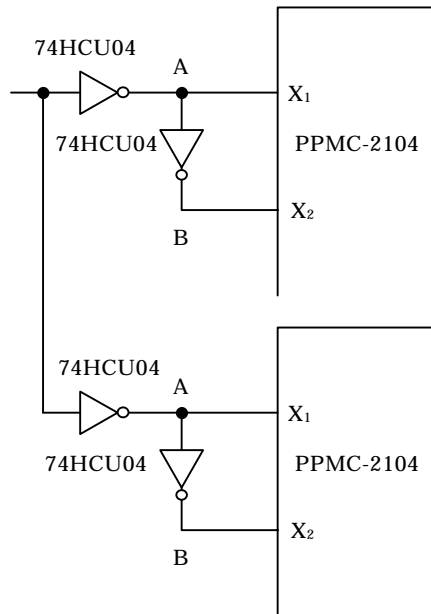


Fig. 2-2 Connection Example for Using Multiple PPMC-2104s

Cautions

(1) Quartz oscillator

The oscillation frequency is determined by the load capacity and external capacities, C1 and C2, of the quartz frequency. The equivalent resistance and external capacities of the quartz frequency has a great effect on stable start and continuation of oscillations. See the recommended values in **Table 2**.

Table 2 Equivalent Series Resistance by Oscillation Frequency

Frequency	Equivalent Series Resistance (Max.)	Frequency	Equivalent Series Resistance (Max.)
1MHz	600 Ω	12MHz	35 Ω
4MHz	100 Ω	16MHz	35 Ω
10MHz	35 Ω		

(2) 2-phase external clock signal input method

When using the 2-phase external clock signal shown in **Fig. 2-1** (right figure) or **Fig. 2-2**, satisfy the following conditions at Points A and B.

Condition-1: Duty ratio at Point A = $50 \pm 5\%$ (@ $V_{cc}/2$)

Condition-2: CL = 50 pF (max.) at Points A and B

2.2 Host Interface Signals

These signals are to connect the PPMC-2104 to the bus of the host processor. They include the signals to access the registers of the PPMC-2104 and interrupt signals.

2.2.1 CS* (Chip Select)

This is a select signal to the PPMC-2104. Connect an address signal whose higher bits have been decoded. The PPMC-2104 can be accessed when this CS* is at the "L" level.

(See 3.1 Host Interface Registers)

2.2.2 A₀ (Register Select)

When reading/writing from the host processor to the registers of the PPMC-2104, this signal is used to select each register. Generally, connect the LSB of an address signal.

(See 3.1 Host Interface Registers)

2.2.3 D₇~D₀ (Data Bus)

This is a bidirectional 8-bit bus used to exchange the data between the host processor and PPMC-2104.

2.2.4 BUSC (Slave Bus Interface Select)

This signal is to select an interface format between the host processor and PPMC-2104. This signal allows you to easily connect to either R/W type CPU or RD* or WR* separate type CPU. For the relations between the BUSC signal and interface format, see 2.2.5, 2.2.6, and Table 3.

Table 3 Relations between BUSC and Host Processor Bus Interface

BUSC Signal	Host Processor Bus Interface	Control Signals Used	
H	R/W* type	Data strobe signal (DS* signal)	Read/write signal (R/W* signal)
L	RD*, WR* separate type	Write strobe signal (WRS* signal)	Read strobe signal (RDS* signal)

2.2.5 DS*, WRS* (Data Strobe, Write Strobe)

If the BUSC signal is at "H", this is used as a data strobe signal for the R/W* type CPU. If the BUSC signal is at "L", it is used as a write strobe signal for the RD* or WR* separate type CPU. See Table 3.

2.2.6 R/W*, RDS* (Read/Write, Read Strobe)

If the BUSC signal is at "H", this is used as a read/write signal for the R/W* type CPU. If the BUSC signal is at "L", it is used as a read strobe signal for the RD* or WR* separate type CPU. See Table 3.

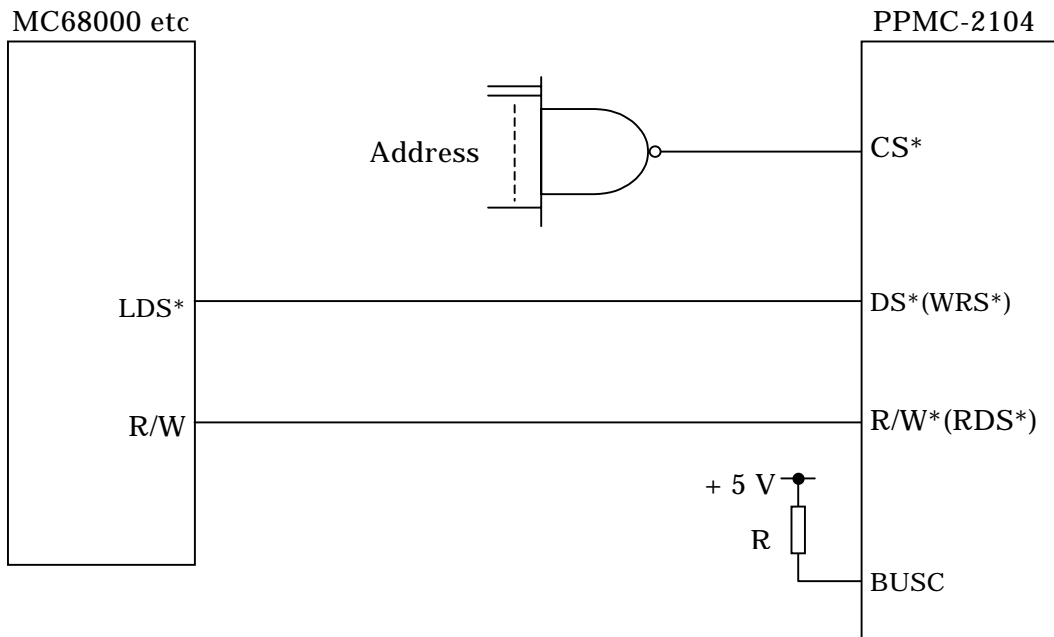


Fig. 2-1 R/W* Type Signal Connection Example

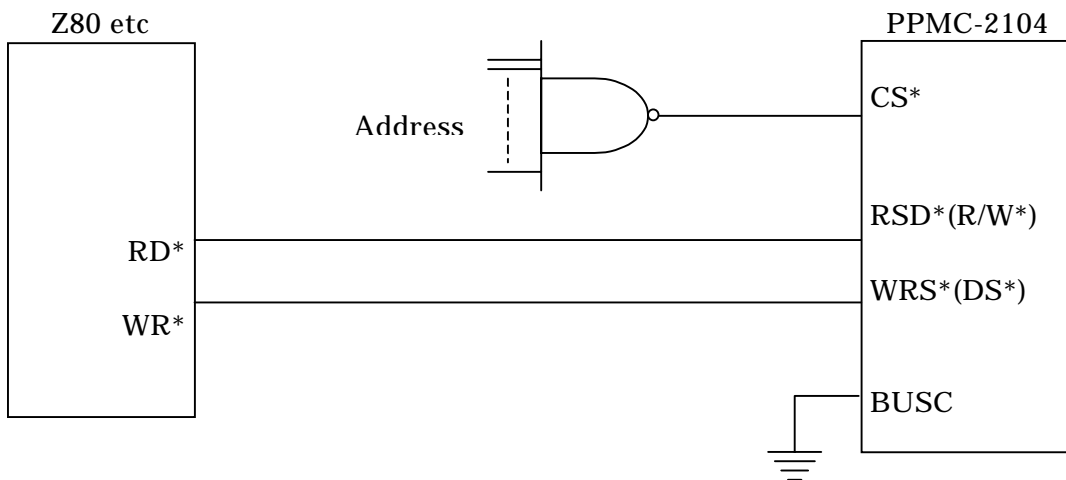


Fig. 2-2 RD* or WR* Separate Type Signal Connection Example

2.2.7 INT* (Interrupt Signal)

This signal is an interrupt signal to the host processor and output in the following cases:

- (1) When instruction code end interrupt control to the PPMC-2104 has been enabled and PPMC-2104 pulse output has ended.
- (2) When the instruction or parameter received from the host processor by the PPMC-2104 is illegal.

The PPMC-2104 has 2 axes worth of control functions. Consequently, there are 4 interrupt causes. The INT* signal is generally at the "H" level and changed to the "L" level when the condition in (1) or (2) above is met. As the INT* signal terminal is not of open collector, install an open collector type buffer as shown in **Fig. 2-1**, when connecting multiple interrupts.

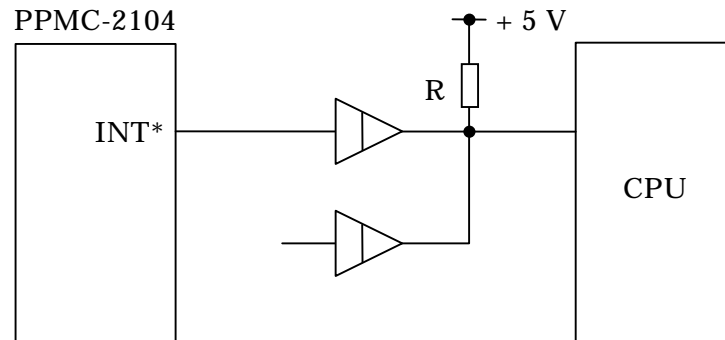


Fig. 2-1 PPMC-2104 Interrupt Output Signal Connection Example

If a pulse output end interrupt is generated, the INT* signal is cleared and changed from the "L" to the "H" level by issuing the **"End Status Code Read Instruction."** If an instruction error interrupt is generated, the INT* signal is cleared and changed from the "L" to the "H" level by issuing the **"Error Code Read Instruction."** Even if INT* is set to "H" by these read instructions, it will be changed to "L" again after 5 μ s, if other interrupt cause remains.

The INT* signal is not cleared by issuing the **"End Status Code Read Instruction"** when the instruction error interrupt is generated, or issuing the **"Error Code Read Instruction"** when the pulse output end interrupt is generated. To clear it, therefore, it is necessary to check Bit-7 (instruction error interrupt status) of the status register and issue the status read instruction with respect to the interrupt generation factor.

2.2.8 ERRINT* (Error Interrupt Enable Signal)

This signal is to determine whether to enable the above-mentioned interrupt at error. An error interrupt is output when it is at "L". If this signal is at "H", an interrupt signal does not change because an error flag is set, even if there is an instruction error.

2.3 Motor Control Signals

The motor control signals are to be connected to a motor driver, etc. There are two sets of these signals independently for the axes. This manual describes the set of signals for one axis. In the signals table, the respective signal names are suffixed with 1 or 2 for distinction.

2.3.1 DIR (Operating Direction Signal)

This is an output signal to indicate the operating direction. It is set to the "L" level when outputting the clockwise pulses, and to the "H" level when outputting the counterclockwise ones. It is used in combination with the POUT* signal in **2.3.2**.

2.3.2 POUT* (Pulse Sequence Output Signal)

This is a pulse sequence signal to be output by the PPMC-2104. Its waveform is output in the form of negative square wave, and the POUT* width is 5 μ s at minimum regardless of the speed. Use it in combination with the DIR signal in 2.3.1.

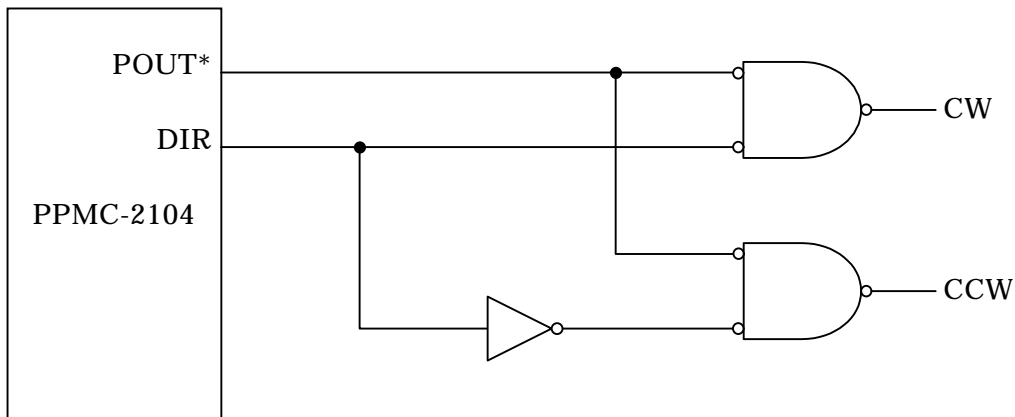


Fig. 2-1 DIR or POUT* Signal Connection Example

2.3.3 HOLD (Motor Hold Signal)

This signal indicates that the motor is stopping. This HOLD signal is set to "L" when pulse output starts, and set to "H" after a lapse of time set with the hold output delay time instruction after pulse output has stopped. If the PPMC-2104 receives the next operational instruction, this signal is set to "L". It is used for reducing the supply voltage of the motor when stopping it or when externally monitoring the motor.

The time from the end of pulse output to output of the HOLD signal can be changed by the hold signal delay time setting instruction. If this instruction is not given, however, its default is 3.2 mS.

2.3.4 S1*-S5* (Phase Excitation Output)

The S1*-S5* signals are phase excitation signals for the unipolar motors; a 3-phase motor uses S1* to S3, 4-phase motor S1* to S4*, and 5-phase motor S1* to S5*, respectively. **Fig. 2-1** shows the respective output patterns.

The output logic level is of negative logic. **Fig. 2-2** shows a circuit example of the driver at that time. The PPMC-2104 holds the output level for S1* to S5* at "H" until the initial setting instruction is given.

(Example) In Case of 3-phase Motor, 2-phase Excitation

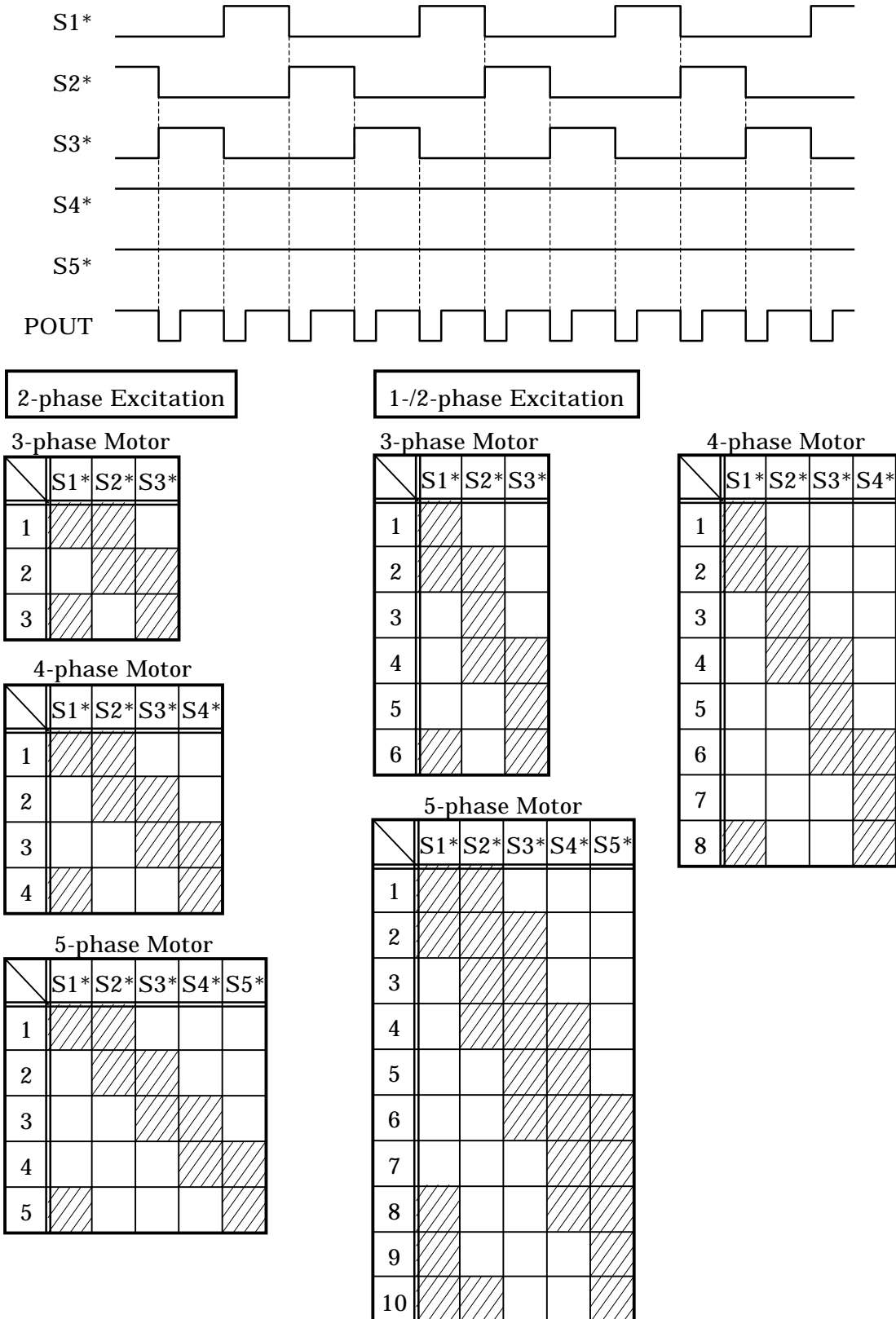


Fig. 2-1 Phase Excitation Signal Output Patterns

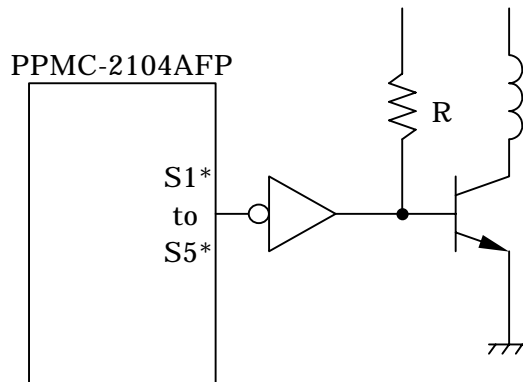


Fig. 2-2 Drive Circuit Example

2.3.5 EXTCLK (External Clock Input)

This is a timing signal which serves as the reference for speed control of the stepper motor in the external clock mode. There are the limitations to the external clock signal, which are shown in Fig. 2-1. When using the external clock, it is necessary to specify it with the initial setting instruction. When not using it, pull it up or down with a resistor of about 10 kΩ.

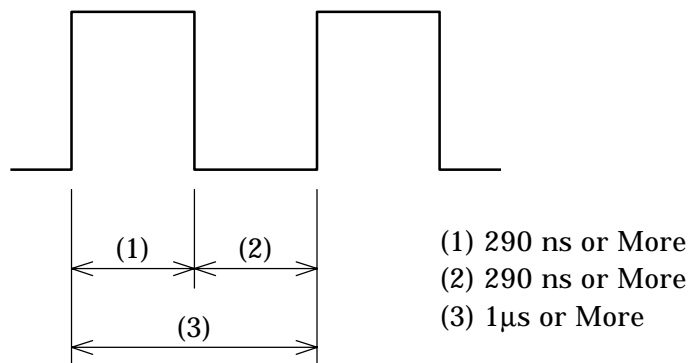


Fig. 2-1 External Clock Input Signal

2.3.6 CSEL (Standard Clock Select Signal)

This signal is to select an operation clock when an internal clock has been set as a clock source with the initial setting instruction. The reference clock is 500 kHz at "H" and 125 kHz at "L".

2.4 Limit and Alarm Input Signals

These are a group of input signals from the limits and motor driver. As with the motor control signals, there is one set of them for each axis. In the signals table, the respective signal names are suffixed with the axis number 1 or 2. This manual describes only one of two sets. All of these signals are of negative logic input.

2.4.1 ORG (Origin (Reference Point) Input Signal)

The PPMC-2104 checks this signal only in case of the "Constant Speed Origin Search" instruction. If this signal is detected, the PPMC-2104 stops pulse output immediately. It normally serves as the origin for various positioning controls.

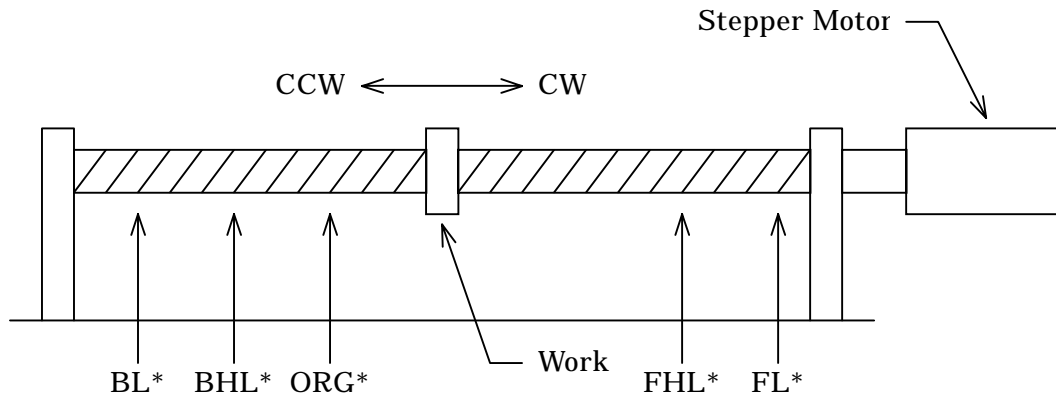
To make this signal detected, it is necessary to hold it at the "L" level during 1 pulse or longer. That is, when the pulse rate is slow, it is necessary to input the proportionally longer ORG signal.

2.4.2 FL*, BL*, FHL*, BHL* (Limit Input Signals)

FL* is the limit to be set at the operation limit point in the positive direction (CW), and BL* at that in the negative direction, respectively. The PPMC-2104 stops with any operational instruction, if it detects these limits in the respective operating directions. Then, if the operational instruction to the same direction is input, no pulses are output.

FHL* is a deceleration limit in the positive direction (CW), and BHL* in the negative direction (CCW), respectively. If the PPMC-2104 detects these limits during acceleration or high-speed operation, it will be decelerated to stop.

Fig. 2-1 shows the physical positional relations of the above-mentioned limit signals.



- ⊙ The FL* and BL* limit switches are to be set at the operation limit points of the work.
- ⊙ The FHL* and BHL* limit switches are to be set inside the FL* and BL* positions by the number of acceleration/deceleration pulses or more.
- ⊙ The ORG* limit switch is to be set at the origin of positioning control.

Fig. 2-1 Limit Switch Positional Relations

2.4.3 ALM* (Alarm Input Signal)

Connect to the alarm output of the motor driver. If the PPMC-2104 receives this signal while outputting the pulses, it stops output.

2.4.4 RUN (Pulse Output Start Signal)

An operational instruction is given from the host processor to the PPMC-2104 and this signal is checked prior to outputting the pulses. If it is at "H", the PPMC-2104 starts outputting the pulses. If this signal is at "L", the PPMC-2104 waits to output them until the signal is switched to "H". At this time, the busy flag for the relevant axis of the status register is set.

It is used when simultaneously starting multiple PPMC-2104s. When not using the function of the RUN signal, be sure to pull up to +5 V.

If there is a factor which immediately stops pulse output triggered by the limit input and alarm input signals, while waiting to output the pulses, pulse output hold is cancelled, overriding the issued operational instruction. (Pulse output hold is not cancelled by inputting the ORG signal at constant speed origin search.)

If the deceleration limit is generated while holding acceleration/deceleration or continuous high-speed operation, the PPMC-2104 is decelerated to stop after cancelling RUN.

2.5 Auxiliary Input and Output Signals

The auxiliary input/output signals are the general purpose 2-bit input/output ports which are not directly related to the stepper motor control functions.

2.5.1 AUXIO-AUXI1 (Auxiliary Input Signals, Bit-0 to Bit-1)

AUXIO to AUXI1 are the 2-bit input ports provided by the PPMC-2104 and available as the auxiliary input ports for the system. It takes about 40 μ sec to read the input port status.

2.5.2 AUXO0*-AUXO1* (Auxiliary Output Signals; Bit-0 to Bit-1)

AUXO0 to AUXO1 are the 2-bit output ports provided by the PPMC-2104 and available as the auxiliary output ports for the system. It takes about 40 μ sec for the output port status to change. These output ports have been set to the "H" level immediately after resetting.

2.6 Calculating the Limit/Alarm Input Signal Width

The PPMC-2104 detects the limits and alarms through polling. This polling cycle greatly differs depending on the operating conditions and it is necessary to input the limit and alarm signals greater than the polling cycle. The following describes how to calculate the maximum polling cycle.

The polling cycle calculated is the maximum value, and as a higher pulse rate is output, an error increases.

Table 4 Command Processing Time T_i

No	Processing	Processing Time T_i
1	Initial setting	71000
2	Immediate stop	400
3	Deceleration stop	32
4	Single step	103
5	Acceleration/deceleration (Triangular)	340
6	Acceleration/deceleration (Trapezoidal)	110
7	Constant speed operation	29
8	Continuous constant speed operation	32
9	Continuous high speed operation	118
10	Constant speed origin search operation	32
11	End status read	40
12	Control input signal read	36
13	Output signal read	32
14	Remaining pulses read	37
15	Error code read	43
16	Excitation OFF	32
17	Auxiliary output	26
18	Auxiliary input	31
19	Switching frequency setting	36
20	Hold signal delay time setting	32

Table 5 Interrupt Processing Times T_1 and T_2

No	Description	Processing Times T_1, T_2
1	Acceleration/deceleration	25
2	Phase excitation acceleration/deceleration	35
3	Constant speed operation	38
4	Origin search in operation	40

Unit of processing time: μ s

Note) As the processing time of initial setting is long, make initial setting before operation when operating the two axes.

Formula:

Interrupt count I_n

Operation speed V_{oth}

Interrupt polling cycle $P_i (= 35 + T_i)$

Regular polling cycle $P_n (= 35)$

Processing time T_i

1-axis processing time T_1

2-axis processing time T_2

Maximum limit detection time T_{max}

$I_n = P_i / ((1/V_{oth}) - (T_1 + T_2))$

$T_{max} = I_n \times (T_1 + T_2) + P_n + T_i$

Note) For I_n , raise a decimal to a unit.

Table 4 shows the processing time of a single command, and **Table 5** the interrupt processing time for pulse output.

First, obtain the processing time from **Table 4** or **Table 5**. When obtaining the processing time from **Table 5**, calculate the cycle out of a pulse rate to be output, subtract the processing time from that cycle, and calculate the polling cycle by polling with the remaining time. The polling cycle is 35 μ sec when nothing is operating.

Example: Polling Cycle during Initial Setting

Table 4 shows $T_i = 71000$. As no pulses are being output, calculate the maximum limit detection time, assuming $I_n = 0$.

$$T_{max} = 71000 + 35 = 71035 \text{ (}\mu\text{sec)}$$

Example: When a Single Axis Is Running at Constant Speed of 10 kpps

Table 5 shows that the processing time for constant speed operation is 38 (μ s). As no commands are being processed at this time, assume $T_i = 0$. As only one axis is operating at constant speed, T_1 and T_2 are 38 and 0, respectively. As it is operating at 10 kpps, each pulse is output at $V_{oth} = 100 \mu$ s (1/10 kpps).

$$I_n = (35 + 0) / (100 - (38 + 0)) = 0.56$$

Count the value I_n as 1 by raising fractions below the decimal point to a whole number. Calculate the maximum limit detection time from this interrupt count I_n .

$$T_{max} = 1 \times (38 + 0) + 35 + 0 = 73 \text{ (}\mu\text{sec)}$$

Example: When Both Axes Are Operating at Constant Speed of 10 kpps

Table 5 shows that the processing time for constant speed operation is 38 (μ s). As no commands are being processed at this time, assume $T_i = 0$. As both axes are operating at constant speed, both T_1 and T_2 are 38. As they are operating at 10 kpps, each pulse is output at $V_{oth} = 100 \mu$ s (1/10 kpps).

$$I_n = (35 + 0) / (100 - (38 + 38)) = 1.45$$

Count the value I_n as 2 by raising fractions below the decimal point to a whole number. Calculate the maximum limit detection time from this interrupt count I_n .

$$T_{max} = 2 \times (38 + 38) + 35 + 0 = 187 \text{ (}\mu\text{sec)}$$

Example: When One Axis Is Operating at Constant Speed of 20 kpps and the Other Axis Is Being Initially Set

Tables 4 and **5** show $T_i = 71000$ and $T_1 = 38$ ($T_2 = 0$ because of one-axis operation). As $V_{oth} = 50 \mu$ s (1/20 kpps), the interrupt count I_n is calculated as follows:

$$I_n = (35 + 71000) / (50 - (38 + 0)) = 5919.58$$

Count the value I_n as 5920 by raising fractions below the decimal point to a whole number. Calculate the maximum limit detection time from this interrupt count I_n .

$$T_{max} = 5920 \times (38 + 0) + 35 + 71000 = 295995 \text{ (approx. 296 msec)}$$

2.7 Flow Chart Example of Interrupt Servicing Routine

The PPMC-2104 has only one INT signal for reporting the interrupts. To distinguish multiple factors with this one signal, see the below-mentioned flow chart.

As a caution, it is necessary to remember the issued instructions at two points in the flow chart; "Instruction Issued Axes" and "Operational Instruction Issued Axes." At "Instruction Issued Axes," determine to which station the previous command has been issued. At "Operational Instruction Issued Axes," determine to which axis number the operational instruction has been issued.

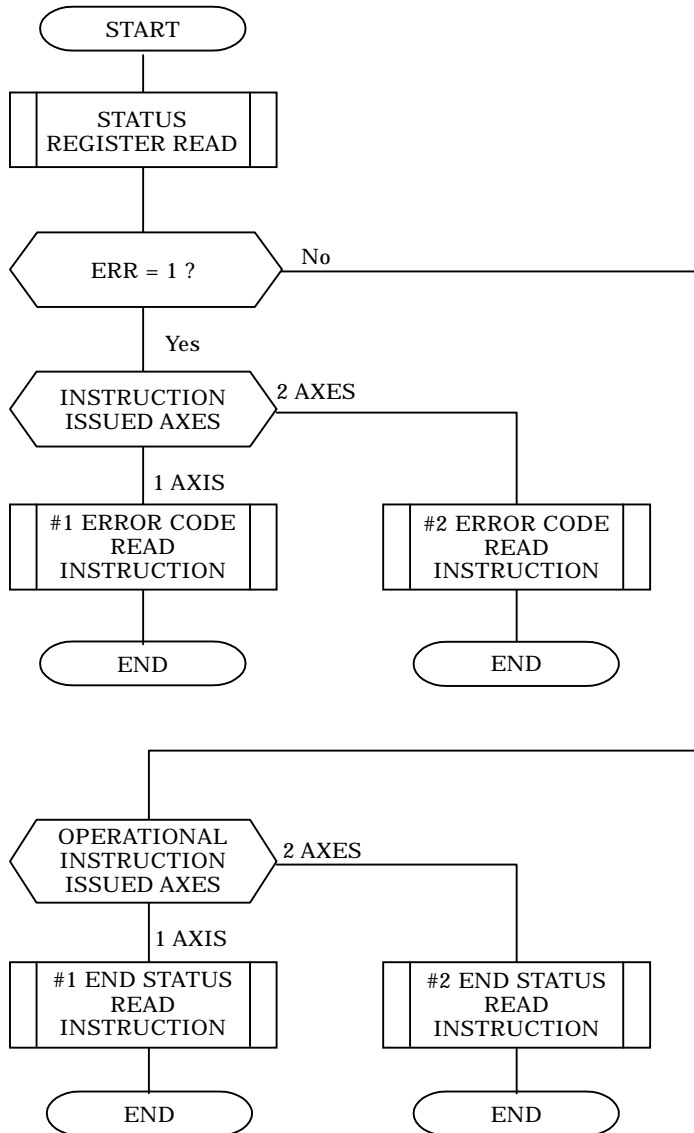


Fig. 2-1 Interrupt Servicing Routine Flow Chart

3. PPMC-2104 CONTROL INSTRUCTIONS

The PPMC-2104 operates in accordance with the instruction codes and data given from the host processor. They are largely divided into the following four kinds of instruction groups.

(1) Initial setting instruction

This instruction is to set an acceleration/deceleration speed range. It is necessary to give it initially to the PPMC-2104 after power-on or resetting.

(2) Operational instructions

These instructions are to operate the stepper motor. There are eight kinds of them, including two kinds of stop instructions. Some instructions are executed only with an instruction code and others require some bytes of data.

(3) Internal register read instructions

The PPMC-2104 has five kinds of internal register read instructions. They can read the end status, control input signal, output signal, remaining pulses, and error code.

(4) Auxiliary instructions

There are five kinds of instructions; excitation OFF, auxiliary output, auxiliary input, switching frequency setting, and hold signal delay time setting.

Table 6 lists the instructions for the PPMC-2104.

Table 6 List of Instructions

Instruction		Command/Data	Function	
Initial Setting	1	00ASCEMM	S: Sets switching C: Sets the clock E: Excitation method MM: Motor type	
	2	Start-up pulse rate	Start-up pulse rate in acceleration/deceleration (Normally sets the self-start frequency)	
	3	High-speed pulse rate	High-speed pulse rate in acceleration/deceleration	
	4	Acceleration/deceleration pulses (L)	Sets the pulses reaching from the start-up speed to high-speed operation.	
	5	Acceleration/deceleration pulses (H)		
Operational Instructions	Immediate stop	1 01A0 0000	Stops pulse output immediately.	
	Deceleration stop	1 01A0 0001	Decelerates to the start-up speed to stop.	
	Single step	1 01AI D010	Outputs one pulse in the specified direction.	
	Acceleration/deceleration	1	P1AI D011	Performs acceleration/deceleration from the start-up speed to the high speed.
		2	Operation pulses (L)	
		3	Operation pulses (M)	Specify the number of operation pulses in 3 bytes. Input sequentially from the lowest byte.
		4	Operation pulses (H)	
	Constant speed operation	1	01AI D100	Performs constant speed operation at the specified constant speed pulse rate.
		2	Constant speed pulse rate	
		3	Operation pulses (L)	Specify the pulse rate in 1 byte. Specify the number of operation pulses in 3 bytes. Input sequentially from the lowest byte.
		4	Operation pulses (M)	
		5	Operation pulses (H)	

Instruction		Command/Data		Function
Operational Instructions	Continuous constant speed operation	1	01AI D101	Performs constant speed operation as far as the limit at the specified speed. Specify the pulse rate in 1 byte.
		2	Constant speed pulse rate	
	Continuous high-speed operation	1	P1AI D110	Decelerates to stop by detecting the high-speed limit in acceleration/deceleration.
	Constant-speed origin search	1	01AI D111	Performs constant speed operation as far as the reference point at the specified speed. Specify the pulse rate in 1 byte.
2		Constant speed pulse rate		
Internal Register Read Instructions	End status read	1	10A0 0000	Reads the end status register.
	Control input signal read	1	10A0 0001	Reads the control input (limit, etc.) status.
	Output signal read	1	10A0 0010	Reads the phase excitation output signal status, etc.
	Remaining pulses read	1	10A0 0011	Reads the remaining pulses in case of emergency stop, etc.
	Error code read	1	10A0 0110	Reads the error register.
Auxiliary Instructions	Excitation OFF	1	11A0 0000	Turns off the phase excitation signal.
	Auxiliary output	1	11DD 0001	Changes the auxiliary output port status. (DD denotes data)
	Auxiliary input	1	1100 0010	Reads the auxiliary input port status.
	Switching frequency setting	1	10A0 0100	Sets the phase excitation signal switching time at stop.
		2	Phase excitation signal ON time	
		3	Phase excitation signal OFF time	
Hold signal delay time setting	1	10A0 0101	Sets the time from the end of pulse output to HOLD signal output.	
	2	Hold delay time		

A : Axis number (0: 1 axis, 1: 2 axes)
I : Bit to specify the pulse output end interrupt
D : Bit to specify the operating direction
P : Bit to specify pulse output

3.1 Host Interface Registers

As the registers to input/output the instructions and data, the PPMC-2104 has the following four kinds of registers. **Table 4** shows the conditions to access them.

Table 7 Host Interface Registers

Register	CS	A ₀	RD	WR	Read/Write
Disable	H	×	×	×	Disable
Data register	L	L	L	H	Read
Status register	L	H	L	H	Read
Data register	L	L	H	L	Write
Command register	L	H	H	L	Write

3.1.1 Status Register (At Read)

The status register is the read only register. It shows the internal status of the PPMC-2104 and can be read any time. Fig. 3-1 shows a bit configuration.

<<Status Register>>

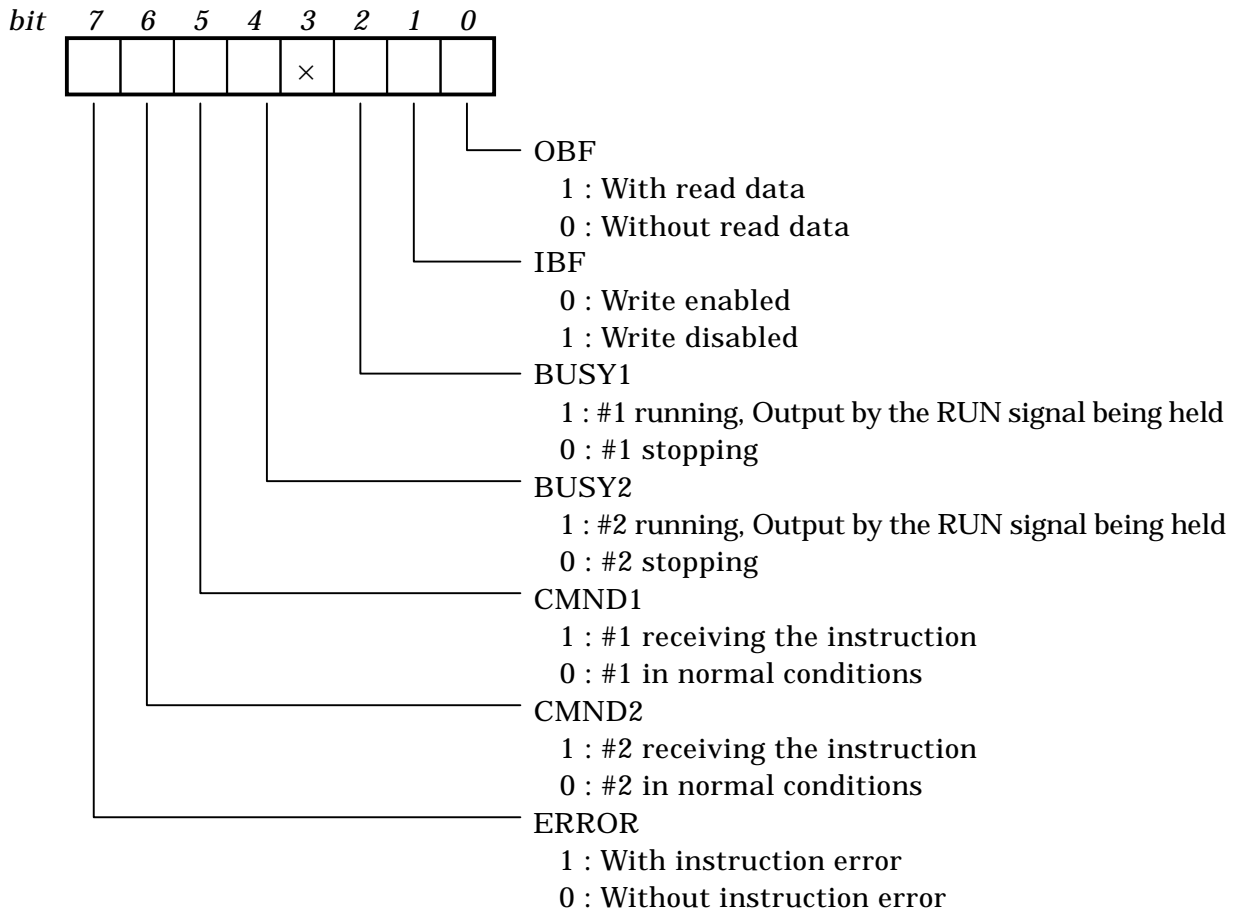


Fig. 3-1 Bit Configuration of Status Register

(1) OBF (Output Buffer Full Flag)

This bit is to check whether the data can be read from the PPMC-2104. When reading the data, make sure that OBF has been set to "1". If set to "0", the data will be invalid.

When it is "1", do not issue a command. Be sure to read the data prior to issuing the next command.

(2) IBF (Input Buffer Full Flag)

This bit is to check whether the instruction or data can be written into the PPMC-2104. When the IBF bit is "1", you cannot write new data.

When writing the instruction or data, make sure that the IBF bit has been set to "0". If you write the instruction or data when IBF is "1", operation will not be guaranteed.

(3) BUSY1 (Motor 1 Busy), BUSY2 (Motor 2 Busy)

The BUSY1 bit is set to "1" when the No. 1 axis of the PPMC-2104 is outputting the pulses (while the motor is rotating or the RUN signal is standing by). When the BUSY1 bit is "1", the No. 1 axis accepts only the stop instruction, auxiliary input/output instruction, and error code read instruction; it does not accept the other instructions. When writing the instruction, check the BUSY1 bit as well as IBF bit.

The BUSY2 bit shows the status corresponding to the No. 2 axis.

(4) CMND1 (Command 1), CMND2 (Command 2)

The CMND1 bit indicates that the PPMC-2104 is executing the host instruction for the No. 1 axis, and the CMND2 bit shows the status corresponding to the No. 2 axis.

When these bits are set, it indicates that the PPMC-2104 is requesting for the data corresponding to the instruction codes given to the relevant axes.

(5) ERROR (Error Flag)

This bit indicates whether or not there is an error in the instruction code or data given from the host processor. By checking this bit after issuing each instruction to complete internal processing, you can check whether or not there is an error in the issued instruction code or data.

When this bit is "0", no error exists, and when "1", it exists. To learn the detail of the error, issue the **"Error Code Read Instruction"** to read the error number. **Table 8** lists the error numbers and their descriptions. The ERROR bit is set to "0" by issuing the error code read instruction.

Table 8 Instruction Error Codes

Error Code	Description
0	No error
1	Undefined instruction
2	Has not received the instruction code
3	Has received the instruction while waiting for the data
4	Initial setting not completed
5	Busy and cannot execute
6	Cannot execute while stopping. (Deceleration and stop instructions)
7	Cannot operate on the limit, ORG, or ALM
8	Has received the deceleration instruction during deceleration or constant speed operation, or while holding RUN.
9	Abnormal rate data or too few acceleration/deceleration pulses
10	Abnormal acceleration/deceleration pulses
11	Switching parameter less than 40h
12	Rate error 1 (Cannot operate at the specified rate because single-axis operation exceeds the limit rate) *
13	Rate error 2 (Cannot operate at the specified rate because the other axis is operating) *

* When Error 2 takes place, issue the error code read instruction to the No. 1 axis.

* Errors 12 and 13 take place only when the internal clock has been selected as the clock source by the initial setting instruction.

3.1.2 Data Register (At Read)

This register is to read the internal register data. When reading the data, check the OBF bit of the status register. For details, see "3.5 Internal Register Read Instructions."

3.1.3 Command Register (At Write)

This register is to write the instruction codes for the initial setting instruction, operational instructions, status read instructions, auxiliary instruction, and so on. When writing, make sure that the IBF bit of the status register is "0".

3.1.4 Data Register (At Write)

This register is to write the data (pulse rate, operation pulses, etc.) required for each instruction, after writing each instruction code. When writing, make sure that the IBF bit of the status register is "0". The writing order is described in the explanation of each instruction. Once this data is written, the PPMC-2104 performs necessary processing internally and operates in accordance with the instruction/data.

3.2 Internal States

The PPMC-2104 has six different internal states; "Initial," "Normal," "Accelerated/Decelerated," "Decelerated," "Constant Speed," and "RUN Wait." See Table 9.

Table 9 List of Internal States

State	Description
Initial	Until the initial setting instruction is successfully completed after turning on the power or resetting. BUSY bit = "0"
Normal	No pulses are being output or pulse output by the RUN signal is not held. BUSY bit = "0"
Accelerated/Decelerated	Pulse output is started by the acceleration/deceleration instruction or continuous high speed instruction, and the PPMC-2104 is being accelerated or operating at high speed. BUSY bit = "1"
Decelerated	Pulse output is started by the acceleration/deceleration instruction or continuous high speed instruction, and the PPMC-2104 is being decelerated. BUSY bit = "1"
Constant Speed	Pulses are being output by the constant speed, continuous constant speed operation, or constant speed origin search instruction. BUSY bit = "1"
RUN Wait	Pulse output is being held by the RUN signal. BUSY bit = "1"

Table 10 shows acceptance/rejection of each instruction depending on the internal state.

Table 10 Acceptance/Rejection of Instructions Depending on Internal State

Instruction	States					
	Initial	Normal	Accelerated/Decelerated	Decelerated	Constant Speed	RUN Wait
Initial setting	○	○	×	×	×	×
Immediate stop	×	×	○	○	○	○
Deceleration stop	×	×	○	×	×	×
Single step	×	○	×	×	×	×
Acceleration/deceleration	×	○	×	×	×	×
Constant speed operation	×	○	×	×	×	×
Continuous constant speed operation	×	○	×	×	×	×
Continuous high speed operation	×	○	×	×	×	×
Constant speed origin search	×	○	×	×	×	×
End status read	○	○	×	×	×	×
Control input signal read	○	○	×	×	×	×
Output signal read	○	○	×	×	×	×
Remaining pulses read	○	○	×	×	×	×
Error code read	○	○	○	○	○	○
Excitation OFF	○	○	×	×	×	×
Auxiliary output	○	○	○	○	○	○
Auxiliary input	○	○	○	○	○	○
Switching frequency setting	○	○	×	×	×	×
Hold signal delay time setting	○	○	×	×	×	×

3.3 Initial Setting Instruction

After power-on reset, the host processor needs to issue the initial setting instruction to the PPMC-2104 at first. With the initial setting instruction code, select the axis number, switching at stop, clock source, excitation method, and motor type. When issuing the initial setting instruction, set three kinds of data such as the start-up pulse rate, high-speed pulse rate, and acceleration/deceleration pulses, following the instruction code.

<<Initial Setting Instruction/Data>>

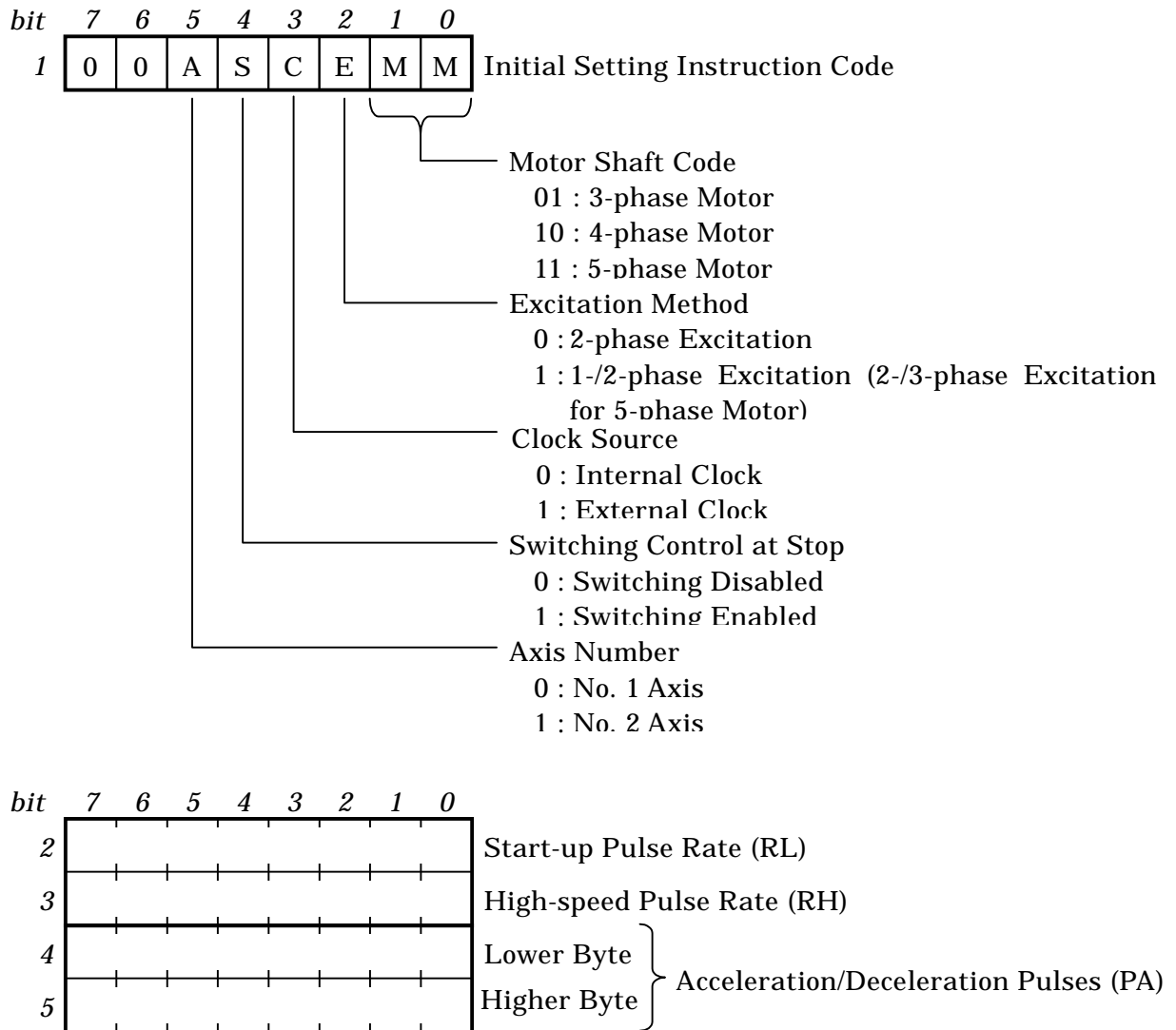


Fig. 3-1 Initial Setting Instruction Code and Data

For the initial setting instruction, write the instruction code and data in the numerical order indicated on the left in Fig. 3-1. Fig. 3-3 shows this sequence in the form of flow chart.

The start-up pulse rate and high-speed pulse rate are 8-bit data, and the number of acceleration/deceleration pulses is 16-bit data; divide the 16-bit data into the higher and lower bytes, and give the lower one first.

The pulse rate ranges from 1h to FFh. The number of acceleration/deceleration ranges from 4h to 2BD4h. RL should be greater than RH by 2 or more. (That is, $(RL + 2) \geq RH$)

Prior to issuing the initial setting instruction again, issue the excitation OFF instruction. Otherwise, only acceleration/deceleration (RL, RH, PA) will be changed.

Formulas 3-1 and **3-2** show the relations between the pulse output speed and start-up pulse rate, and high-speed pulse rate. **Fig. 3-2** shows the relations between each data and acceleration/deceleration.

$$SH = \frac{T_{clock}}{(RH+1)} \text{ ---- Formula 3-1}$$

SH : High speed (pps)
 RH : High-speed pulse rate
 Tclock : Reference clock

$$SL = \frac{T_{clock}}{(RL+1)} \text{ ---- Formula 3-2}$$

SL : Start-up speed (pps)
 RL : Start-up pulse rate
 Tclock : Reference clock

* Reference clock --- Clock (500 k/125 k) selected with the CSEL signal when the internal clock is selected as the clock source, or the clock input to the EXTCK signal when the external clock is selected as the clock source.

From the formulas above, **Table 11** shows the relations between the reference clock and pulse output speed ranges.

Table 11 Reference Clock and Pulse Output Speed Ranges

Reference Clock (Tclock)	Pulse Output Speed Range with Single Axis	Pulse Output Speed Range with Both Axes
500kHz	1.95kppS to 38kppS	1.95kppS to 19kppS
125kHz	488ppS to 38kppS	488ppS to 19kppS

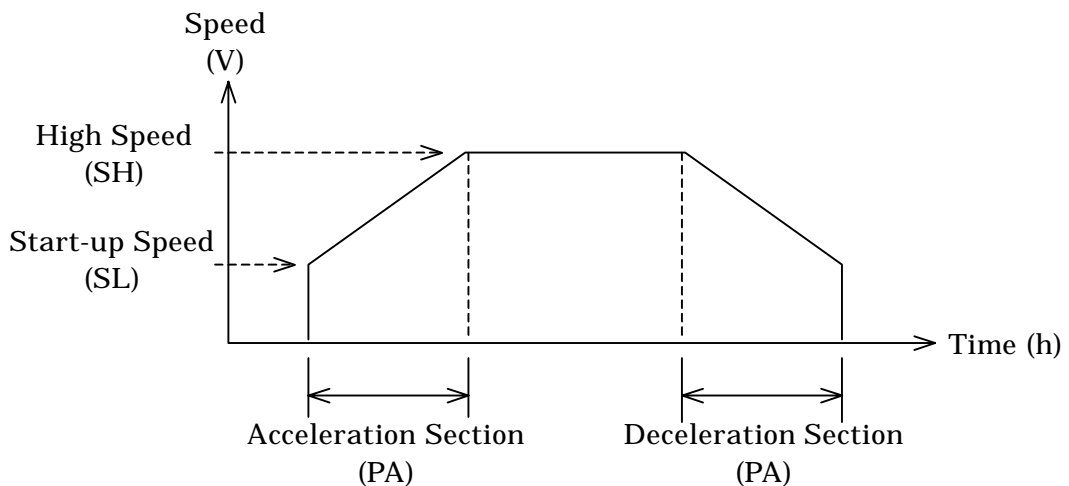


Fig. 3-2 Relations between Initial Setting Instruction Data and Acceleration/Deceleration

The number of acceleration/deceleration pulses means that of operation pulses to be output in the acceleration or deceleration section. It tells you how many pulses are required to reach the high speed after start-up (pulse output start) or to stop from the deceleration start point.

Fig. 3-3 shows a flow chart for issuing the initial setting instruction.

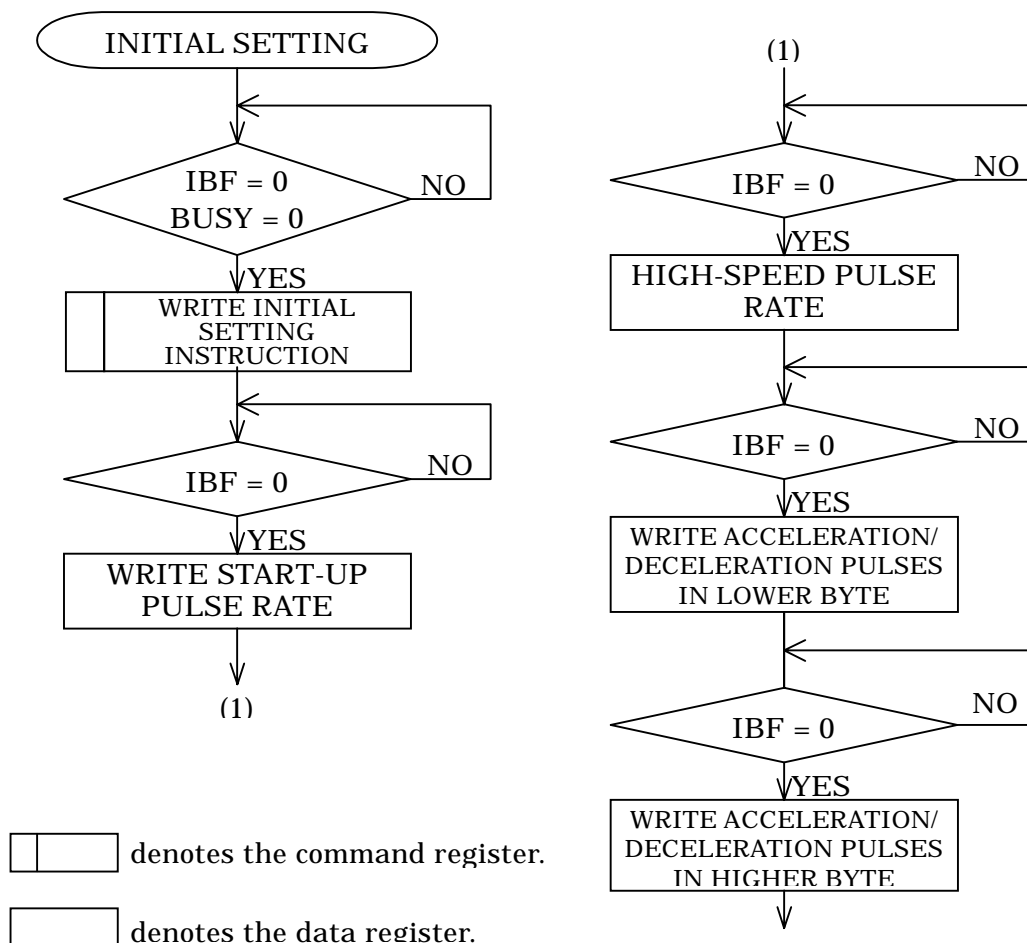


Fig. 3-3 Initial Setting Instruction Flow Chart

Supplementary Explanation: Pulse Output Rate Setting and Switching Control

The available pulse output rate range differs depending on selection of the clock source with the initial setting instruction. See **Table 12**.

Table 12 Available Pulse Rate Ranges

Clock Source		P-OUT		Phase Excitation			
				Constant Speed Origin Search		Other than Constant Speed Origin Search	
		1-axis Operation	2-axis Operation	1-axis Operation	2-axis Operation	1-axis Operation	2-axis Operation
Internal	500k	Ch to FFh	19h to FFh	14h to FFh	25h to FFh	12h to FFh	23h to FFh
		38.46k to 1.95kppS	19.23k to 1.95kppS	23.8k to 1.95kppS	13.15k to 1.95kppS	26.31k to 1.95kppS	13.88k to 1.95kppS
	125k	3h to FFh	6h to FFh	5h to FFh	9h to FFh	4h to FFh	8h to FFh
		31.35k to 488ppS	17.85k to 488ppS	20.83k to 488ppS	12.5k to 488ppS	25k to 488ppS	13.88k to 488ppS
External		0h to FFh					

When setting the clock source outside, you must pay attention to the pulse output speed. If one axis is operated at 38 kpps or higher and two axes at 19 kpps or higher at P-OUT mode, or one axis at 27 kpps or higher and two axes at 15 kpps or higher at phase excitation mode, the PPMC-2104 will be incapable of responding. If it falls into such conditions, you have to reset it. There are no other ways to revert.

The axis under switching control is considered operating even during pulse output suspension, and therefore, both axes are supposed to be operating. At this time, the operation limit of the other axis is 19 kpps or higher at P-OUT mode and 15 kpps or higher at phase excitation mode.

3.4 Operational Instructions

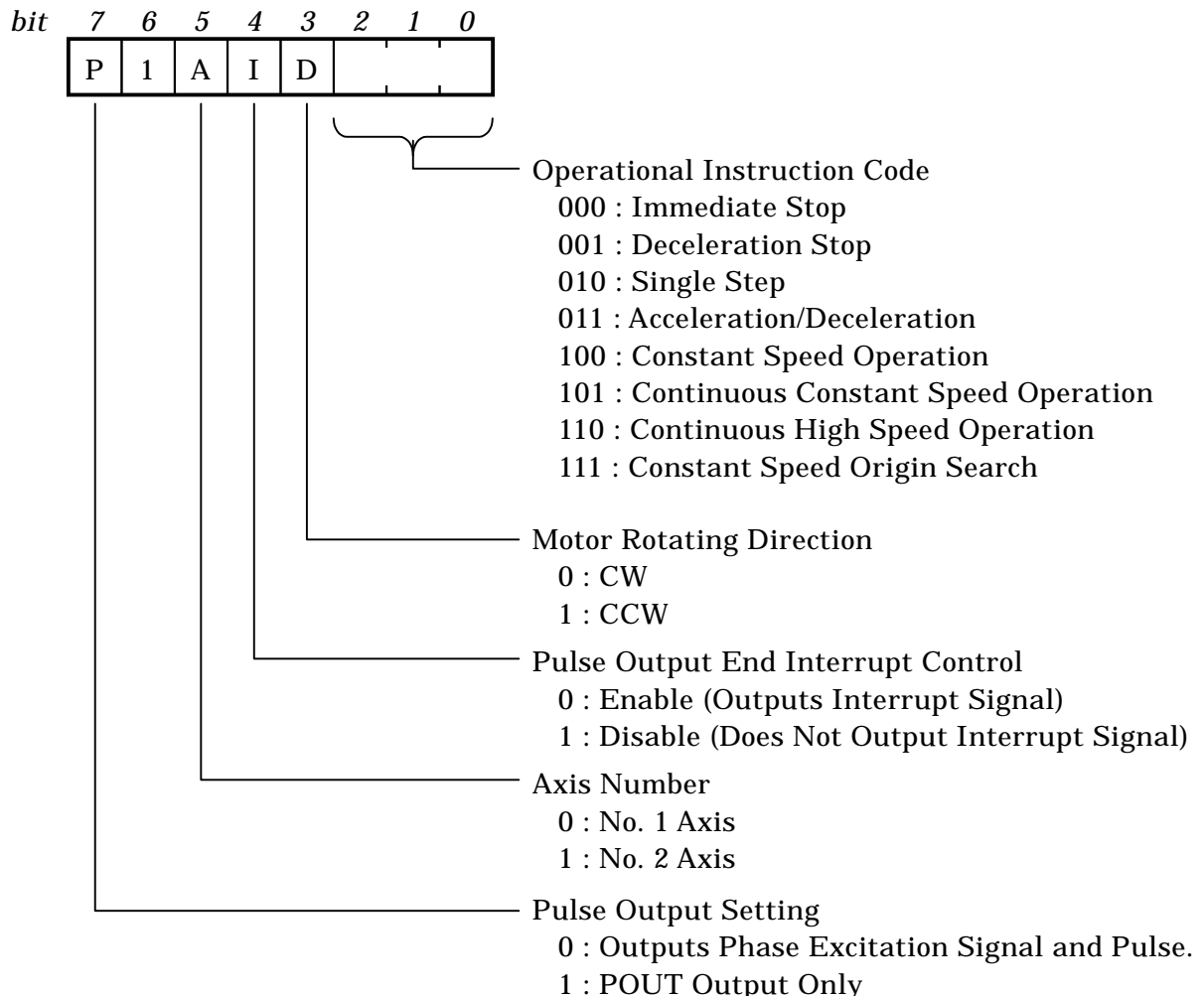


Fig. 3-1 Bit Configuration of Operational Instruction Code

3.4.1 Immediate Stop

If the PPMC-2104 receives this instruction during acceleration/deceleration or constant speed operation, it will immediately stop outputting the pulses. If the stepper motor is running in the higher speed range than the self-start range at execution of this instruction is executed, it may go out of adjustment due to inertia of motor load.

If the INT bit of the given operational instruction is "0", the interrupt signal (INT*) will be output after pulse output is completed.

This instruction has no data, but only the instruction code, and is meaningful only during pulse output (BUSY = 1). Check the IBF bit of the status register, followed by the BUSY bit of the relevant axis, and then, write this instruction.

From starting to accept this instruction code until stopping pulse output, the PPMC-2104 cannot detect the control input signals such as limit signal, etc., even if they are input.

The RUN wait status can be cancelled by issuing the immediate stop instruction while waiting for RUN. The number of remaining pulses at this time is equal to the set value of the given operational instruction.

<<Immediate Stop Instruction>>

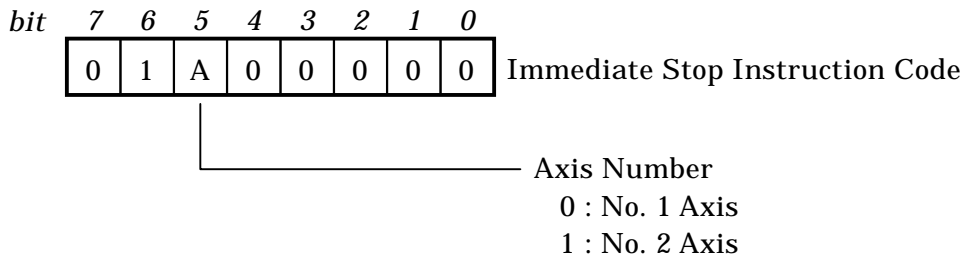
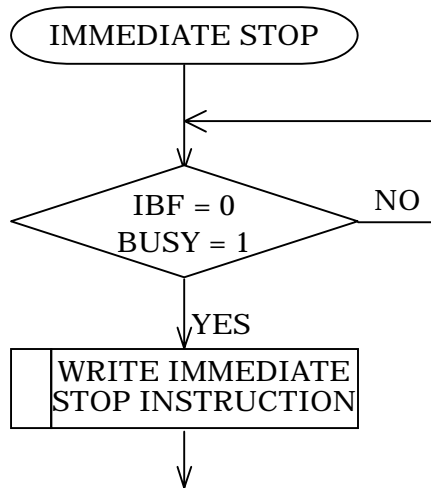


Fig. 3-1 Immediate Stop Instruction Code

Fig. 3-2 shows a flow chart for issuing the immediate stop instruction.



denotes the command register.

Fig. 3-2 Flow Chart for Immediate Stop Instruction

3.4.2 Decelerated Stop

Once this instruction is received, the PPMC-2104 immediately start deceleration and ends pulse output at start-up speed after deceleration. If the INT bit of the given operational instruction is "0", the interrupt signal (INT*) will be output after stopping. If the operating speed upon accepting this instruction is equal to the start-up speed specified at the time of initial setting instruction, the PPMC-2104 will stop immediately without deceleration.

This instruction has no data, but only the instruction code, and is meaningful only during pulse output (BUSY = 1). Check the IBF bit of the status register, followed by the BUSY bit of the relevant axis, and then, write this instruction.

From starting to accept this instruction code until starting deceleration, the PPMC-2104 cannot detect the control input signals such as limit signal, etc., even if they are input.

<<Deceleration Stop Instruction>>

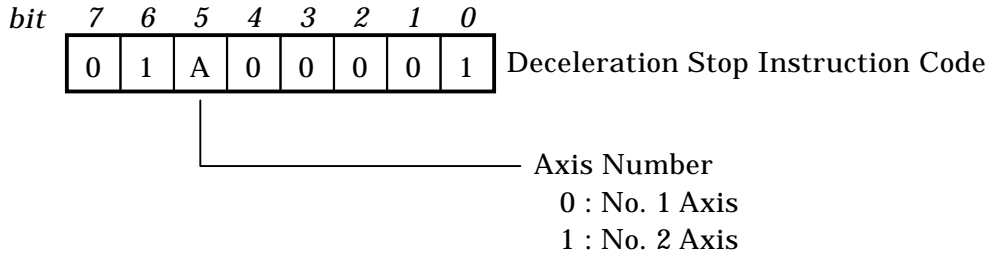
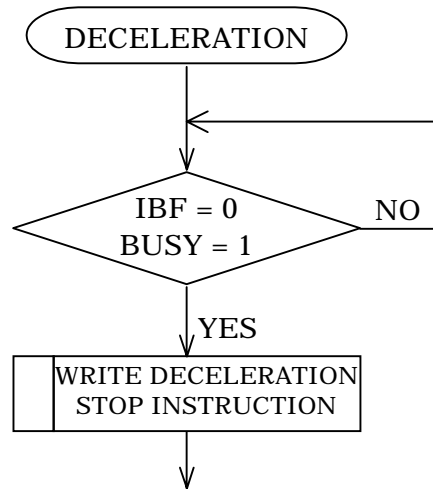


Fig. 3-1 Deceleration Stop Instruction Code

Fig. 3-2 shows a flow chart for issuing the deceleration stop instruction.



--	--

 denotes the command register.

Fig. 3-2 Flow Chart for Deceleration Stop Instruction

3.4.3 Single Step

This instruction from the host process is to move the PPMC-2104 pulse by pulse. It is used for the host processor to check the position by itself. This instruction has no data, but only the instruction code. Check the IBF bit of the status register, followed by the BUSY bit of the relevant axis, and then, write this instruction. As the single step operational instruction examines the RUN signal by starting pulse output, it waits for RUN.

<<Single Step Operational Instruction>>

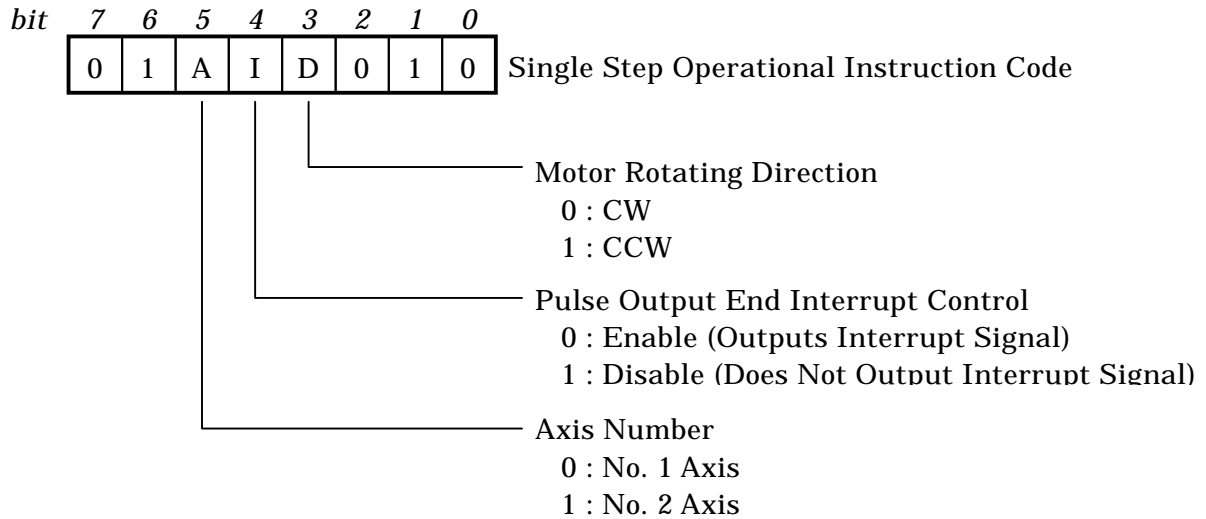


Fig. 3-1

Fig. 3-2 shows a flow chart for issuing the single step operational instruction.

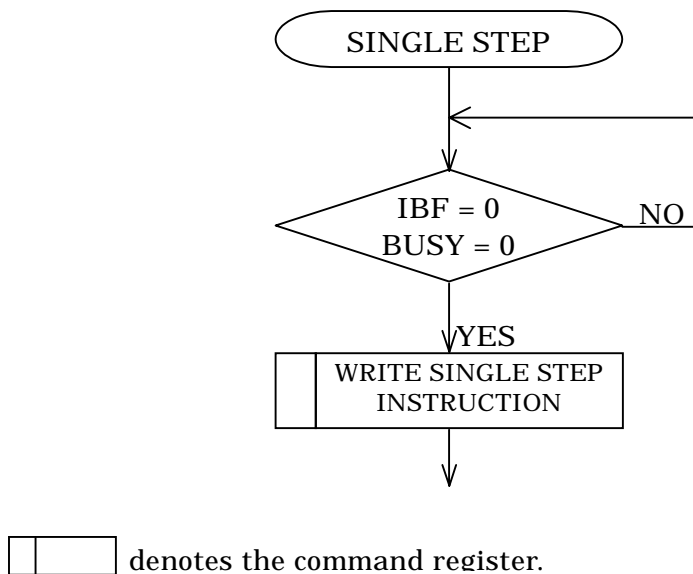


Fig. 3-2 Flow Chart for Single Step Operational Instruction

3.4.4 Acceleration/Deceleration

This instruction is to output pulses in accordance with acceleration/deceleration set with the initial setting instruction. Together with the instruction, it is necessary to specify the number of operation pulses in 3 bytes. Once this instruction is received, the PPMC-2104 starts outputting the pulses at the start-up speed specified at the time of the initial setting instruction and accelerates up to the high speed at the specified number of acceleration/deceleration pulses. Then, it operates at high speed, reaches the deceleration start point, and decelerates to the start-up speed at the number of acceleration/deceleration pulses to complete outputting the pulses. If you set the number of operation pulses smaller than twice the number of acceleration/deceleration pulses, the PPMC-2104 will start deceleration halfway acceleration, resulting in triangular drive.

If the INT bit is set to "0", the interrupt signal (INT*) will be output after completion of pulse output. When writing the instruction code of this instruction, check the IBF bit of the status register, followed by the BUSY bit of the relevant axis. When writing the number of operating pulses, check the IBF bit.

The number of operation pulses can be specified from 0h to FFFFFFFh. The number of pulses to be output is that of operation pulses + 1.

Pulse output can be stopped by the ALM signal, rotating direction limit signal, deceleration limit signal, immediate stop instruction, or deceleration stop instruction.

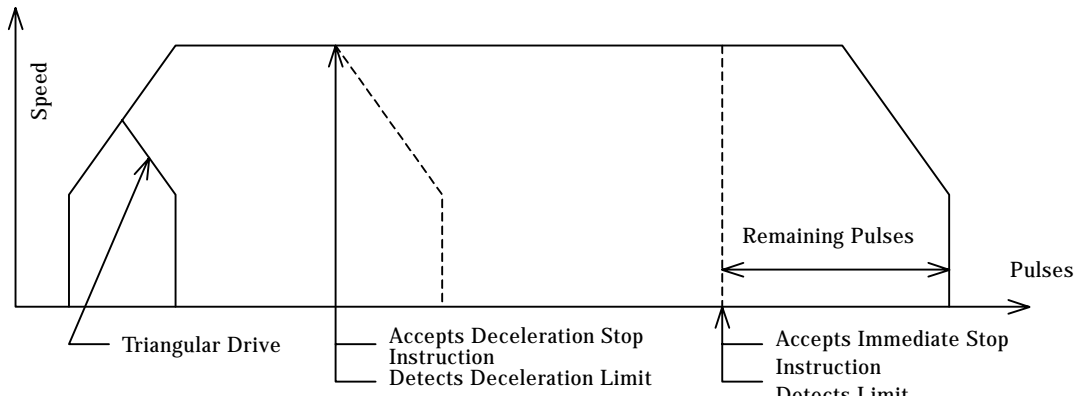


Fig. 3-1 Acceleration/Deceleration

<<Acceleration/Deceleration Instruction/Data>>

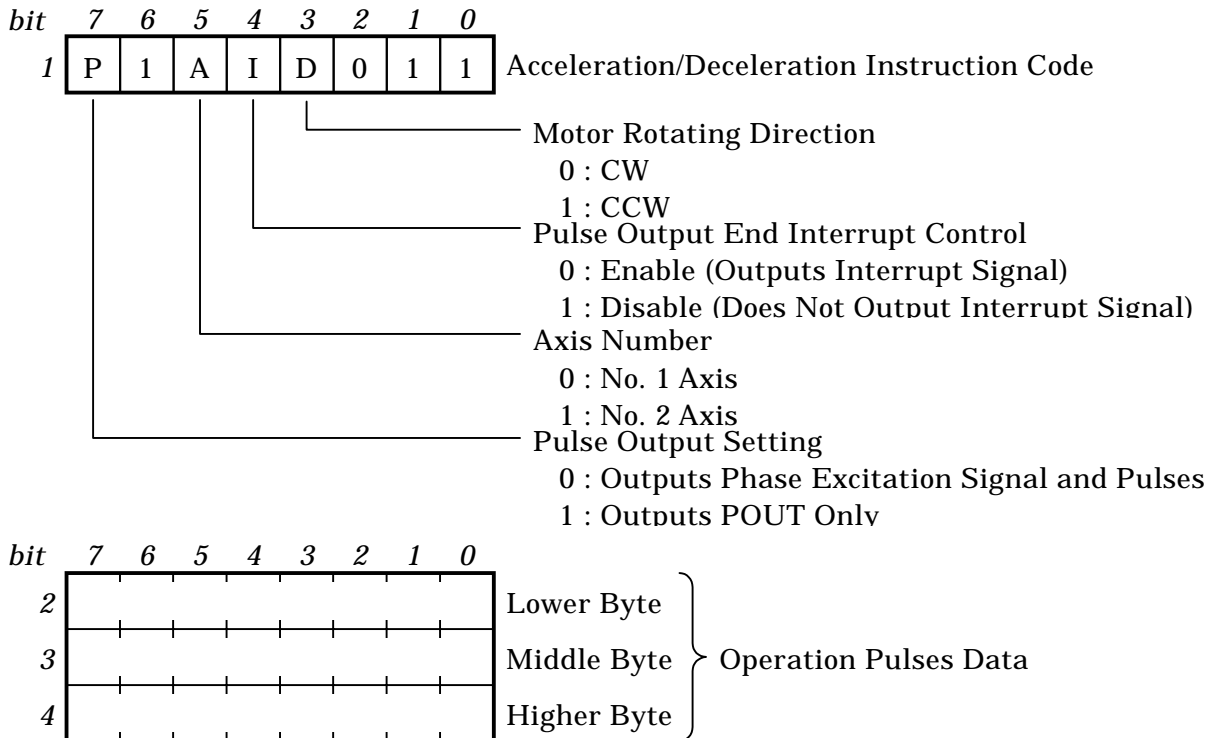


Fig. 3-2 Acceleration/Deceleration Instruction Code and Data

Fig. 3-3 shows a flow chart for issuing the acceleration/deceleration instruction.

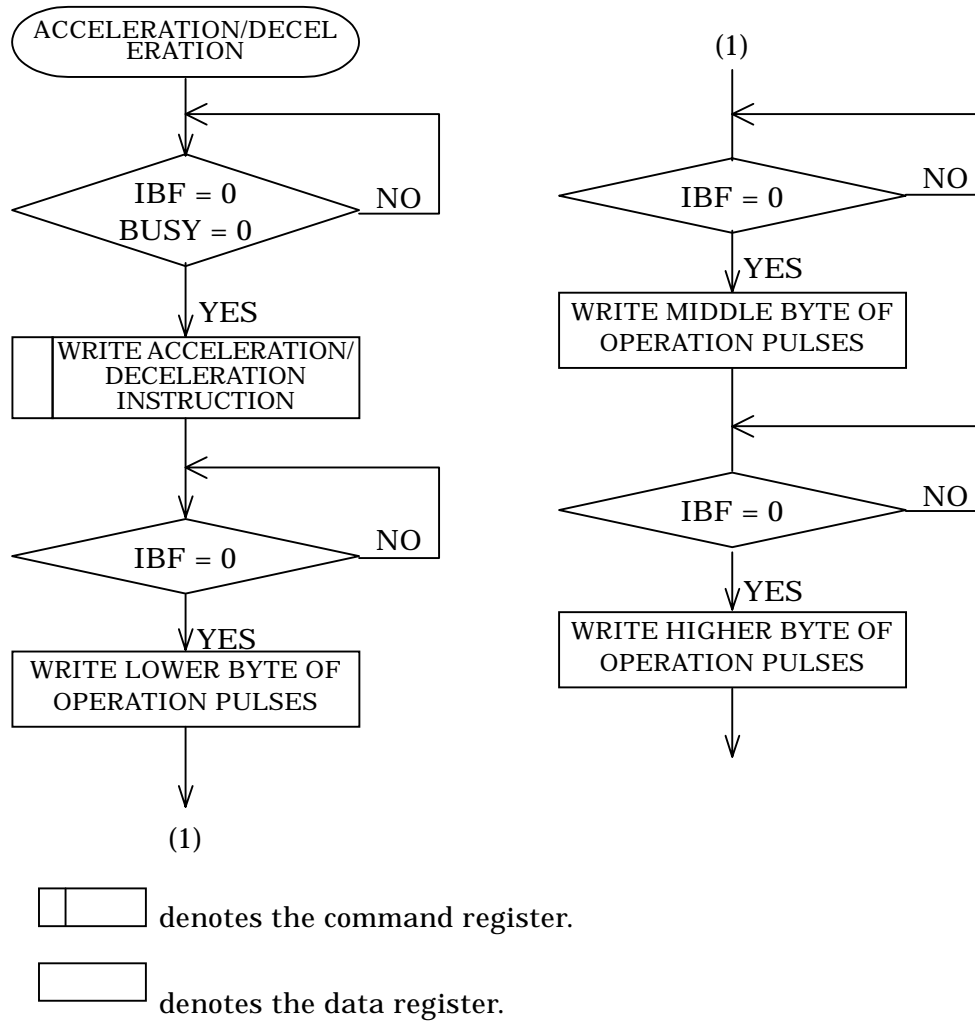


Fig. 3-3 Flow Chart for Acceleration/Deceleration Instruction

3.4.5 Constant Speed Operation

Pulse output is allowed only in the phase excitation mode.

This instruction is to output the number of pulses specified at the specified constant speed. It is necessary to specify 1-byte constant speed pulse rate and 3-byte operation pulses, following the instruction code.

If the INT bit is set to "0", the interrupt signal (INT*) will be output after completion of pulse output. When writing the instruction code of this instruction, check the IBF bit of the status register, followed by the BUSY bit of the relevant axis. The data should be written sequentially, checking the IBF bit.

The number of operation pulses can be specified within a range of 0h to FFFFFFFh. The number of pulses to be output is that of operation pulses + 1.

Pulse output can be stopped by the ALM signal, rotating direction limit signal, or immediate stop instruction.

The constant speed pulse rate can be specified within a range of 1h to FFh, but it is necessary to pay attention to the specified rate. For details, see Supplementary Explanation in **3.3 Initial Setting Instruction**.

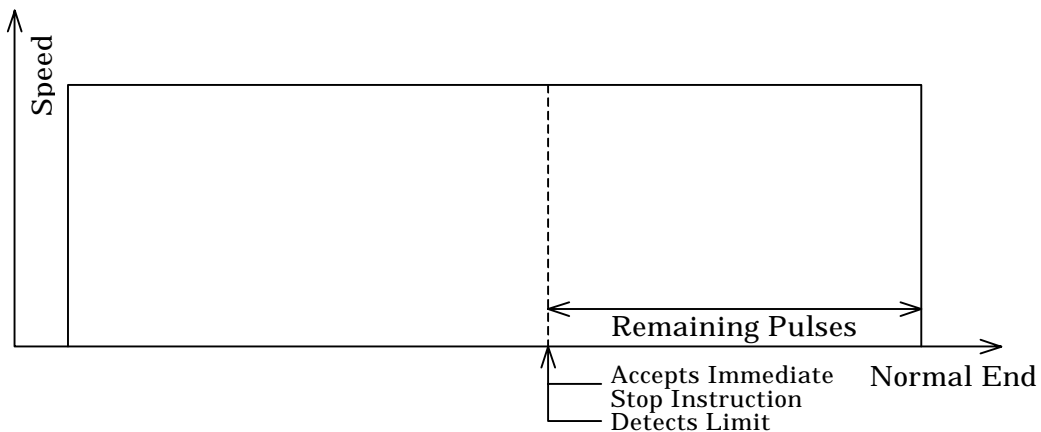


Fig. 3-1 Constant Speed Operation

<<Constant Speed Operational Instruction/Data>>

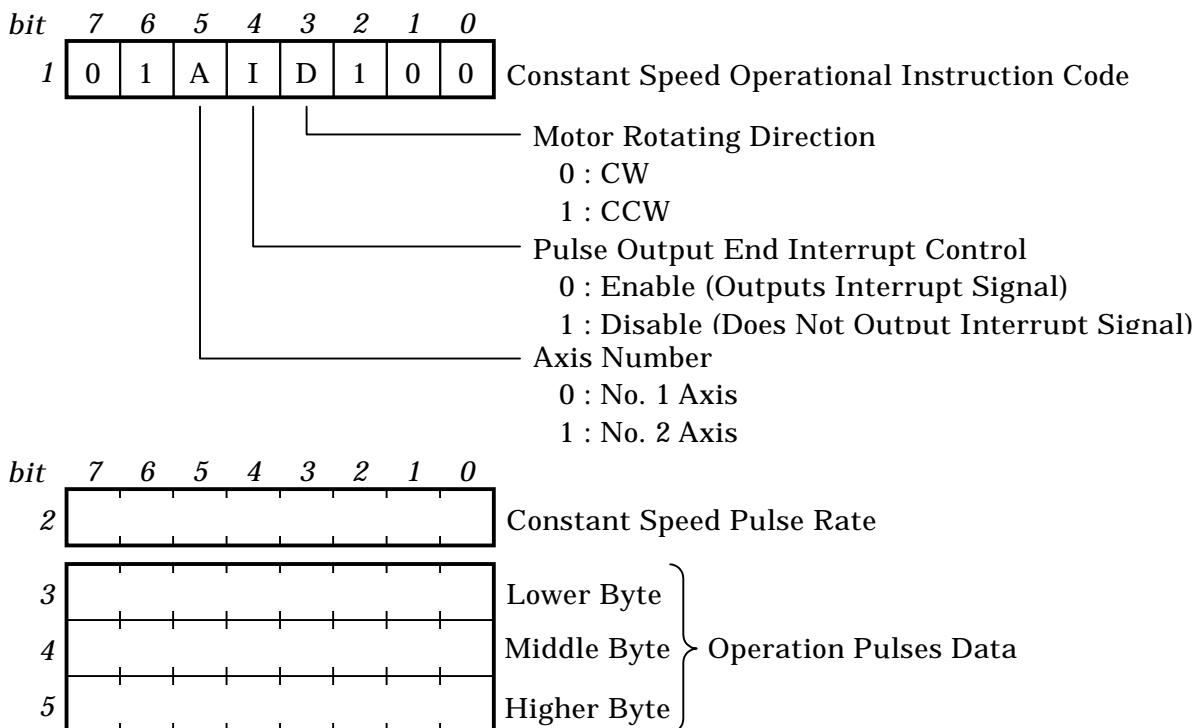


Fig. 3-2 Constant Speed Operational Instruction Code and Data

Fig. 3-3 shows a flow chart for issuing the constant speed operational instruction.

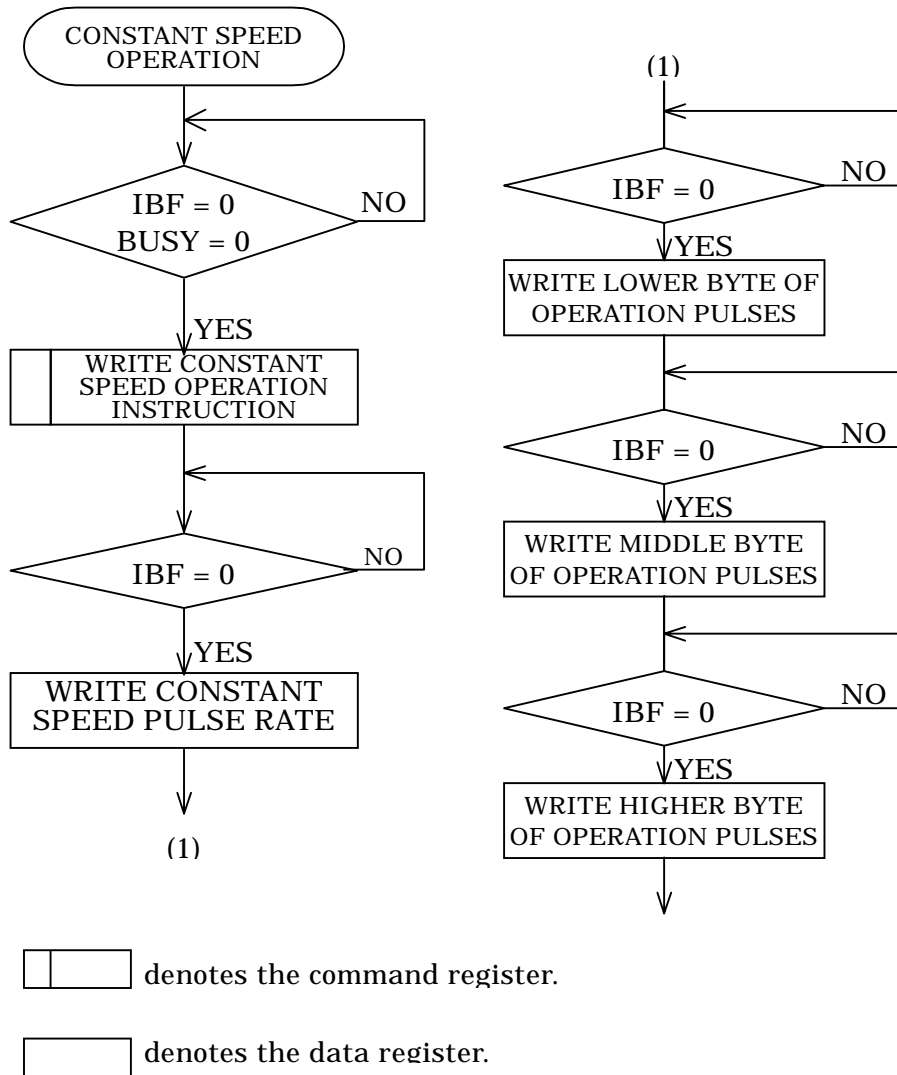


Fig. 3-3 Flow Chart for Constant Speed Operational Instruction

3.4.6 Continuous Constant Speed Operation

Pulse output is allowed only in the phase excitation mode.

This instruction is to output the pulses until the limit signal is detected at the specified constant speed.

It is necessary to specify the 1-byte constant speed pulse rate, following the instruction code. Pulse output is immediately stopped upon detecting the limit (FLn* or BLn*) corresponding to the rotating direction of the operating axis. If it is not detected, pulse output will continue. The maximum pulses to be output at this time is 16,777,216. The limit signal corresponding to the rotating direction is the FL* limit if clockwise pulses are being output, and the BL* limit if the counterclockwise ones are being output. The limits in the non-rotating direction are ignored. If the INT bit is set to "0", the interrupt signal (INT*) will be output after completion of pulse output.

When writing this instruction code, check the IBF bit of the status register and the BUSY bit of the relevant axis. The data should be written sequentially, checking the IBF bit.

The constant speed pulse rate can be specified within a range of 1h to FFh, but it is necessary to pay attention to the specified rate. For details, see Supplementary Explanation in 3.3 **Initial Setting Instruction**.

Pulse output can be stopped by the ALM signal, rotating direction limit signal, or immediate stop instruction.

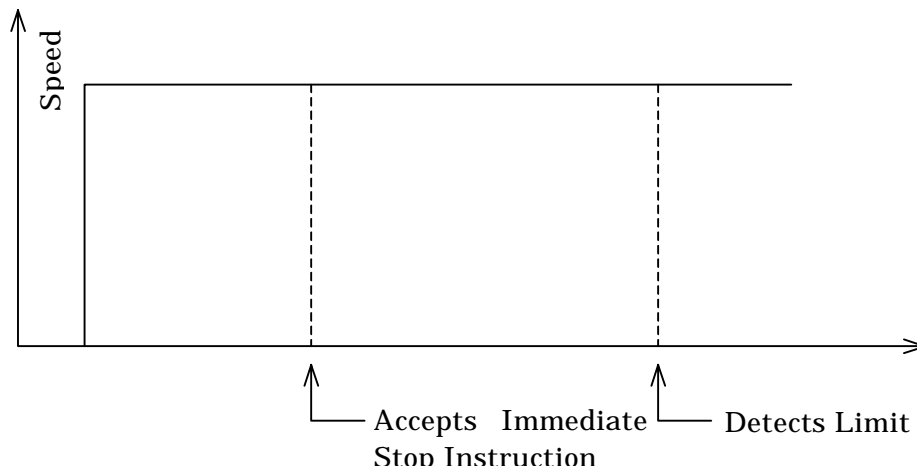


Fig. 3-1 Continuous Constant Speed Operation

<<Continuous Constant Speed Operational Instruction/Data>>

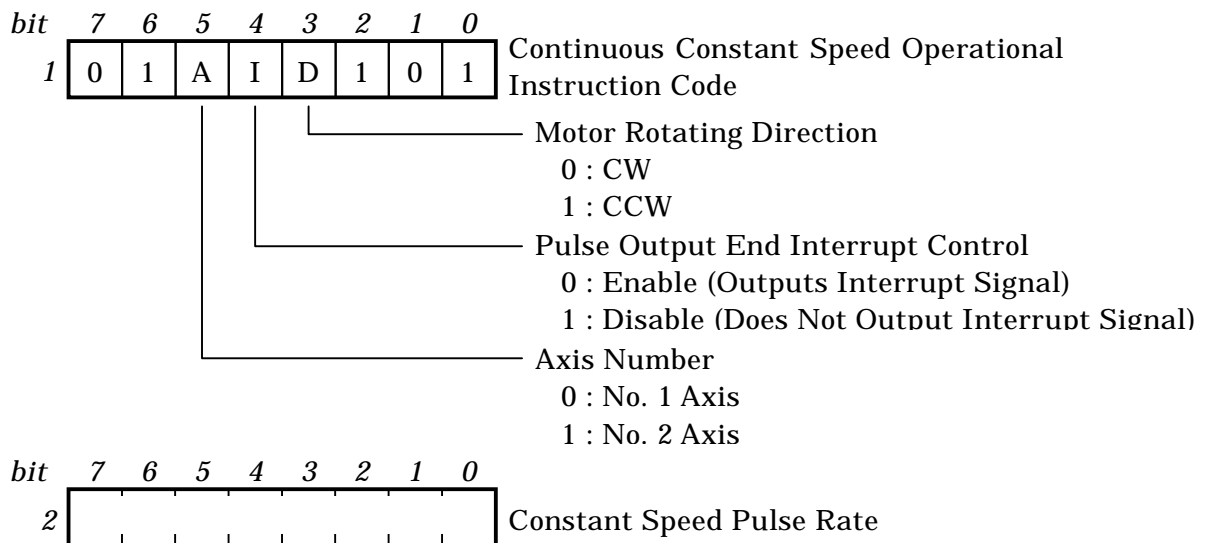


Fig. 3-2 Continuous Constant Speed Operational Instruction Code and Data

Fig. 3-3 shows a flow chart for issuing the continuous constant speed operational instruction.

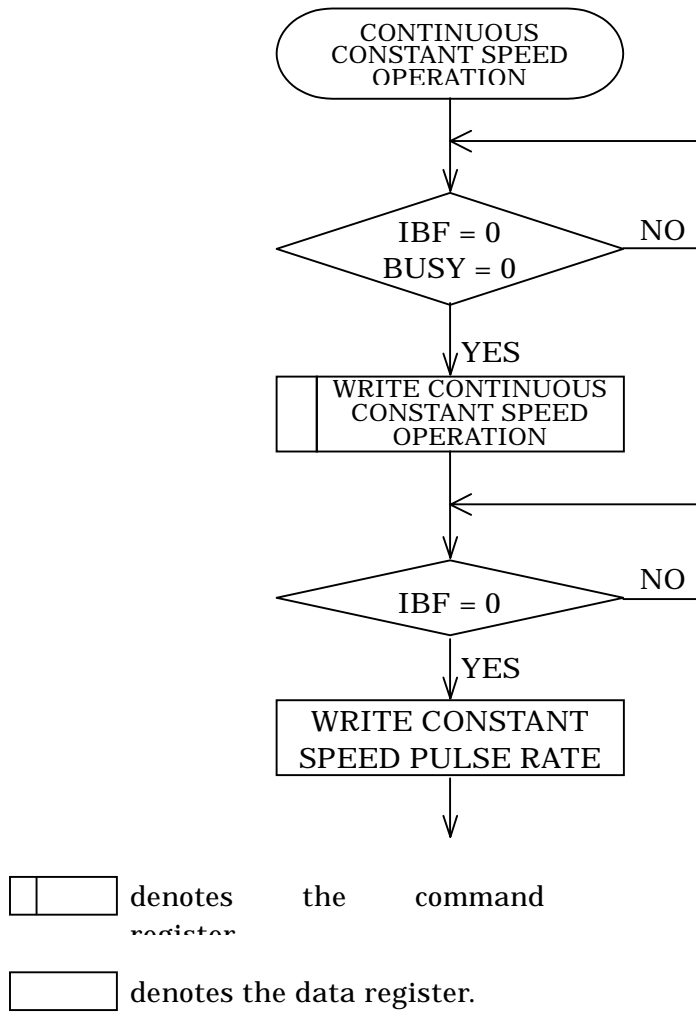


Fig. 3-3 Flow Chart for Continuous Constant Speed Operational Instruction

3.4.7 Continuous High Speed Operation

This instruction is to accelerate in accordance with the initial setting instruction and continue to output the pulses at high speed until the high speed limit is detected. As it only contains the instruction code, it is not necessary to specify the data. Pulse output stops upon detecting the limit (FLn* or BLn*) corresponding to the rotating direction of the specified axis or the deceleration limit (FHLn* or BHLn*). If none of them can be detected, 16,777,216 pulses will be output at high speed (decelerates when stopping). The high speed limit corresponding to the rotating direction is the FHLn* limit if clockwise pulses are being output, and the BHLn* limit if the counterclockwise ones are being output. The high speed limits in the non-rotating direction are ignored. If the INT bit is set to "0", the interrupt signal (INT*) will be output after completion of pulse output. When writing this instruction code, check the IBF bit of the status register and the BUSY bit of the relevant axis.

Pulse output can be stopped by the ALM signal, rotating direction limit signal, deceleration limit signal, immediate stop instruction, or deceleration stop instruction.

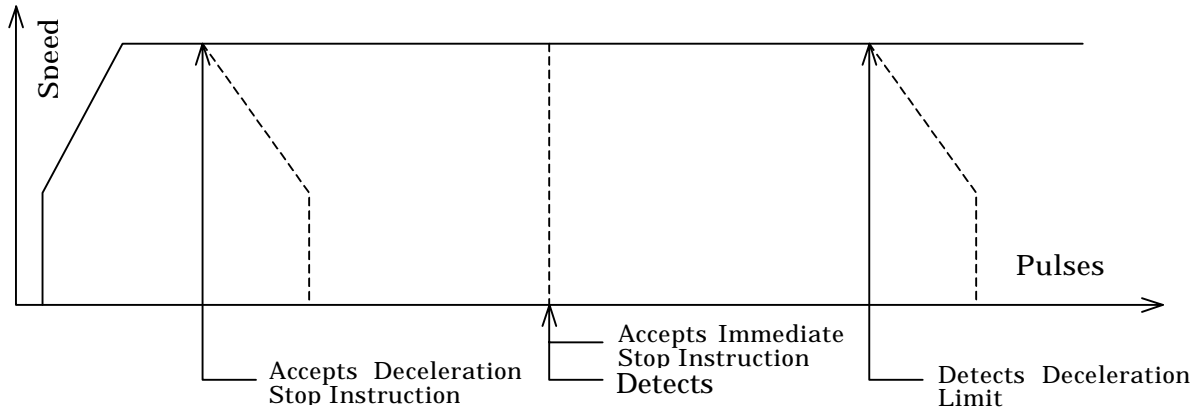


Fig. 3-1 Continuous High Speed Operation

<<Continuous High Speed Operational Instruction>>

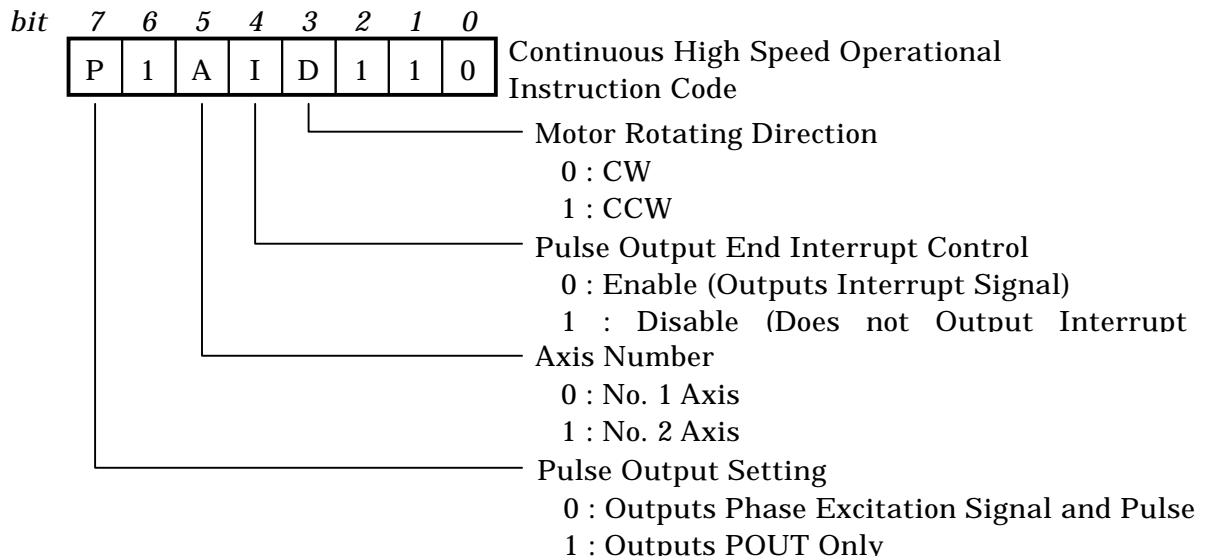
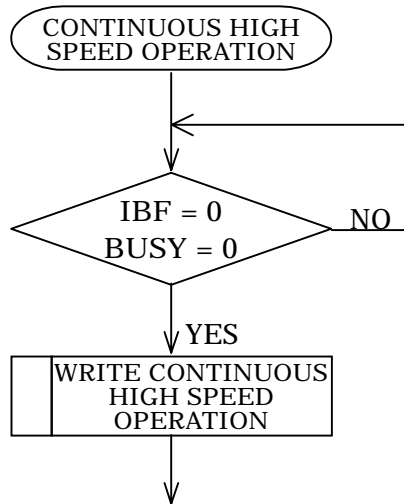


Fig. 3-2 Continuous High Speed Operational Instruction Code

Fig. 3-3 shows a flow chart for issuing the continuous constant speed operational instruction.




 denotes the command register.

Fig. 3-3 Flow Chart for Continuous High Speed Operational Instruction

3.4.8 Constant Speed Origin Search

Pulse output is allowed only in the phase excitation mode.

This instruction is to output the pulses until the origin signal is detected at the specified constant speed.

It is necessary to specify the 1-byte constant speed pulse rate, following the instruction code. Pulse output is completed upon detecting the origin signal (ORGn*) for the relevant axis or detecting the limit (FLn* or BLn*). If either of them cannot be detected, the pulses will be output until reaching the maximum pulse output count, 16,777,216.

If the INT bit is set to "0", the interrupt signal (INT*) will be output after completion of pulse output.

When writing this instruction code, check the IBF bit of the status register and the BUSY bit of the relevant axis. The data should be written sequentially, checking the IBF bit.

The pulse rate can be specified within a range of 1h to FFh, but it is necessary to pay attention to the specified rate. For details, see Supplementary Explanation in 3.3 **Initial Setting Instruction**.

Pulse output can be stopped by the ALM signal, rotating direction limit signal, or immediate stop instruction.

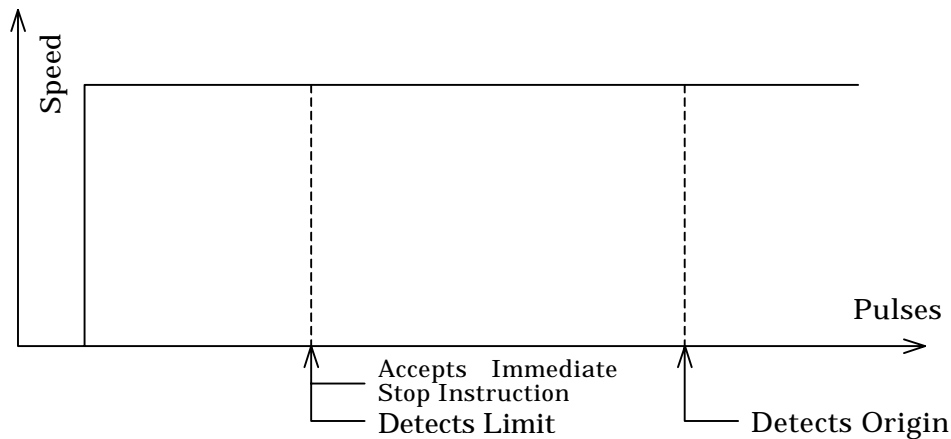


Fig. 3-1 Constant Speed Origin Search

<<Constant Speed Origin Search Operational Instruction/Data>>

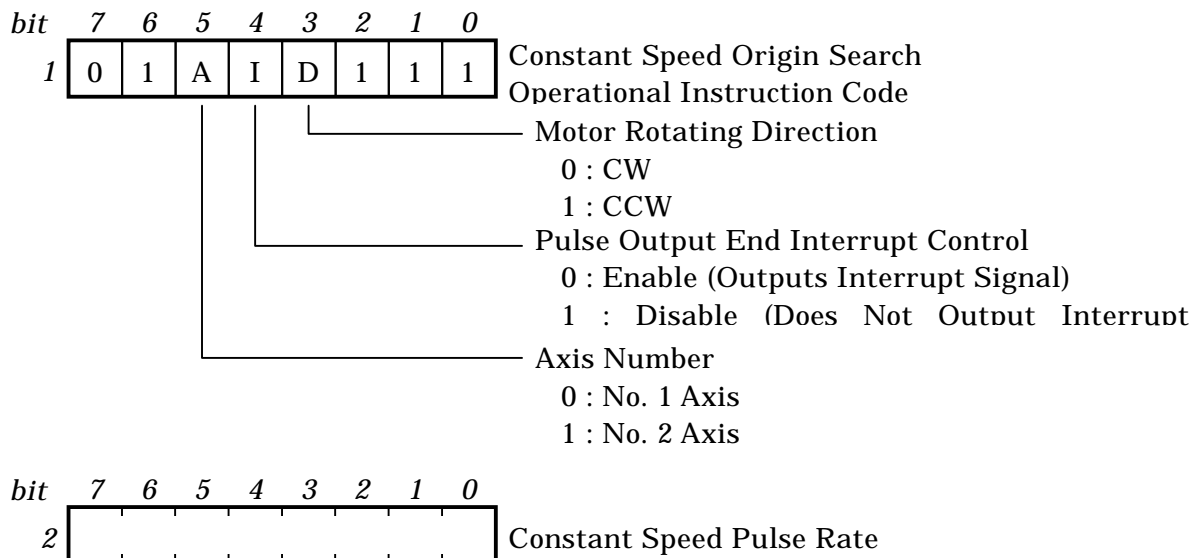
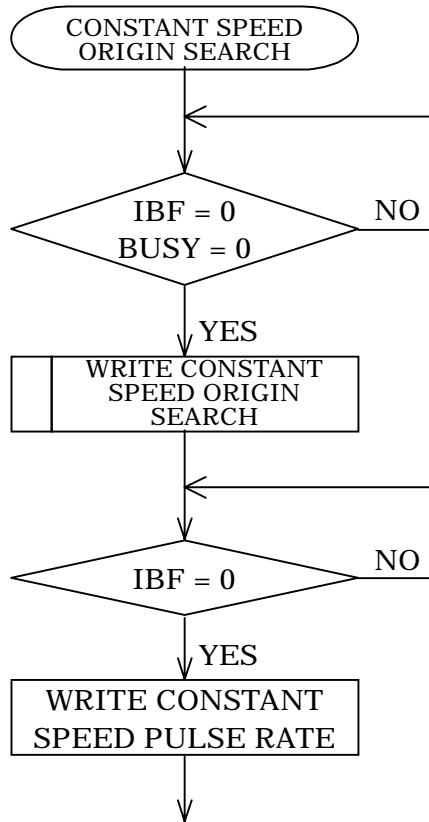
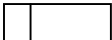


Fig. 3-2 Constant Speed Origin Search Operational Instruction Code and Data

Fig. 3-3 shows a flow chart for issuing the constant speed origin search operational instruction.



 denotes the command register.

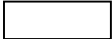
 denotes the data register.

Fig. 3-3 Flow Chart for Constant Speed Origin Search Operational Instruction

3.5 Internal Register Read Instructions

These instructions allow you to check the PPMC-2104 internal state or input signal state. There are five kinds of internal information read instructions as shown in **Fig. 3-1**.

<<Internal Register Read Instruction>>

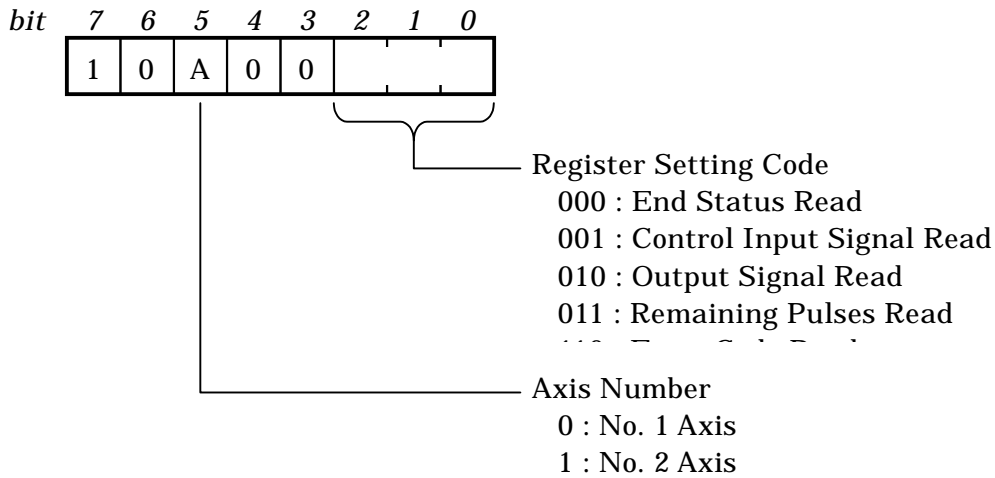


Fig. 3-1 Bit Configuration of Internal Register Read Instruction

3.5.1 End Status Code Read Instruction

This instruction is to read the factor upon ending pulse output. It contains only the instruction code. It checks the OBF bit of the status register after reading the instruction code and reads the 1-byte end status code.

<<End Status Read Instruction/Data>>

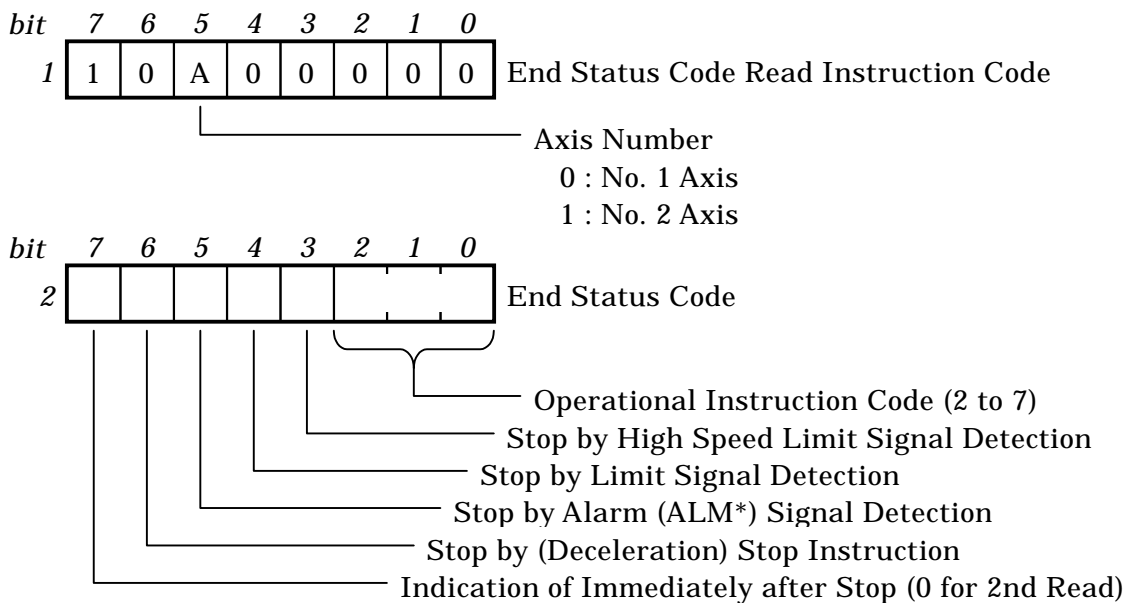


Fig. 3-1 End Status Code Read Instruction Code and Read Data

The Bit 7 of the end status code has been set to "1" at the first read immediately after a stop and can be read as many times as you want while the relevant axis is stopping. From the second read onward, it will be set to "0".

(1) Bits 2-0 [Operational Instruction]

These bits hold the lower three bits of the instruction code given upon starting operation.

(2) Bit 3 [Stop by High Speed Limit Input Signal Detection]

The Bit 3 detects the high speed limit signal (FLn* or BLn*) corresponding to the specified operating direction of the relevant axis while outputting the pulses and is set to "1" upon ending pulse output.

(3) Bit 4 [Stop by Limit Input Signal Detection]

The Bit 4 detects the limit signal (FHLn* or BHLn*) corresponding to the specified operating direction of the relevant axis while outputting the pulses and is set to "1" upon ending pulse output.

(4) Bit 5 [Stop by Alarm Input Signal Detection]

The Bit 5 detects the alarm signal (ALMn*) for the relevant axis while outputting the pulses and is set to "1" upon ending pulse output.

(5) Bit 6 [Stop by Stop Instruction]

The Bit 6 accepts the stop or deceleration stop instruction while outputting the pulses and is set to "1" upon ending pulse output.

(6) Bit 7 [Flag Indicating Immediately after Stop]

The Bit 7 is set to "1" when this register is read for the first time after ending pulse output. It will be set to "0" at the second read onward.

Interrupt (INT*) signal output upon completion of pulse output is reset by issuing the end status read instruction. If there has been any interrupt generated by an instruction error simultaneously (or if there has been an interrupt upon completion of pulse output of the other axis), interrupt (INT*) signal output will be reset once, but resumed again 5 μ s later. To reset interrupt (INT*) signal output caused by the instruction error, issue the "Error Code Read Instruction."

When writing this instruction code, it is necessary to check the IBF and BUSY bits of the status register. When reading the end status code, it is necessary to make sure that the OBF bit is "1". If the OBF bit is "1", be sure to read the data.

Fig. 3-2 shows a flow chart for issuing the end status read instruction.

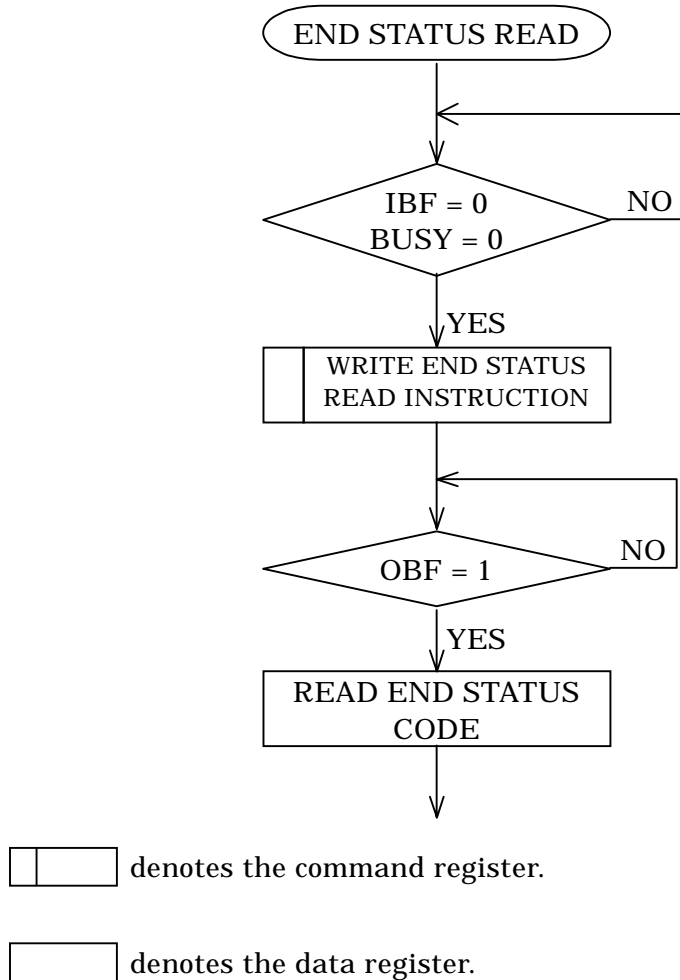


Fig. 3-2 Flow Chart for End Status Read Instruction

3.5.2 Control Input Signal Read Instruction

This instruction is to read the status of each limit input signal, origin signal, or alarm signal for the PPMC-2104. It reads the status of each input terminal upon executing it. If the PPMC-2104 detects the high speed limit and decelerates to stop, therefore, the Bits 2 and 0 will not be turned to "0" because it has passed the high speed limit detection point. For the bit status, "0" indicates that there is an input signal, and "1" that there is no input signal. This instruction contains only the instruction code and reads the 1-byte control input signal status code after writing the instruction code.

To write this instruction code, it is necessary to check the IBF and BSY bits of the status register. To read the control input signal status code, it is necessary to check the OBF bit. When the OBF bit is "1", be sure to read the data.

<<Control Input Signal Read Instruction/Data>>

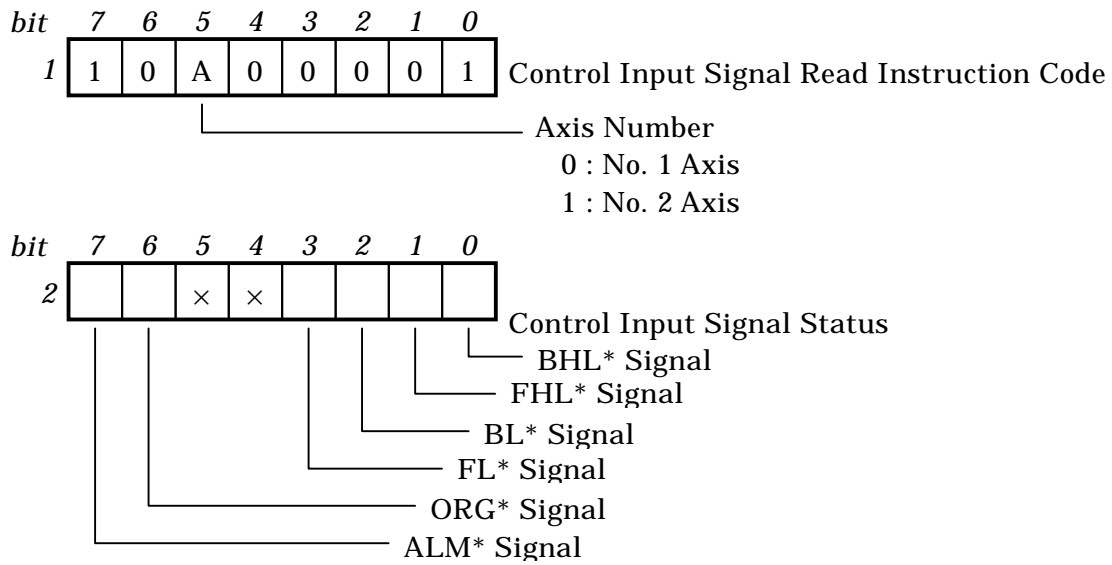
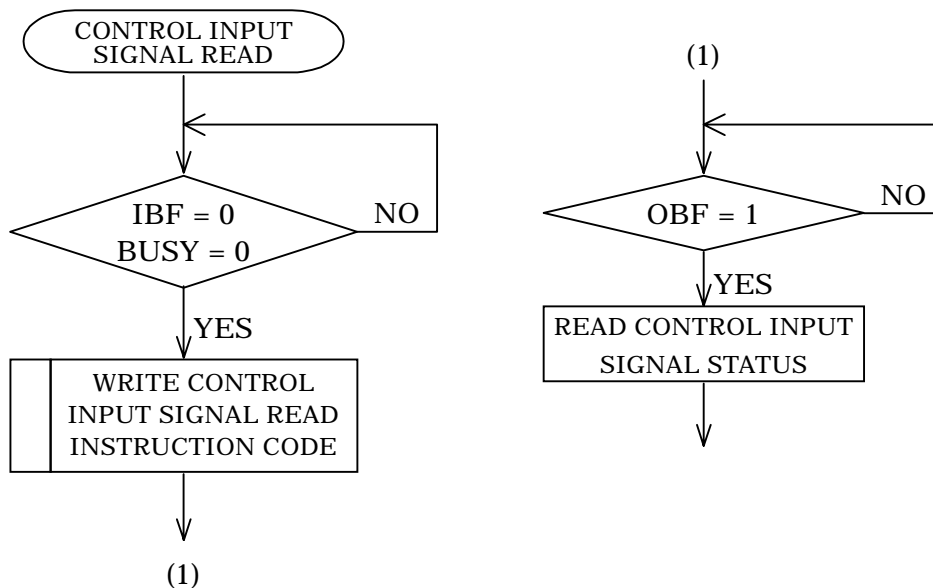


Fig. 3-1 Control Input Signal Read Instruction Code and Read Data

Fig. 3-2 shows a flow chart for issuing the control input signal read instruction.



 denotes the command

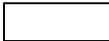
 denotes the data register.

Fig. 3-2 Flow Chart for Control Input Signal Read Instruction

3.5.3 Output Signal Read Instruction

This instruction is to read the status of the phase excitation output signal, etc. for the axis specified in the Bit 5 of the instruction code. It can be executed while pulse output of the specified axis is stopping. This instruction contains only the instruction code and reads an 8-bit output signal after writing the instruction code.

To write this instruction code, it is necessary to check the IBF and BSY bits of the status register. To read the output signal status, check the OBF bit. When the OBF bit is "1", be sure to read the data.

<<Output Signal Read Instruction/Data>>

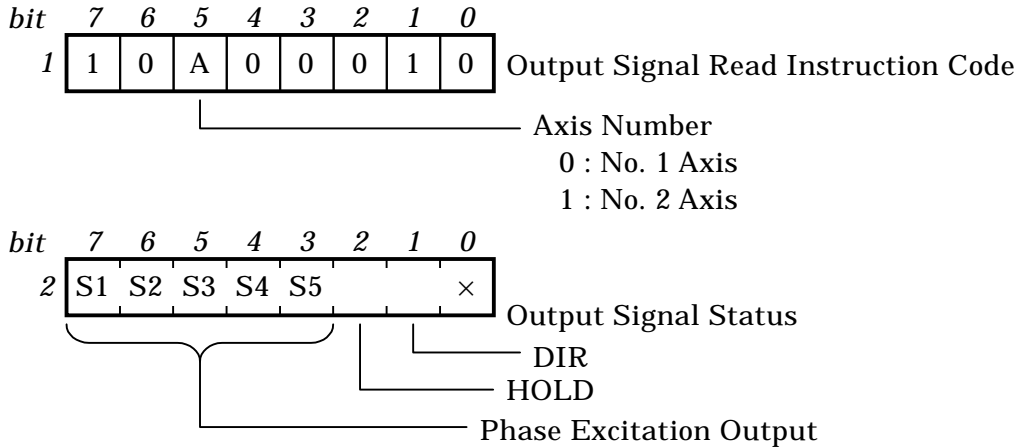


Fig. 3-1 Output Signal Read Instruction Code and Read Data

Fig. 3-2 shows a flow chart for issuing the output signal read instruction.

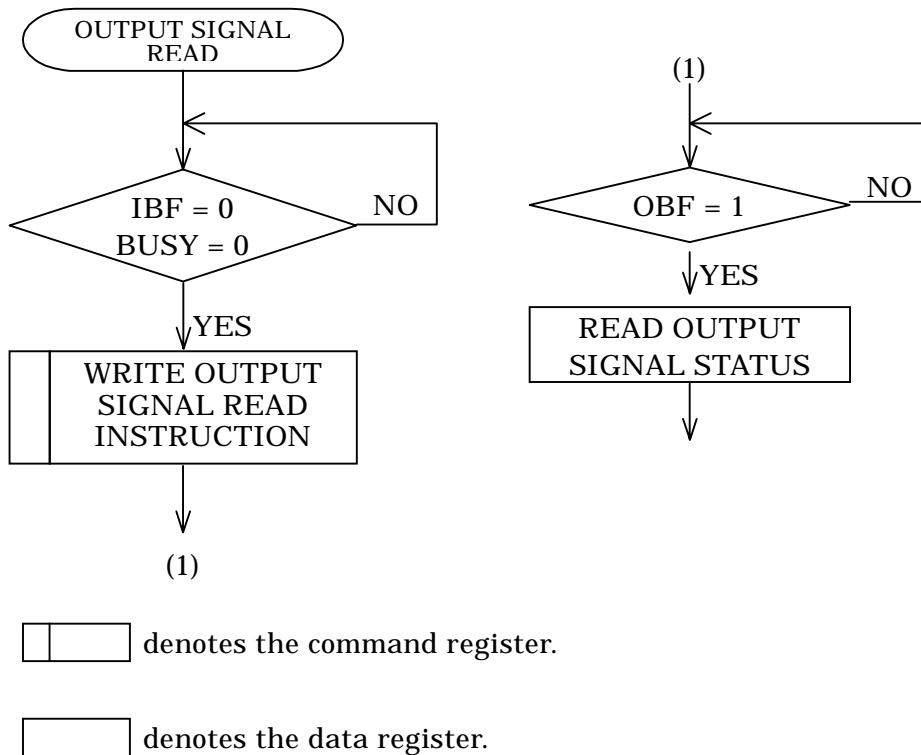


Fig. 3-2 Flow Chart for Output Signal Read Instruction

3.5.4 Remaining Pulses Read Instruction

This instruction is to read the number of remaining pulses when the PPMC-2104 has stopped. It can be executed while pulse output of the specified axis is stopping. This instruction contains only the instruction code and reads the 24-bit number of remaining pulses.

To write this instruction code, it is necessary to check the IBF and BUSY bits of the status register. When reading the number of remaining pulses, read in order of the lower, middle, and higher bytes one by one, checking the OBF bit. When OBF bit is "1", be sure to read the data.

For the number of remaining pulses returned, the actual value minus 1 is reported. That is, when the actual number of remaining pulses is 3, the number reported will be 2. If the number of remaining pulses is reported 0, determine whether the actual number of remaining pulses is 0 or 1, together with the result of the end status read instruction.

<<Remaining Pulses Read Instruction/Data>>

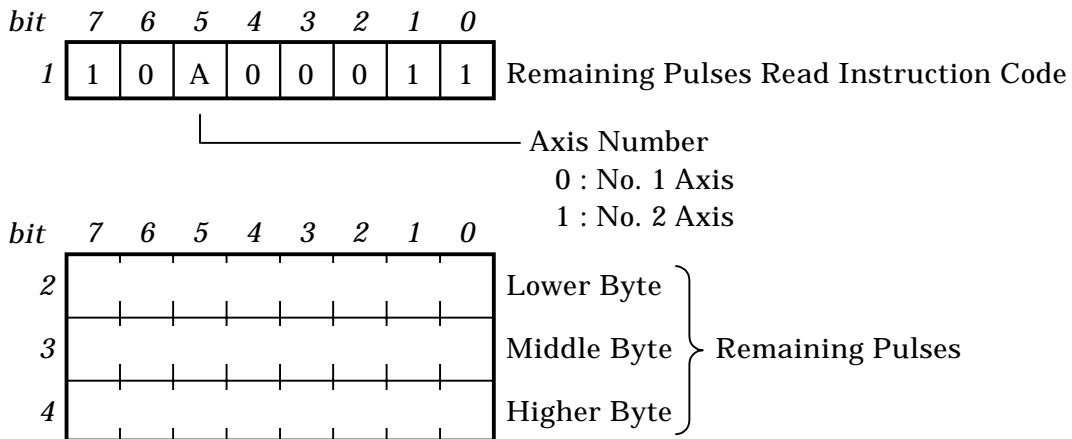


Fig. 3-1 Remaining Pulses Read Instruction Code and Read Data

Fig. 3-2 shows a flow chart for issuing the PPMC-2104 position read instruction.

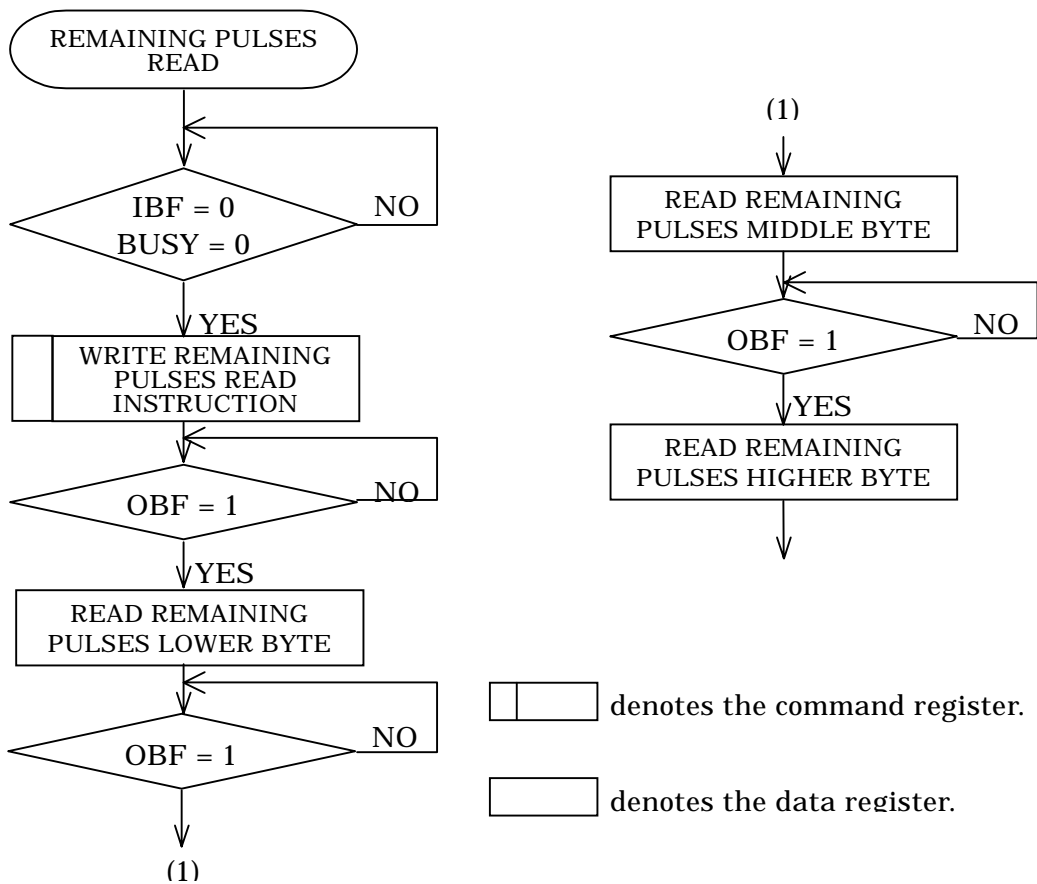


Fig. 3-2 Flow Chart for Remaining Pulses Read Instruction

3.5.5 Error Code Read Instruction

When there is an instruction error, this instruction is to read its error factor. It can be executed regardless of the pulse output status of the relevant axis. This instruction code contains only the instruction code and reads the 1-byte error code after writing the instruction code.

When issuing this instruction code, it is necessary to make sure that the IBF bit of the status register is "0". When reading the error code, it is necessary to make sure that the OBF bit is "1". When the OBF bit is "1", be sure to read the data.

If there is any error in the instruction code or data given from the host processor to the PPMC-2104, the interrupt (INT*) signal will be output, setting "1" in the Bit 7 (ERR bit) of the status register.

The error code is overwritten every time a wrong instruction is received from the host processor, and cleared to "00h" when this instruction is executed. The Bit 7 (ERR bit) of the status register is also set every time a wrong instruction is received from the host processor, and reset to "0" when this instruction is given.

The interrupt (INT*) signal caused by an instruction error is reset by issuing the error code read instruction. If there has been an interrupt generated by completion of pulse output, the interrupt (INT*) signal will be reset once and set again 5 μs later. The interrupt (INT*) signal by completion of pulse output is only reset by the end status read instruction.

<<Error Code Read Instruction/Data>>

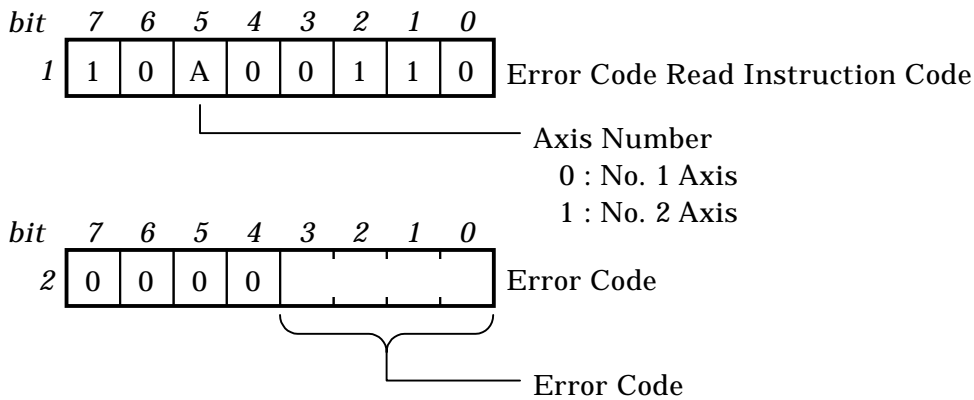
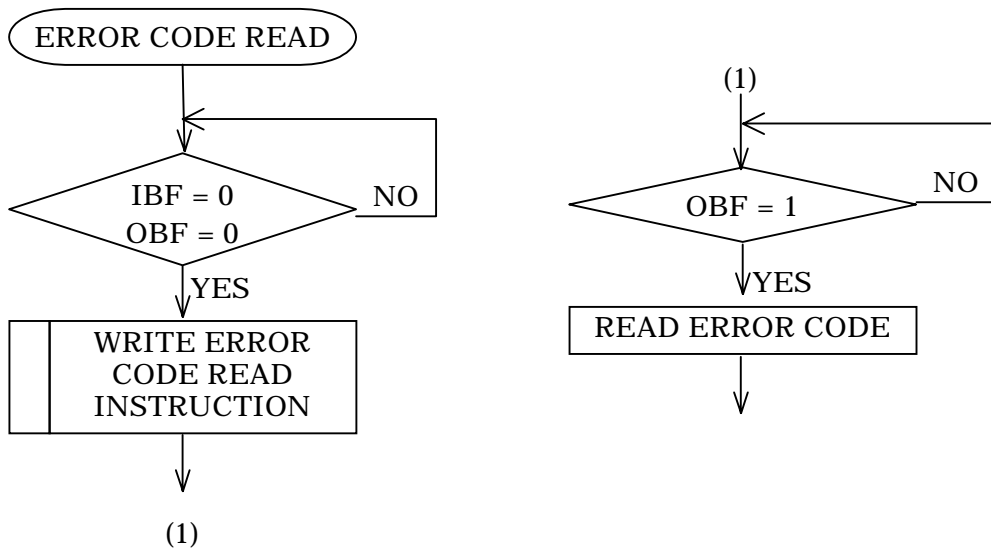



Fig. 3-1 Error Code Read Instruction Code and Read Data

Fig. 3-2 shows a flow chart for issuing the error code read instruction.



 denotes the command register.


 denotes the data register.

Fig. 3-2 Flow Chart for Error Code Read Instruction

Table 13 Instruction Error Codes List

Error Code	Description
00	No error
01	Undefined instruction
02	Has not received the instruction code.
03	Has received the instruction while waiting for the data.
04	Initial setting not completed.
05	Busy and cannot execute.
06	Cannot execute while stopping. (Deceleration stop instruction)
07	Cannot operate on the limit ALM or ORG.
08	Has received the deceleration instruction during deceleration or constant speed operation, or while holding RUN.
09	Abnormal rate data or too few acceleration/deceleration pulses
10	Abnormal acceleration/deceleration pulses
11	Switching parameter less than 40h
12	Rate error 1 (Cannot operate at the specified rate because single-axis operation exceeds the limit rate) *
13	Rate error 2 (Cannot operate at the specified rate because the other axis is operating) *

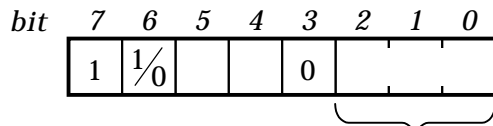
* When Error 2 takes place, issue the error code read instruction to the No. 1 axis.

* Errors 12 and 13 take place only when the internal clock has been selected as the clock source with the initial setting instruction.

3.6 Auxiliary Instructions

The auxiliary instructions allow excitation OFF operation and auxiliary input/output operation. As shown in Fig. 3-1, there are 5 kinds of auxiliary instructions. The auxiliary input/output instructions can be executed regardless of whether the pulses are being output or stopping. The excitation OFF instruction, etc. can be executed only when pulse output is being stopping.

<<Auxiliary Instruction>>



Instruction Code

000 : Excitation OFF Instruction

001 : Auxiliary Output Instruction

010 : Auxiliary Input Instruction

100 : Switching Frequency Setting Instruction

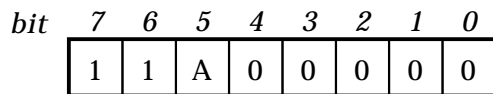
101 : Hold Signal Delay Time Setting Instruction

Fig. 3-1 Bit Configuration of Auxiliary Instruction

3.6.1 Excitation OFF Instruction

When writing this instruction code, it is necessary to make sure that the BUSY and IBF bits for the relevant axis of the status register are "0".

<<Excitation OFF Instruction>>



Excitation OFF Instruction Code

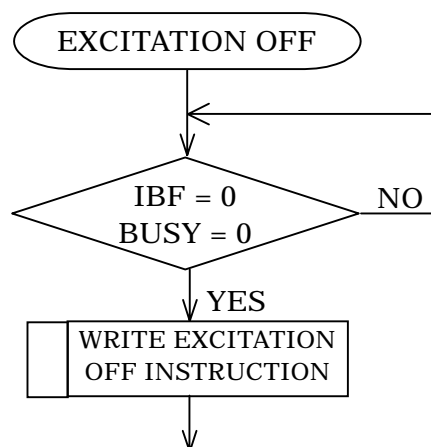
Axis Number

0 : No. 1 Axis

1 : No. 2 Axis

Fig. 3-1 Excitation OFF Instruction Code

Fig. 3-2 shows a flow chart for issuing the excitation OFF instruction.



 denotes the command register.

Fig. 3-2 Flow Chart for Excitation OFF Instruction

3.6.2 Auxiliary Output Instruction

This instruction is to set the signal output of the auxiliary output terminals, AUXO0 and AUXO1. After the PPMC-2104 has received this auxiliary output instruction, there is a delay of about 40 μ s until the output terminals change their status. The auxiliary output signal is set to the "H" level after resetting.

This instruction is valid even while the PPMC-2104 is outputting the pulses. To write the instruction code, it is necessary to make sure that the IBF bit of the status register is "0".

The auxiliary output data is of negative logic output. Setting "0" outputs the "H" level to the relevant terminal of the auxiliary output signal, and "1" outputs the "L" level.

<<Auxiliary Output Instruction>>

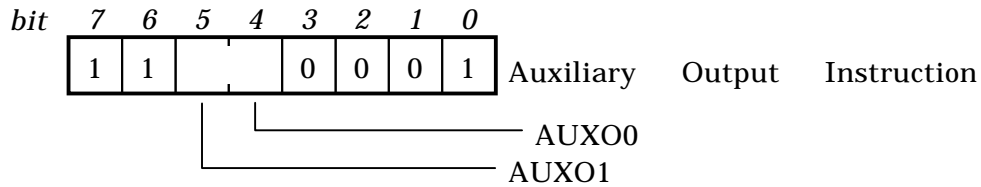
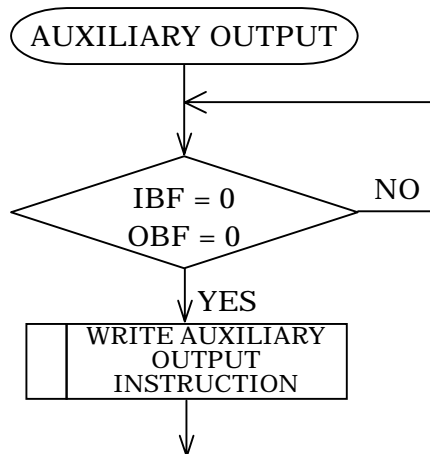


Fig. 3-1 Auxiliary Output Instruction Code

Fig. 3-2 shows a flow chart for issuing the auxiliary output instruction.



denotes the command register.

Fig. 3-2 Flow Chart for Auxiliary Output Instruction

3.6.3 Auxiliary Input Signal Read Instruction

This instruction is to read the status of the auxiliary input AUXI0/AUXI1 signal. There is a delay of about 40 μs to read the auxiliary input signal. This instruction contains only the instruction code and reads the 1-byte (2-bit) auxiliary input data after writing the instruction code.

To write this instruction, it is necessary to make sure that the IBF bit of the status register is "0".

To read the auxiliary input signal, make sure that the OBF bit is "1". When it is "1", be sure to read the data.

<<Auxiliary Input Signal Read Instruction Code/Data>>

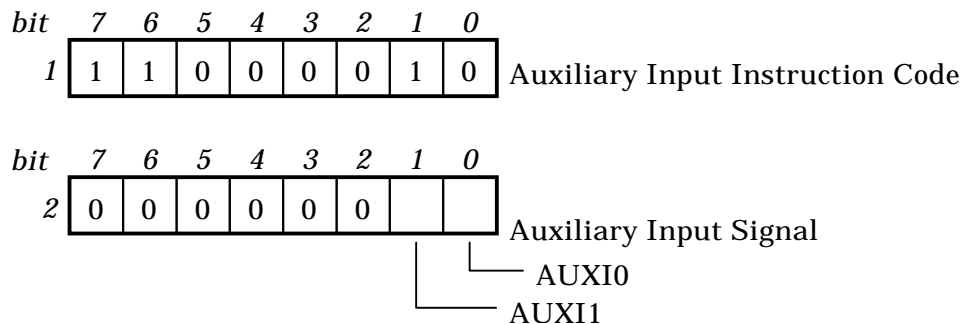
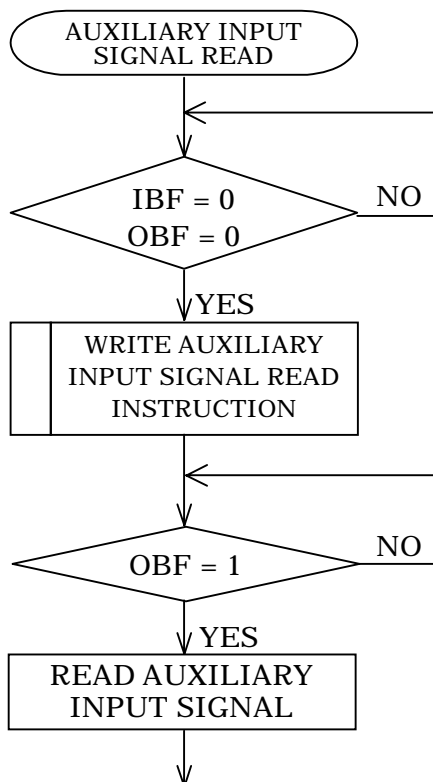


Fig. 3-1 Auxiliary Input Read Instruction Code and Read Data

Fig. 3-2 shows a flow chart for issuing the auxiliary input signal status code read instruction.



denotes the command

denotes the data register.

Fig. 3-2 Flow Chart for Auxiliary Input Signal Read Instruction

3.6.4 Switching Frequency Setting Instruction

Switching means to turn on/off the phase excitation signal in order to reduce the phase excitation current while the PPMC-2104 is stopping. While the stepping motor is stopping, only its winding resistance limits the current running to the activated (turned to ON) phase, and at this time, the current becomes maximum. If the phase excitation signal is turned on/off, the current can be limited by the winding inductance of the stepping motor.

For this instruction, write the ON-time data and OFF-time data in that order, subsequent to the instruction code. If this instruction is not executed, the switching frequency is set to about 8 kHz (ON-time: 53 hours, OFF-time: A6h).

The set value is 40h to FFh. The actual time is 0.5 x the set value [μ sec].

<<Switching Frequency Setting Instruction/Data>>

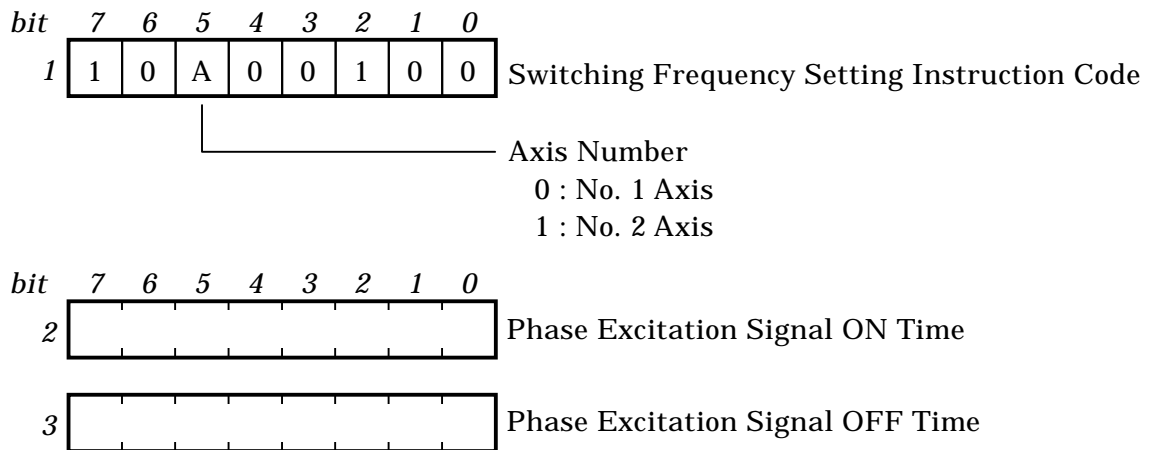


Fig. 3-1 Switching Frequency Setting Instruction Code and Data

Fig. 3-2 shows a flow chart for issuing the switching frequency setting instruction.

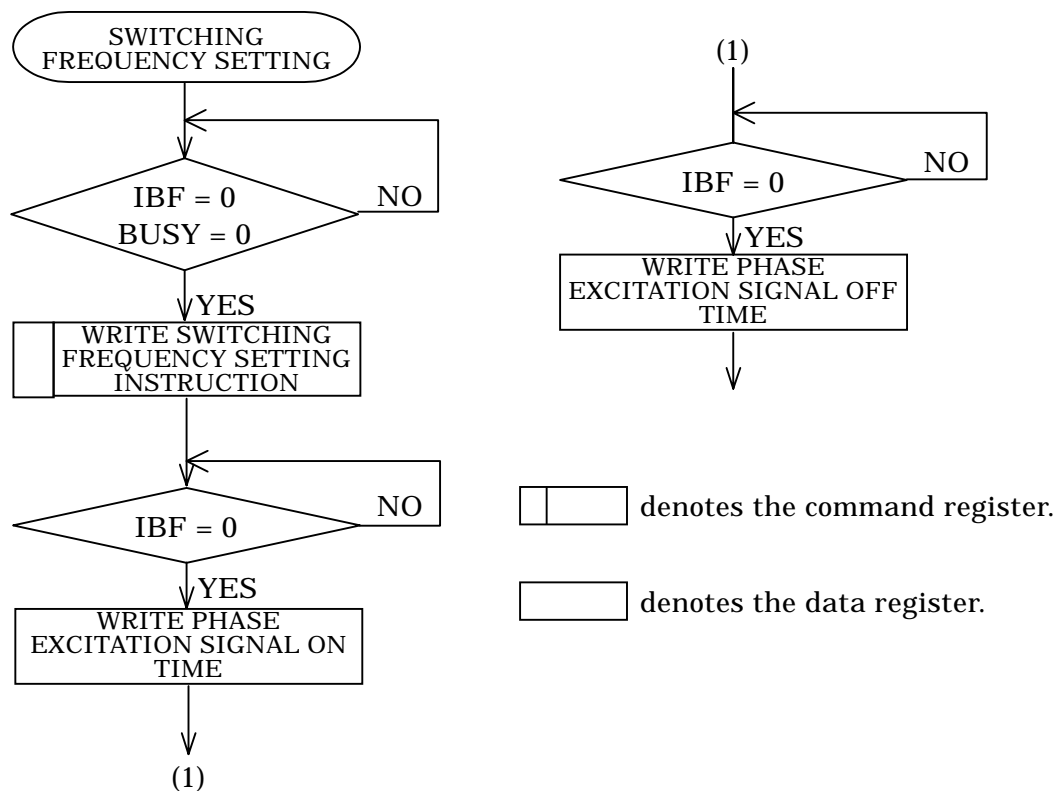


Fig. 3-2 Flow Chart for Switching Frequency Setting Instruction

3.6.5 Hold Signal Delay Time Setting Instruction

This instruction is to set the time between when the PPMC-2104 stops pulse output and when it outputs the HOLD signal.

The set value ranges from 0h to FFh. The delay time is $128 \times (\text{Set value} + 1) [\mu \text{sec}]$. When this instruction is not executed, it is set to 3.2 msec.

<<Hold Signal Delay Time Setting Instruction/Data>>

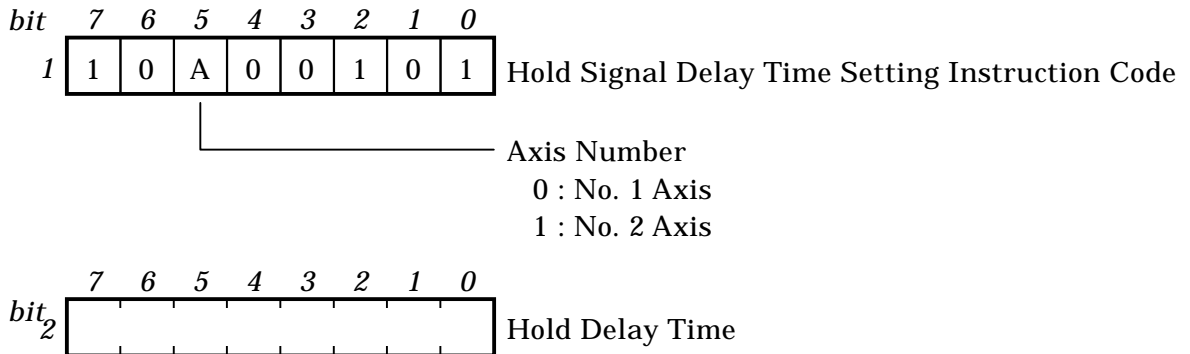
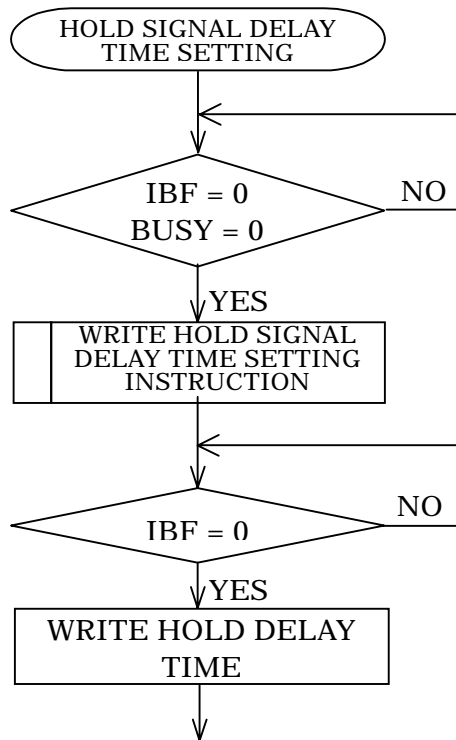


Fig. 3-1 Hold Signal Delay Time Setting Instruction Code and Data

Fig. 3-2 shows a flow chart for issuing the hold output delay time setting instruction.



denotes the command register.

denotes the data register.

Fig. 3-2 Flow Chart for Hold Signal Delay Time Setting Instruction

4. RATINGS

4.1 Absolute Maximum Ratings

Table 14 shows the absolute ratings of the PPMC-2104.

Table 14 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	-0.5 to +6.5	V
Input Voltage	V_{in}	-0.5 to $V_{CC} + 0.5$	V
Power Consumption ($T_a = 85\text{ }^\circ\text{C}$)	P_d	500 (PPMC-2104AFP)	mW
Operating Temperature	T_{opr}	-40 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Soldering Temperature (10s)	T_{solder}	260	$^\circ\text{C}$

If the PPMC-2104 is used beyond the absolute maximum ratings, it may be deteriorated or permanently destroyed.

4.2 DC Characteristics

Table 15 shows the DC characteristics of the PPMC-2104.

Table 15 DC Characteristics

Item	Symbol	Min.	Max.	Unit	Condition
Input "Low" Level Voltage	RESET	-0.3	$0.25V_{CC}$	V	
	X_1	-0.3	$0.2V_{CC}$		
	Others	-0.3	$0.3V_{CC}$		
Input "High" Level Voltage	RESET	$0.75V_{CC}$	$V_{CC} + 03$	V	
	X_1	$0.8V_{CC}$	$V_{CC} + 03$		
	Others	$0.7V_{CC}$	$V_{CC} + 03$		
Output "Low" Level Voltage	All Output Terminals	V_{OL}	0.45	V	$I_{OL} = 1.6\text{mA}$
Output "High" Level Voltage	AUXO0 to AUXO1	V_{OH}	2.4	V	$I_{OH} = -400\text{ }\mu\text{A}$
	Others	V_{OH}	$0.75V_{CC}$		$I_{OH} = -100\text{ }\mu\text{A}$
Input Leak Current	I_{LI}	0.02 (Typ)	± 5	μA	$0.0 \leq V_{in} \leq V_{CC}$
Output Leak Current	I_{LO}	0.05 (Typ)	± 10	μA	$0.0 \leq V_{in} \leq V_{CC} - 0.2$
Current Consumption	I_{CC}	35 (Typ)	50	mA	F = 16MHz
Input Capacity	All Input Pins	C_{IN}	10	PF	F = 1MHz

$V_{CC} = 5\text{ V} \pm 10\%$; $T_a = -20\text{ to }70\text{ }^\circ\text{C}$ (1-16 MHz);

Typical T_a and V_{CC} values are $25\text{ }^\circ\text{C}$ and 5 V, respectively.

4.3 AC Characteristics

4.3.1 RD, WR Separate Type Bus Mode

(1) Register read operation

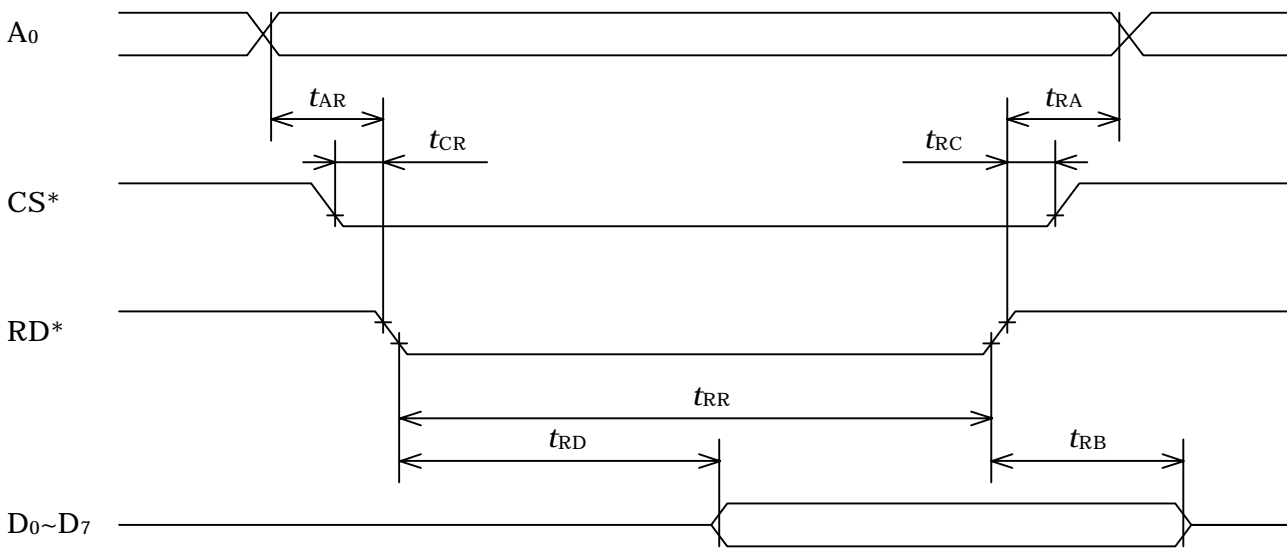


Fig. 4.1 RD, WR Separate Type Bus Mode Register Read Timing

Table 16 RD, WR Separate Type Bus Mode Register Read Parameters

Item	Symbol	Min	Max	Unit
A ₀ Setting Time (To RD* ↓)	t_{AR}	20		ns
A ₀ Holding Time (To RD* ↑)	t_{RA}	5		ns
CS* Setting Time (To RD* ↓)	t_{CR}	0		ns
CS* Holding Time (To RD* ↑)	t_{RC}	0		ns
RD* Pulse Width	t_{RR}	120		ns
RD* ↓ → Valid Data Output	t_{RD}		100	ns
RD* ↑ → Valid Data Hold	t_{RB}	10	90	ns

(V_{CC} = +5 V ±10%, T_a = -20 to 70°C)

(2) Register write operation

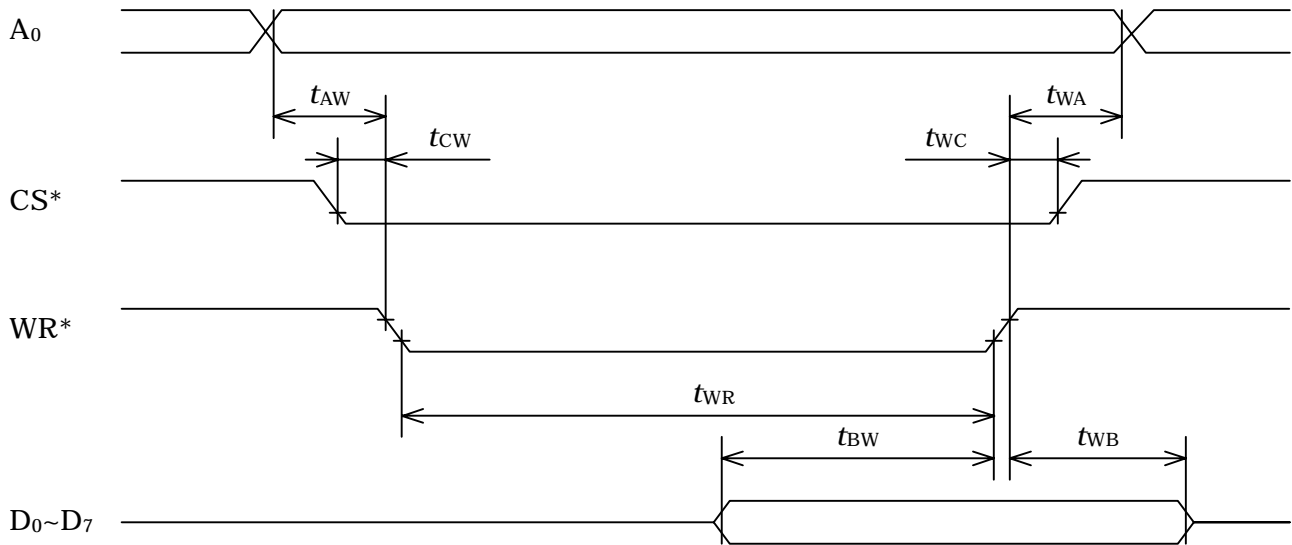


Fig. 4.2 RD, WR Separate Type Bus Mode Register Write Timing

Table 17 RD, WR Separate Type Bus Mode Register Write Parameters

Item	Symbol	Min	Max	Unit
A_0 Setting Time (To $WR^* \downarrow$)	t_{AW}	20		ns
A_0 Holding Time (To $WR^* \uparrow$)	t_{WA}	5		ns
CS^* Setting Time (To $WR^* \downarrow$)	t_{CW}	0		ns
CS^* Holding Time (To $WR^* \uparrow$)	t_{WC}	0		ns
WR^* Pulse Width	t_{WR}	120		ns
Valid Data Input $\rightarrow WR^* \uparrow$	t_{BW}	80		ns
$WR^* \uparrow \rightarrow$ Valid Data Hold	t_{WB}	10		ns

($V_{CC} = +5\text{ V} \pm 10\%$, $T_a = -20$ to 70°C)

4.3.2 DS*, R/W* Type Bus Mode

(1) Register read operation

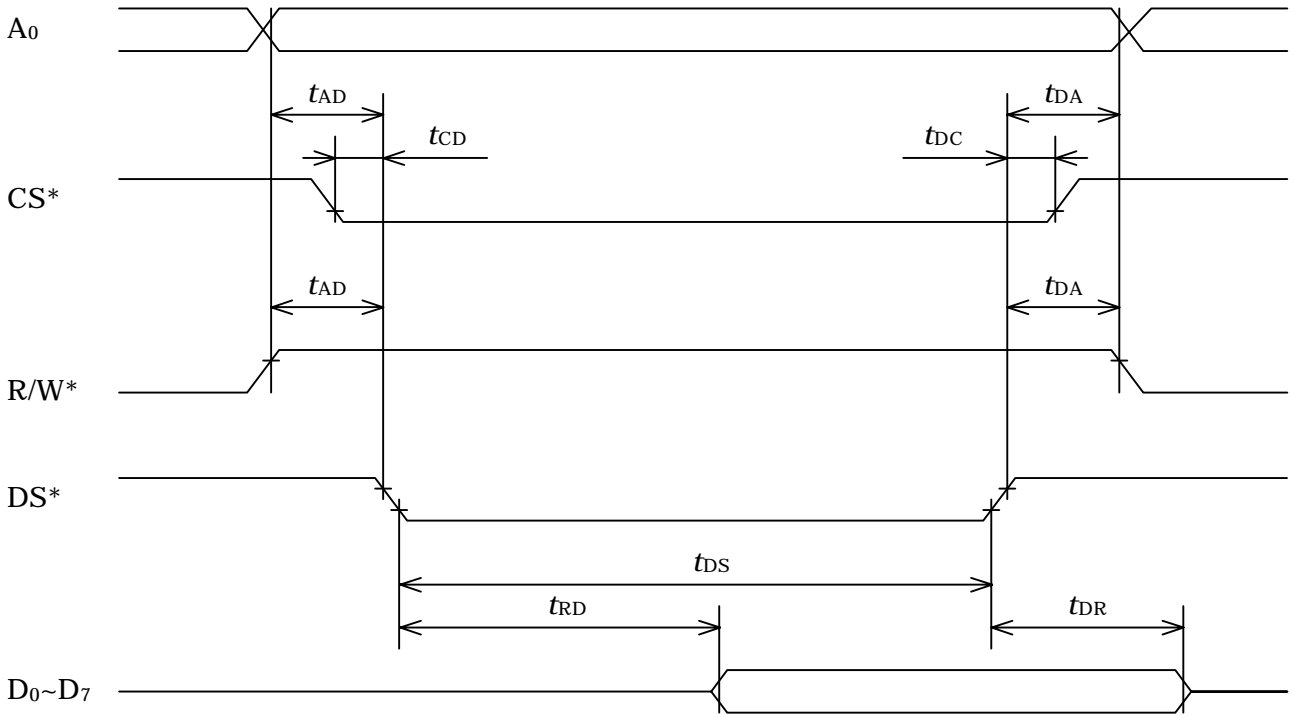


Fig. 4.1 DS*, R/W* Type Bus Mode Register Read Timing

Table 18 DS*, R/W* Type Bus Mode Register Read Parameters

Item	Symbol	Min	Max	Unit
A ₀ R/W* Setting Time (To DS* ↓)	t_{AD}	20		ns
A ₀ R/W* Holding Time (To DS* ↑)	t_{DA}	5		ns
CS* Setting Time (To DS* ↓)	t_{CD}	0		ns
CS* Holding Time (To DS* ↑)	t_{DC}	0		ns
DS* Pulse Width	t_{DS}	120		ns
DS* ↓ → Valid Data Output	t_{RD}		100	ns
DS* ↑ → Valid Data Hold	t_{DR}	10	90	ns

(V_{CC} = +5 V ±10%, T_a = -20 to 70°C)

(2) Register write operation

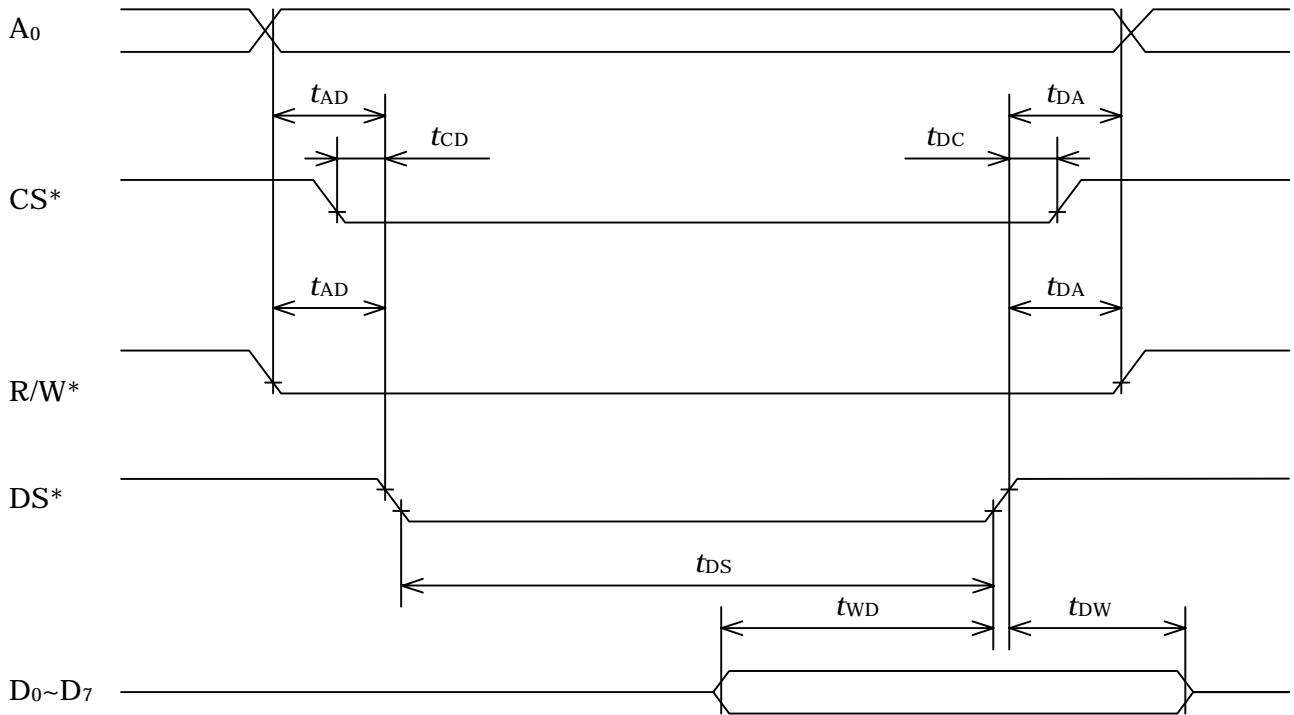


Fig. 4.2 DS*, R/W* Type Bus Mode Register Write Timing

Table 19 DS*, R/W* Type Bus Mode Register Write Parameters

Item	Symbol	Min	Max	Unit
A_0 R/W* Setting Time (To $DS^* \downarrow$)	t_{AD}	20		ns
A_0 R/W* Holding Time (To $DS^* \uparrow$)	t_{DA}	5		ns
CS^* Setting Time (To $DS^* \downarrow$)	t_{CD}	0		ns
CS^* Holding Time (To $DS^* \uparrow$)	t_{DC}	0		ns
DS^* Pulse Width	t_{DS}	120		ns
Valid Data Input $\rightarrow DS^* \uparrow$	t_{WD}	80		ns
$DS^* \uparrow \rightarrow$ Valid Data Hold	t_{DW}	10		ns

($V_{CC} = +5\text{ V} \pm 10\%$, $T_a = -20$ to 70°C)

4.4 Outer Dimensions Drawing

4.4.1 PPMC-2104AFP Outer Dimensions Drawing

[Unit: mm]

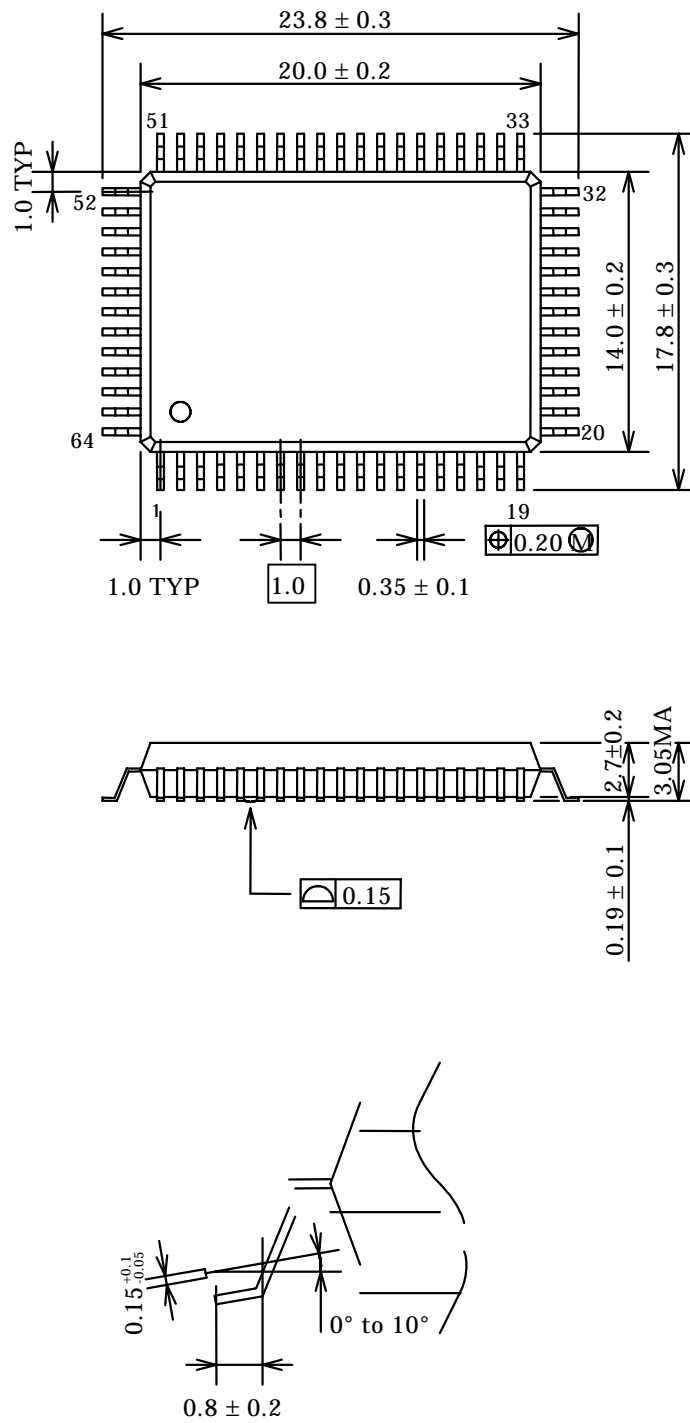


Fig. 4.1 Appearance of PPMC-2104AFP

5. RECOMMENDED MOUNTING CONDITIONS AND PRECAUTIONS FOR HANDLING

The PPMC-2104's package is surface mounting type PPMC-2104CFP. When the PCB is mounted, The most serious effects on the PPMC-2104's reliability include contamination by flux and thermal stress at soldering. The following describes the recommended temperature profile in each mounting method and general precautions.

5.1 Temperature Profile

5.1.1 In Case of Soldering Iron

- (1) The lead area temperature should be 260 °C, within 10 seconds or 350 °C, within 3 seconds.

5.1.2 In Case of Far/Medium Infrared Ray Reflow

- (1) Recommended is the vertical heating method with far/medium infrared rays.
- (2) The package surface temperature should be 210 °C or higher, 240 °C at maximum, within 30 seconds. **Fig. 5.1** shows an example of the recommended temperature profile.
- (3) Note that near infrared reflow will result in thermal stress like solder dip.

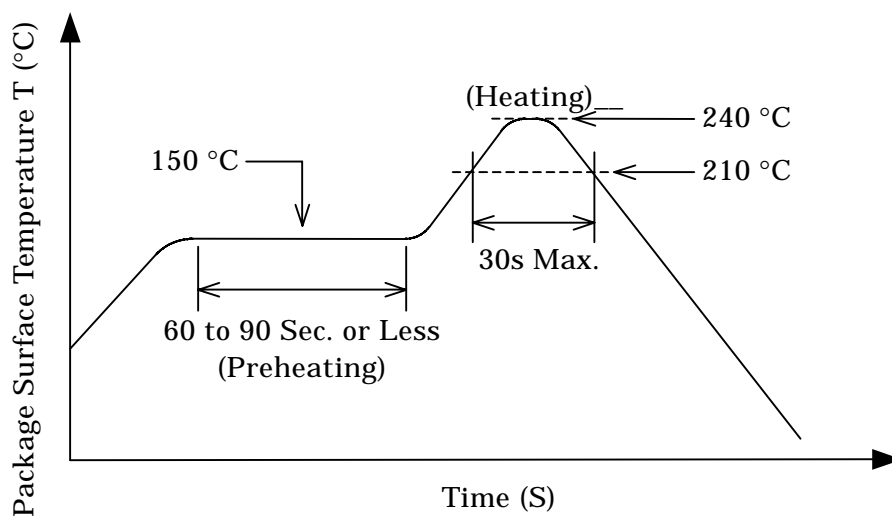


Fig. 5-1 Temperature Profile

5.1.3 In Case of Hot Air Reflow

- (1) The package surface temperature should be 210 °C or higher, 240 °C at maximum, within 30 seconds.
- (2) For the recommended temperature profile, see **Fig. 5-1**.

5.1.4 Baking

If a tray is heat resistant, perform baking for 20 hours at 125 °C, and If not, for 168 hours at 70 °C.

5.1.5 In Case of Vapour Phase Reflow

- (1) The recommended solvent is Florinarto FC-70 or equivalent.
- (2) The atmospheric temperature should be 215 °C, within 30 seconds or 200 °C, within 60 seconds.
- (3) **Fig. 5-1** shows an example of the recommended temperature profile at V.P.S.

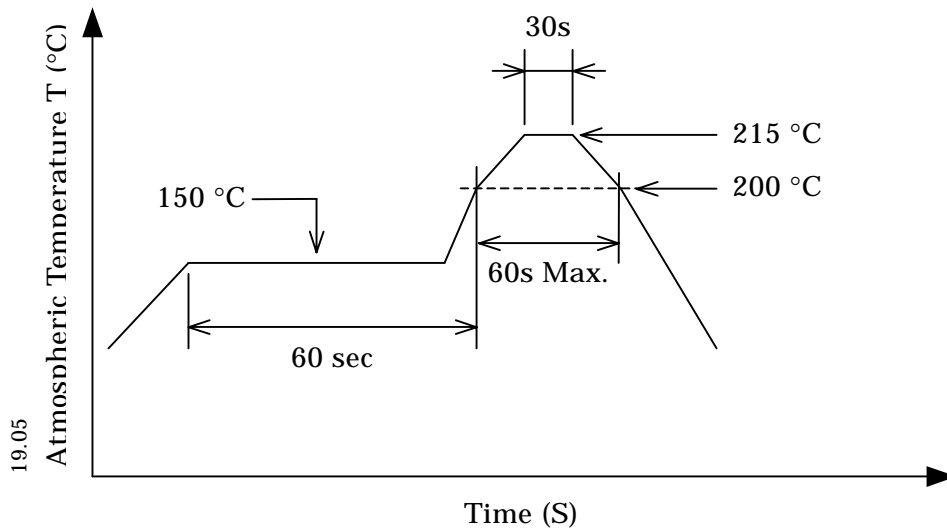


Fig. 5-1 Temperature Profile

5.1.6 In Case of Solder Dip

- (1) Perform preheating at 150 °C for 60 seconds or more.
- (2) In solder flow at up to 260 °C solder flow, perform it within 10 seconds.

5.2 Flux Cleaning (Supersonic Cleaning)

- (1) Clean properly so that reactive ions such as Na, Cl will not remain. Note that an organic solvent may react to water to produce a corrosive gas such as hydrogen chloride and deteriorate the PPMC-2104.
- (2) Do not rub the indication mark surface with a brush or hand while cleaning or with the cleaning liquid adhered to the PPMC-2104. The indication mark may be erased.
- (3) Immersion cleaning, shower cleaning, and steam cleaning depend on the chemical action of a solvent. Choose the solvent carefully. The time of immersion in the solvent or steam should be within 1 minute at the liquid temperature of 50 °C or less.
- (4) When performing supersonic cleaning which has a high cleaning effect in a short time, the following basic conditions are recommended.

Recommended Conditions for Supersonic Cleaning

- Frequency: 27 to 29 kHz
- Supersonic output: 300 W or less (0.25 W/cm² or less)
- Cleaning time: 30 seconds or less

Suspend a supersonic oscillator in the solvent so that it will not come into direct contact with the PCB or PPMC-2104.

5.3 Lead Machining

When cutting or machining the PPMC-2104 into the form of wave upon mounting it onto the PCB, an abnormal force may be applied to the inside of the PPMC-2104, destroying it mechanically or deteriorating its reliability. It is mainly caused by a relative stress applied to between the PPMC-2104 body and leads, which leads to damages on the PPMC-2104 internal leads, lower tightness, or destruction of the sealing section. Observe the following upon machining the leads.

- (1) The spacing between the insertion holes at the tip of the leads on the PCB surface should be designed identical to the lead pitch dimension of the PPMC-2104.
- (2) When the spacing between the insertion holes in the PCB does not match the lead pitch of the PPMC-2104, do not pull the leads or push the PPMC-2104 hard.
- (3) Do not put the PPMC-2104 and PCB too tight to each other. Use a spacer or for the leads to make a clearance.
- (4) Do not repeatedly bend and extend the leads.
- (5) The lead pins are sharp at their tip in order to facilitate mounting. When handling them with naked hand, be careful not to hurt yourself.
- (6) When forming the leads in advance;
 - a. Fix and bend the leads on the near side of the mold of the PPMC-2104.
 - b. Space out between the mold of the PPMC-2104 and a fixing jig.
 - c. Note that if the leads are bent along the fixing jig, they may be damaged by the corner of the jig.

5.4 Coating the Substrate

When using for the devices which require high reliability or those which are used in the bad environment (humidity, corrosive gas, dust, etc.), deliberate an effect of stress, impurities, etc. as to use of the humidity preventive coating of the PCB.

Coating resin has been chosen almost experientially out of various kinds of resins available. As it is unknown what thermal or mechanical stress is applied to the PPMC-2104. When you use the coating resin, take them into full account.

5.5 Deterioration and Destruction due to Static Discharge

When handling the PPMC-2104 alone, the worker should wear electrification preventive clothing in the environment where static electricity is not easily generated, use an electrification preventive material for the containers, etc. with which the PPMC-2104 comes into contact, and earth via a 0.5 to 1 M Ω protective resistor.

5.5.1 Controlling the Working Environment

- (1) If the humidity drops in the working environment, the human body and insulators tend to be electrified by static electricity due to friction, etc. Keep the humidity at 40 to 60 %, considering its absorption by the PPMC-2104.
- (2) Earth the equipment, jigs, etc. installed in the work area.
- (3) Spread a conductive mat on the floor in the work area to protect the floor surface against static electricity, and earth it.
- (4) Spread a conductive mat on the work bench surface to diffuse static electricity and earth it. The work bench surface should be made of anything, but metal which abruptly discharges electricity at low resistance when the PPMC-2104 comes into direct contact with it.
- (5) When using the automated equipment, pay attention to the following:
 - a. When picking up the PPMC-2104 package surface by vacuum, use conductive rubber, etc. for the tip of the pickup to prevent electrification.
 - b. Minimize the friction to the PPMC-2104 package surface. If the friction is mechanically unavoidable, reduce the friction surface or use a material with low friction coefficient or electric resistance, and ionizer, etc.
 - c. Use a static electricity dissipative material for the contact area with the lead terminals of the PPMC-2104.
 - d. Take care that a charged body (work uniform, human body, etc.) does not come into contact with the PPMC-2104.
 - e. Take care that the jigs and tools used in the processes do not come into contact with the PPMC-2104.
 - f. In the process where the PPMC-2104's package is electrified, use the ionizer to neutralize ion.
- (6) Earth the equipment, jigs, etc. installed in the work area.
- (7) Use a VDT filter, etc. to protect the CRT surface against electrification in the work area, and avoid turning it on/off as much as possible. Failure to observe this induce the electric field to the PPMC-2104.
- (8) Cover the work chair with electrification preventive fiber and earth it to the floor with an earthing chain.
- (9) Spread a static electricity preventive mat on the surface of the PPMC-2104 storage shelf.
- (10) Use a static electricity dissipative material or static electricity preventive material for the container used to transport or store the PPMC-2104 temporarily.
- (11) Install a special earthing conductor in the static electricity control area to protect against static electricity. You can use the earthing conductor for the power transmission circuit (Class-3) for that purpose, but do not use it commonly for the equipment.

5.5.2 Cautions at Work

- (1) The worker should wear static electricity preventive clothing and conductive shoes.
- (2) The worker should wear a wrist strap to earth through an about 1 M Ω resistance.
- (3) Use a soldering iron for low voltage and earth its tip.
- (4) Use static electricity preventive tweezers which may come into contact with the lead terminals of the PPMC-2104. Avoid using metallic ones as much as possible. The electrified PPMC-2104 causes abrupt discharge at low resistance. When using vacuum tweezers, use a conductive adsorptive pad on their tips and earth them to a special earthing conductor to protect against static electricity.
- (5) Do not place the PPMC-2104 or its housing container close to the high electric field generating area (on the CRT, etc.)
- (6) The PCBs with the PPMC-2104 mounted onto them should be spaced out in an electrification preventive PCB container to avoid directly piling them on each other. Failure to observe this causes friction, electrification, and electric discharge.
- (7) When you directly touch the PPMC-2104, wear static electricity preventive finger sacks, gloves, etc. as much as possible.
- (8) When the wrist strap is not available or when the PPMC-2104 is likely to be exposed to frictions, use the ionizer.

5.6 Precautions for Working Environment

5.6.1 Temperature Environment

Generally speaking, the semiconductor parts are more sensitive to the temperature than other mechanical parts. Various electrical characteristics are restricted by the working temperature. It is necessary to grasp the temperature characteristic in advance and take derating into account. Use of them beyond the assured operating temperature range may not only fail to assure the electrical characteristics, but quicken deterioration of the PPMC-2104, shortening the service life.

5.6.2 Humidity Environment

The molded PPMC-2104 is not perfectly airtight. Long-time use in the high-humidity environment may lead to deterioration or trouble of semiconductor chips due to the moisture, etc. allowed into the interior. Consider humidity preventive treatment for the PPMC-2104 surface. In the low-humidity environment, static discharge causes damages on the parts. Use the PPMC-2104 within a humidity range of 40 to 60 %, unless a special countermeasure is taken.

5.6.3 Corrosive Gas

The PPMC-2104 may react to a corrosive gas and deteriorate the characteristics. For example, a sulfide gas including sulfur such as rubber may be produced near the PPMC-2104, corrode the lead terminals, cause a chemical reaction between them, thus forming foreign substances and resulting in a leak.

5.6.4 Radioactive Rays/Cosmic Rays

The PPMC-2104 is not designed resistant to the radioactive rays or cosmic rays. In the environment where those rays are produced, therefore, it is necessary to install a shield for preventing them.

5.6.5 Strong Electric Field/Strong Magnetic Field

Exposure of the PPMC-2104 to the strong electric field may cause abnormal phenomena such as an impedance change or increased leak current due to the polarizing phenomena of the plastic materials or inside the IC chips. An electric field/magnetic field shield is required. Particularly, the AC magnetic field environment requires the magnetic shield because it produces an electromotive force.

5.6.6 Vibrations/Shocks/Stress

The plastic-sealed PPMC-2104 is designed relatively resistant to vibrations and shocks because it has internal wires secured with resin. In the actual equipment, however, a stress may be applied to the soldered section, etc. snapping the wires. Bear this in mind when the equipment is exposed to vibrations. If a stress is applied to the semiconductor chip via the package, the resistance in the chip may change due to the piezoeffect. Pay attention to the stress as well.

If a strong vibration, shock, or stress is applied, the package or chip may be cracked.

5.6.7 Dust/Oil

As with the corrosive gas, the PPMC-2104 may react chemically to the dust or oil. Use it in the environment where it is not exposed to them which have an effect on its characteristics.

5.6.8 Smoking/Ignition

The PPMC-2104 is not incombustible. If it is burned or combusted, it may smoke or be ignited, producing a toxic gas. Do not use it near a flame, heating element, or ignitable/inflammable substance.

5.7 Precautions for Designing

In order to achieve the required reliability as the customer's system, the PPMC-2104 should be used in line with the maximum ratings and recommended operating conditions. It is also necessary to pay attention to the working environmental conditions such as the ambient temperature, transient noise, surge, fully considering an effect on the PPMC-2104's reliability.

5.7.1 Observing the Maximum Ratings

The maximum ratings are the standard which should not be exceeded even momentarily; any one of them cannot be exceeded. The maximum ratings include the voltage and current of each lead terminal, storage temperature, and lead terminal temperature.

If the voltage/current of each lead terminal exceeds the maximum rating, the PPMC-2104 will be deteriorated internally due to an overvoltage or overcurrent. In a considerable case, heat generation in the internal circuit may lead to fused wiring or internal destruction of the semiconductor chip.

If the storage temperature or soldering temperature exceeds the rating, airtightness may be worsened or the bonded section may be opened due to the difference in the thermal expansion coefficients of various constituent materials of the PPMC-2104.

5.7.2 Observing the Guaranteed Operating Range

The recommended operating conditions are to assure the functioning of the PPMC-2104.

5.7.3 Treating the Unused Input/Output Terminals

If the PPMC-2104 is used with an unused input terminal left opened, input may become unstable. Do not connect the output terminals to the supply voltage (Vcc) or other output terminals.

If the PPMC-2104 is used with the unused input terminal left opened, it may pick up noise more easily, becoming unstable. It is necessary to pull up the terminal to the power source (Vcc) or connect it to Ground (GND), depending on its function.

5.7.4 Latch-up

The PPMC-2104 may have a phenomenon called latch-up due to the CMOS structure; this phenomenon allows a high current of some hundred mA or more to run between Vcc and GND, resulting in destruction.

Latch-up takes place when the input/output voltage exceeds the rating, causing a high current to run to the internal elements, or when the voltage of the power terminal (Vcc) exceeds the rating, causing the internal elements to yield.

In this case, even if application of the voltage beyond the rating is instantaneous, once the PPMC-2104 falls into the latch-up state, a high current between Vcc and GND is held and there may be a danger of heat generation or smoking. Observe the following points.

- (1) Do not raise the voltage level of the input/output terminals higher than Vcc or lower than GND. Consider the power-on timing as well.
- (2) Take care that abnormal noise is not applied to the PPMC-2104.
- (3) Secure the unused input terminal to Vcc or GND.
- (4) Do not short-circuit the output terminals.

5.7.5 Input/Output Protection

Never connect the output terminals to each other (wired theoretical configuration) because the output of the PPMC-2104 is shorted. Also, do not connect them directly to Vcc or GND.

5.7.6 Interface

When connecting a device with different input/output conditions to the PPMC-2104, malfunctioning will result if the respective levels of input V_{IL}/V_{IH} and output V_{OL}/V_{OH} do not match.

5.7.7 External Noise

If the signal lines for the input/output signals to the PPMC-2104 mounted onto the PCB are long, and noise or surge is applied to the PPMC-2104 by external induction, an overcurrent (overvoltage) may cause malfunctioning or destruction. For the noise, lower the impedance of the signal lines or insert a noise eliminating circuit, and take a protective measure against the surge.

5.7.8 Other Precautions

- (1) When designing the system, take a measure such as a fail-safe, depending on the purpose of the system, and assure system shipment such as aging treatment.
- (2) If the PPMC-2104 is placed in the high electric field, a surface leak may be caused by charge-up, resulting in malfunctioning. When using in the high electric field, take a proper measure such as shielding the package surface with a conductive shielding plate.
- (3) Take care that a conductive object (metallic pin, etc.) does not fall onto the terminals of the mounted PPMC-2104 from the outside, short-circuiting them.
- (4) The PPMC-2104 is not developed or intended for the systems (atomic power control, aviation/space devices, traffic control devices, combustion control, various safety devices, and so on) whose troubles or malfunctioning could directly endanger the human life or be hazardous to the human body. When using it for the above-mentioned systems, we will not be responsible for the resultant damages, etc.

Materials

For your information, the following pages show the circuit diagrams of the 4-axis stepper motor control module with the mounted PPMC-2104 compliant with the ISA (PC/AT) bus. The details of these circuit diagrams are provided under no warranties.

AMPERE, therefore, will assume no responsibilities for any troubles resulting