4. RATINGS

4-1. Absolute maximum ratings

The absolute ratings of PPMC-112 are as specified in Table 4-1.

Table 4-1. Table of Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +6.5	V
Input voltage	Vin	-0.5to+Vcc+0.5	V
Power consumption (Ta=85 ºC)	Pd	500	mW
Operating temperature	Topr	-40 to +85	ºC
Storage temperature	Tstg	-65 to +150	ºC
Soldering temperature (10s)	Tsolder	260	ºC

Use of PPMC-112 beyond the absolute maximum ratings may result in deterioration and permanent damage.

4-2. DC Characteristics

The DC characteristics of PPMC-112 are as shown in Table 4-2.

Table 4-2. Table of DC Characteristics

Item		Symbol	Min.	Max.	Unit	Condition
Low level input voltage	RESET	V_{IL}	-0.3	0.25Vcc	V	
	X1		-0.3	0.2Vcc		
	Other		-0.3	0.3Vcc		
High level input voltage	RESET	V_{IH}	0.75Vcc	Vcc+0.3	V	I_{OL} = 1.6mA
	X1		0.8Vcc	Vcc+0.3		
	Other		0.7Vcc	Vcc+0.3		
Low level output voltage	All output terminals	V_{OL}		0.45	V	
High level output voltage	AUXO0 - AUXO7	V_{OH}	2.4		V	I_{OH} = -400microA
	Other		0.75Vcc			I_{OH} = -100microA
Darlington Drive current		Idr	-1.0	-3.5	mA	Vext = 1.5V Rext = 1.1kohm
Input leakage current		I_{LI}	0.02 (typical)	-5 to +5	microA	0.0 to Vin to Vcc
output leakage current		I_{LO}	0.05 (typical)	-10 to +10	microA	0.0 to Vin to Vcc - 0.2
Current consumption		I_{CC}	35 (typical)	50	mA	f = 16MHz
Input capacity	All input pins	C_{IN}		10	PF	f = 1MHz

*Darlington drive current means the maximum current for driving darlington transistors by an Auxiliary output pin.

4-3. AC Characteristics

4-3-1. RD and WR separate bus mode

(1) Register read operation

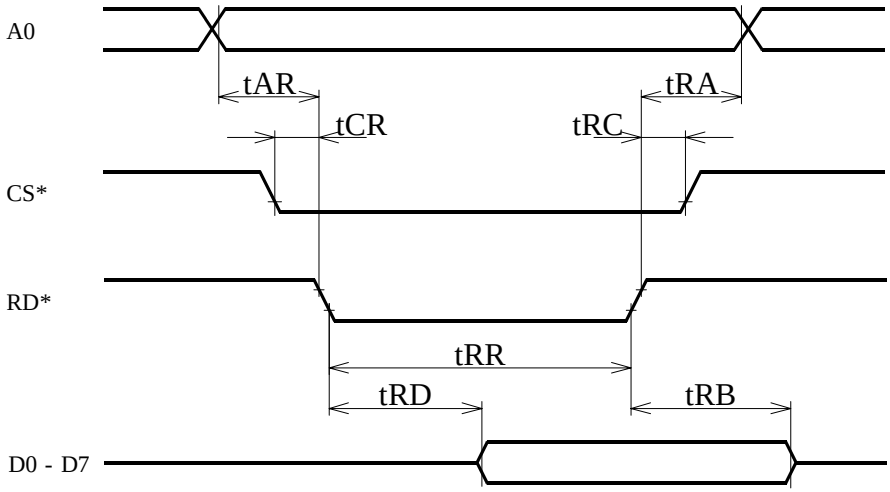


Fig.4-1. RD and WR Separate Bus Mode Register Read Timing

Table 4-3. RD and WR Separate Bus Mode Register Read Parameters

Item	Symbol	Min.	Max.	Unit
A_0 set time to RD*	t_{AR}	20		ns
A_0 hold time after RD*	t_{RA}	5		ns
CS* set time to RD*	t_{CR}	0		ns
CS* hold time after RD*	t_{RC}	0		ns
RD* pulse width	t_{RR}	120		ns
RD* to Data out delay	t_{RD}		100	ns
RD* to Data hold	t_{RB}	10	90	ns

(Vcc = +5V -10 to +10%, Ta = -20 to +70 ^{o}C)

(2) Register write operation

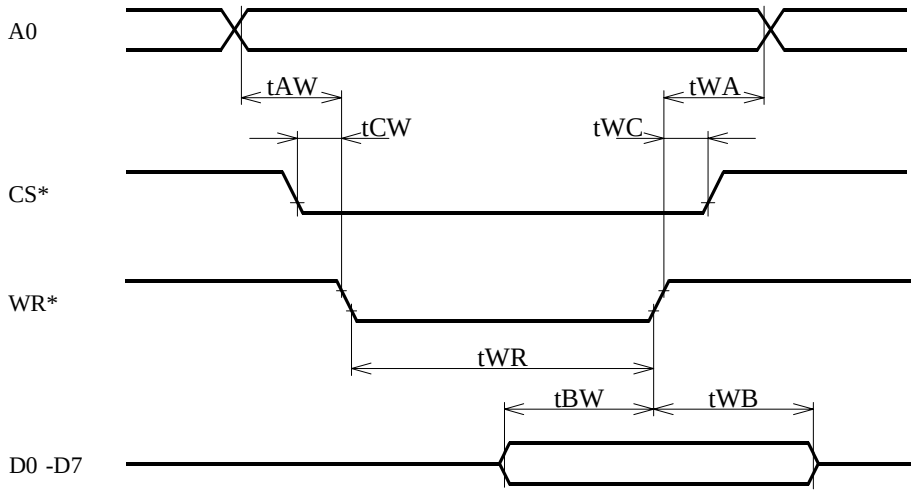


Fig.4-2. RD and WR Separate Bus Mode Register Write Timing

Table 4-4. RD and WR Separate Bus Mode Register Write Parameters

Item	Symbol	Min.	Max.	Unit
A_0 set time to WR*	t_{AW}	20		ns
A_0 hold time after WR*	t_{WA}	5		ns
CS* set time to WR*	t_{CW}	0		ns
CS* hold time after WR*	t_{WC}	0		ns
WR* pulse width	t_{WR}	120		ns
Data setup to WR*	t_{BW}	80		ns
Data hold time after WR*	t_{WB}	10		ns

(Vcc = +5V -10 to 10%, Ta = -20 to +70 ^{o}C)

4-3-2. DS* and R/W*bus mode

(1) Register read operation

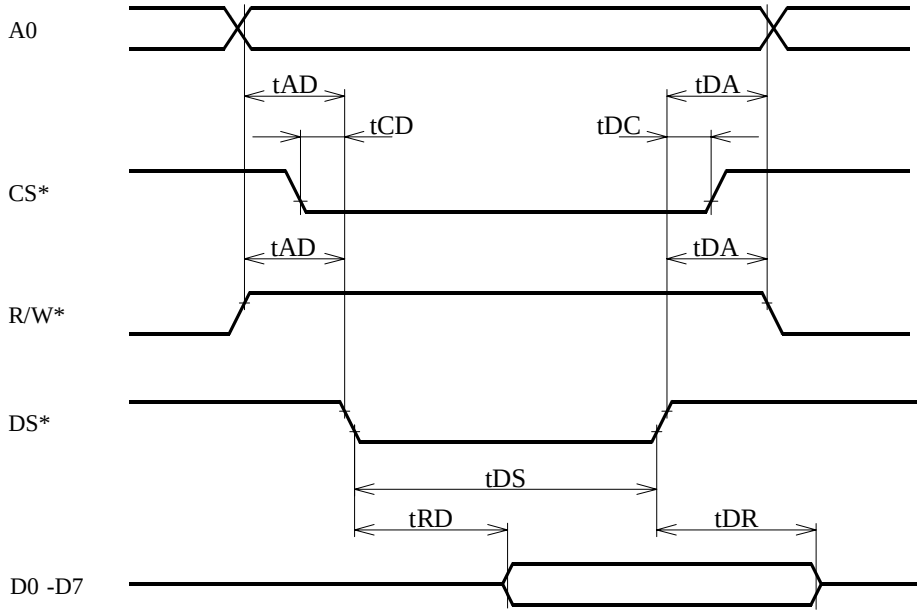


Fig.4-3. DS* and R/W* Bus Mode Register Read Timing

Table 4-5. DS* and R/W* Bus Mode Register Read Parameters

Item	Symbol	Min.	Max.	Unit
A_0, R/W* set time to DS*	t_{AD}	20		ns
A_0, R/W* hold time after DS*	t_{DA}	5		ns
CS* set time to DS*	t_{CD}	0		ns
CS* hold time after DS*	t_{DC}	0		ns
DS* pulse width	t_{DS}	120		ns
DS* to Data out delay	t_{RD}		100	ns
DS* to Data hold	t_{DR}	10	90	ns

(Vcc = +5V -10 to +10%, Ta = -20 to +70 ºC)

(2) Register write operation

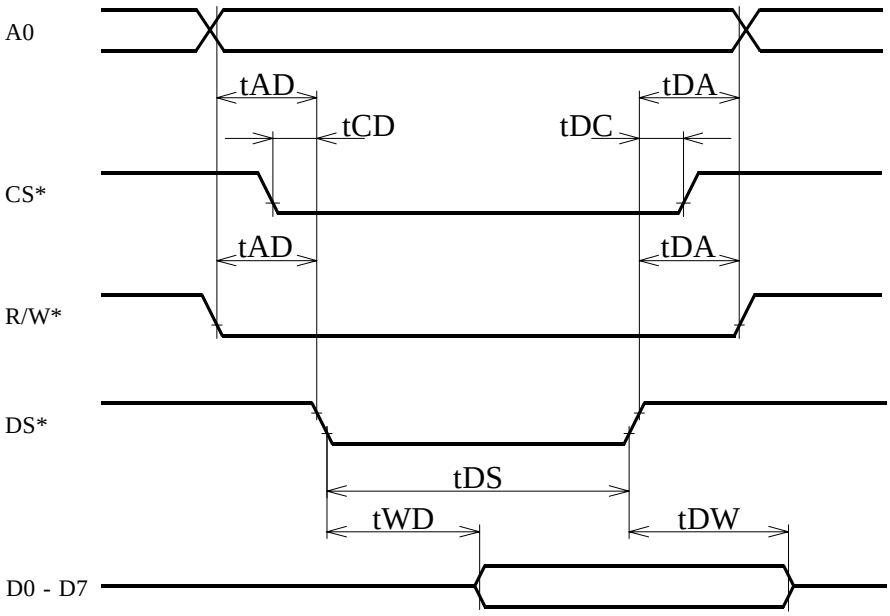


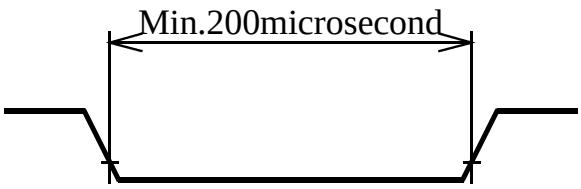
Fig. 4-4 DS*, R/W* Bus Mode Register Write Timing

Table 4-6. DS*, R/W* Bus Mode Register Write Parameters

Item	Symbol	Min.	Max.	Unit
A_0, R/W* set time to DS*	t_{AD}	20		ns
A_0, R/W* hold time after DS*	t_{DA}	5		ns
CS* set time to DS*	t_{CD}	0		ns
CS* hold time after DS*	t_{DC}	0		ns
DS* pulse width	t_{DS}	120		ns
DS* to Data input delay	t_{WD}	80		ns
Data hold after DS*	t_{DW}	10		ns

(Vcc = +5V -10 to +10%, Ta = -20 to +70 ºC)

4-3-3. Alarm and limit signal input timing



ALM*
ORG*, YORG*
FL*, FHL*, BL*, BHL*

Fig.4-5. Alarm and Limit Signal Input Timing

4-4. Outline drawing of PPMC-112AFP

[Unit : mm]

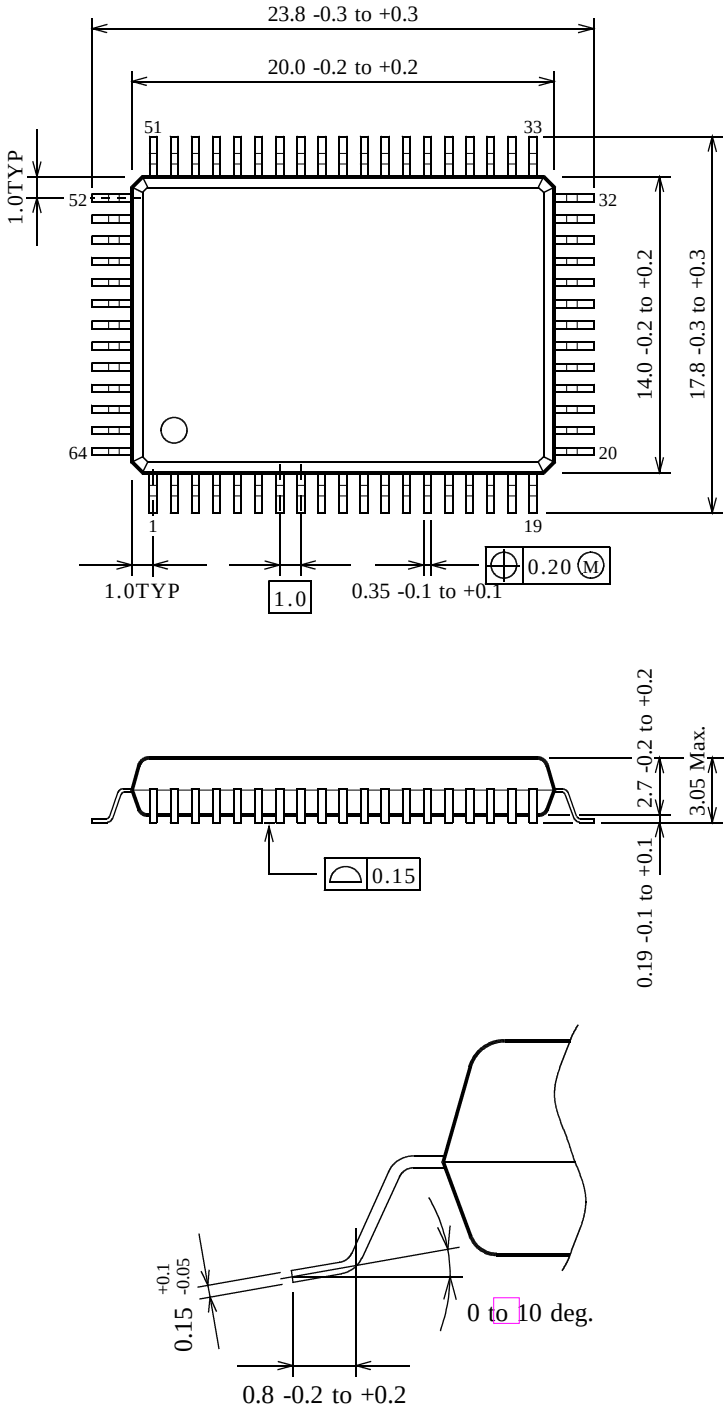


Fig.4-6. Outline Drawing of PPMC-112AFP