3 . CONTROL COMMANDS OF PPMC-112

3-1. PPMC-112 control commands in parallel mode

The PPMC-112 operates according to the command codes and data transmitted from the host processor. There are, in general, four (4) groups of commands as listed below:

(1) Initialization commands

This command is used to set the profile of an acceleration/deceleration curve and the range of operation speed. PPMC-112 must be provided with this command either following the supply of power or resetting prior to any other operations.

(2) Operation commands

These commands are used to operate the stepper motor. There are ten (10) commands, including two (2) stop commands. Some of the commands operate with command codes alone, while other commands require some bytes of data.

(3) Auxiliary commands

PPMC-112 has seven (7) data reading commands and four (4) data writing commands. Data reading commands are capable of reading the various cause of operation termination including the cause of operation termination, command error code, data on current motor position, auxiliary input data and limit switch activation, acceleration/deceleration table, and version information.

(4) SYNC-1-1 control commands

SYNC-101 start operation commands are available for limit signal inspection and direction control in the interpolation operation. In parallel mode SYNC-101accepts the command directly from the host computer. In parallel mode, the command which PPMC-112 and SYNC-101 have to execute in a coordinated way, are limited to the above stated limit detect operation and direction control signal processing.

In serial mode, all SYNC-101 control commands are fed through PPMC-112. Please refer to chapter 3, section 3-2-4 (page 3-63) for the further references.

3. CONTROL COMMANDS OF PPMC-112

Table 3-1 shows all the command set in parallel mode.

Table 3-1. Command set in parallel mode

Command		Command/data		Function
Initialization		1	00CCxxDD	CC : Base clock assigned DD : Acceleration/deceleration mode assigned xx : Invalid bits
		2	Start pulse rate (L)	Start speed rate at acceleration/deceleration operation (Normally set to self tart frequency)
		3	Start pulse rate (H)	
		4	High speed pulse rate (L)	High speed rate at acceleration/deceleration operation(Set to maximum operation speed)
		5	High speed pulse rate (H)	
		6	Acceleration/Deceleration pulse rate (L)	Set the number of pulse from start speed to high speed.
		7	Acceleration/Deceleration pulse rate (H)	
Drive command	Instantaneous stop	1	10xI0000	Immediately stop the pulse output I: Termination interrupt assigned
	Decelerate and stop	1	10xI0001	Decelerate to start speed and stop
	Single step	1	10DI0010	Output single pulse to the designated direction. D: Drive direction
	Acceleration/ deceleration operation	1	10DI0011	Accelerate/decelerate from start speed to high speed. D: Drive direction I: Termination interrupt assigned (0=interrupt assigned) Number of drive pulse is assigned in 3 bytes Input data from lower byte and up in order
		2	Drive pulse number (L)	
		3	Drive pulse number (M)	
		4	Drive pulse number (H)	
	Constant speed operation	1	10DI0100	Accelerate/decelerate from start speed to high speed. D: Drive direction I: Termination interrupt assigned (0=interrupt assigned) Pulse rate is assigned in 2 bytes. Number of drive pulse is assigned in 3 bytes Input data from lower byte and up in order.
		2	Constant pulse rate (L)	
		3	Constant pulse rate (H)	
		4	Drive pulse number (L)	
		5	Drive pulse number (M)	
		6	Drive pulse number (H)	
	Continuous constant speed	1	10DI0101	Constant speed drive till limit at assigned speed D: Drive direction I:Termination interrupt assigned (0=interrupt assigned) Pulse rate is assigned in 2 bytes.
		2	Constant speed pulse rate (L)	
		3	Constant speed pulse rate (H)	
	Continuous high speed	1	10DI0110	Decelerate and stop following accelerating/decelerating operation, or high speed limit detection

Command		Command/data		Function
Drive Command	Constant speed origin search	1	10DI0111	Constant speed drive at assigned speed to the origin point. D: Drive direction I: Termination interrupt assigned(0=interrupt assigned)
		2	Constant pulse rate (L)	
		3	Constant pulse rate (H)	
	Instantaneous speed change	1	10001000	Changes to the assigned speed immediately Target pulse rate is assigned in 2 bytes.
		2	Target pulse rate (L)	
		3	Target pulse rate(H)	
	Acceleration/ deceleration speed change	1	10001001	Accelerate/decelerate to the assigned speed. Target pulse rate is assigned in 2 bytes.
		2	Target pulse rate (L)	
		3	Target pulse rate (H))	
	Finish status	1	01000000	Read finish status register.
	Error code	1	01000001	Read error code register.
	Current position reading	1	01000010	Read finish position data (returns 3 bytes code)
	Current position setting	1	01000011	Set the current position Current position is set in 3 bytes. Input data from lower bytes in order.
		2	Current position (L)	
		3	Current position (M)	
		4	Current position (H)	
Auxiliary Command	Auxiliary input	1	01000100	Read auxiliary input port status.
	Auxiliary output	1	01000101	Change auxiliary output port status. Input 1 byte of output bit patter.
		2	Auxiliary output data	
	Control input	1	01000110	Read status of control input port (limit signal)
	High speed limit effective speed setting	2	Effective speed rate (L)	Set the effective speed for the high speed limit. Effective speed is assigned in 2 bytes. Input data from lower bytes in order.
		3	Effective speed rate (H)	

Command		Command/data		Function
Auxiliary Command	Interlock position setting	1	01001000	The interlock release position is set with the number of pulse from starting position. When it reaches to assigned value interlock signal changes to "H." Position is set by 3 bytes data inputting from lower byte in order.
		2	Interlock release position (L)	
		3	Interlock release position (M)	
		4	Interlock release position (H)	
	Acceleration/ deceleration table reading	1	01001001	Read accelerate/decelerate data table.
	Version reading	1	01001010	Read version code.
	Pulse width setting	1	01001011	Pout output pulse width setting.
		2	Pulse width	

3-1-1. Host interface registers

PPMC-112 has four (4) registers listed below. These registers are used for the input/output of commands and/or data. Table 3-2 shows their access conditions.

Table 3-2. Host interface register

Name of Register	CS	A_0	RD	WR	Read/Write
Disable	H	x	x	x	Disable
Data Register	L	L	L	H	Read
Status Register	L	H	L	H	Read
Data Register	L	L	H	L	Write
Command Register	L	H	H	L	Write

3-1-1-1. Status register

Status register is a read-only register that indicates the internal conditions of PPMC-112. These internal conditions can be read at any time. Fig. 3-1 shows the bit configuration.

<Status register>

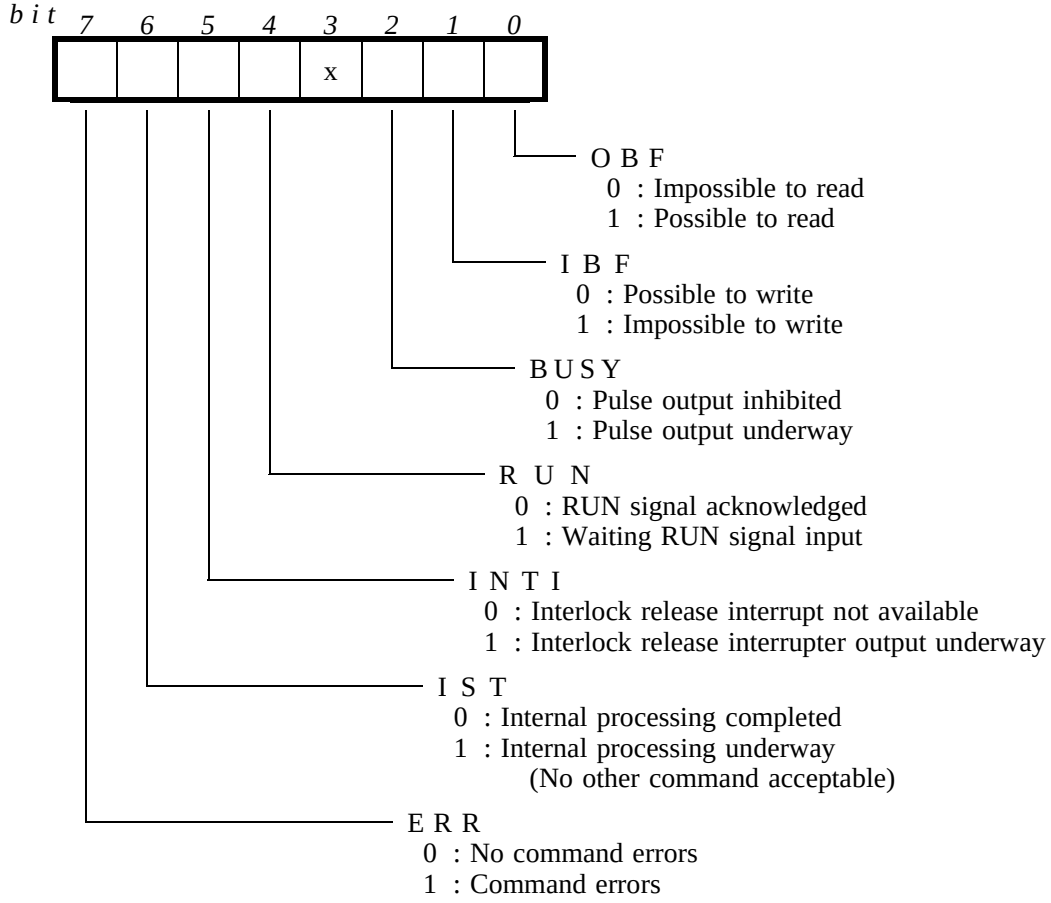


Fig.3-1. Status register bit configuration

(1) OBF : Output Buffer Full Flag

This bit enables checking whether it is ready to read data from PPMC-112. Data must be read after making certain that OBF indicates "1". Data read is void if OBF shows "0".

(2) IBF : Input Buffer Full Flag

This bit enables checking whether it is ready to write commands or data to PPMC-112. Data cannot be written if the IBF bit is "1". Commands and data must be written after making certain that IBF indicates "0". Entry of commands or data when the IBF bit shows "1" deletes previously written commands and data.

(3) BUSY: Motor Busy

The BUSY bit indicates "1" when PPMC-112 is engaged in pulse output (i.e., when the motor is rotating). No command other than the stop command, speed change command, status read command, error code read command and auxiliary output command can be accepted when the BUSY bit indicates "1".

This BUSY bit, as well as the IBF bit, must be checked when writing a command.

(4) RUN : RUN Signal

If this bit indicates "1", the RUN input signal of PPMC-112 is "L", and it is impossible to send any pulse output. When the RUN bit indicates "0", BUSY bit is to set, thus the operation will start.

This bit indicates the output of interrupt signal following the termination of pulse output on PPMC-112.

(5) INTI : INT by Inter lock Release

This bit indicates the output of interrupt signal by interlock release. If the INTE bit reads "1," the interrupt signal (INT) is being output by reaching to the interlock release. The INTI bit indicates "0" upon issuing the termination status read command (Section 3-4-2). In this case, the status to be read will be "00h"

(6) IST : Internal Status Flag

This bit indicates the progress of processing of command. The IST bit shows "1" if any command code is written in PPMC-112. The bit changes to "0" when data has been written according to the command code and the internal processing has been completed.

It is necessary to make sure that the IST bit indicates "0" before issuing the first command code to PPMC-112.

In issuing a command which requires the setting of data, such as the pulse rate and operation pulse number (number of operating pulses), command error (Error No.7) occurs if, following the entry of that command code, another command code is written without writing the necessary data.

(7) ERR : Error Flag

This bit enables checking for any error in the command codes or data furnished by the host processor.

Checking this bit after the internal processing (IST bit of status register = 0) is completed following the issuing of each command enables the detection of an error in the command codes or data issued.

"0" indicates no errors. "1" shows the existence of an error. This bit shows "0" if the command given next is correct. This bit is to be set to "0" following the next command code writing. More information on the error can be read through the identification of the error number by issuing the command error code read command (Section 3-1-4-2). Command error codes and their descriptions are shown in table 3-3.

Table 3-3. Command error codes in parallel mode

Error Code		Descriptions of Error
Decimal	Hexadecimal	
0	0 0	No errors.
1	0 1	Command error not defined.
2	0 2	No initialization command provided.
3	0 3	Not operable due to limit signal or alarm signal.
4	0 4	Not operable as moving quantity is zero.
5	0 5	Stop/Decelerating stop/Speed command received while at stop.
6	0 6	Received data not preceded by command.
7	0 7	Received command code while waiting for data.
8	0 8	Not operable as being on origin for origin search command.
9	0 9	Received the command, which is unable to process during BUSY status.
10	0 A	Abnormal pulse rate of initialization command (Starting pulse rate must be 25 or over, high speed pulse rate must be 8 or over), Alternatively external mode pulse rate initialization error.
11	0 B	Excessively small pulse number(acceleration/deceleration pulse number at the time of initialization must be 8 or over).
12	0 C	Abnormal pulse rate at the time of initialization (RH = RL or RH > RL).
13	0 D	Abnormal steps of acceleration/deceleration in performed initialization command for the free-curve acceleration/deceleration method.
14	0 E	Received speed change command while decelerating due to detection of limit.
15	0 F	Received decelerating stop command while decelerating.
16	1 0	Designation of abnormal speed range (> RL, < RH).
17	1 1	Pulse width setting is "0", or larger than high speed pulse width.
18	1 2	Not being able to control due to excessively interlock release setting (< 20).
20	1 4	Acceleration/deceleration impossible speed range as speed range is out of acceleration/deceleration speed range.

3-1-1-2. Data register (at read)

This register is used to read the data that is readable by status read command. Data must be read by referring to the OBF bit of the status register. More information is provided in Section 3-1-4 (Register read command).

3-1-1-3. Command register (write only)

This register is for writing the command code for each command, including the initialization command, operation command, status read command, auxiliary command, etc. Writing can only be done when the IBF bit of the status register indicates "0".

3-1-1-4. Data register (at write)

This register is for writing, after writing each command code, the data necessary for each command (e.g., pulse rate, operation pulse, etc.) Writing can only be done when the IBF bit of the status register reads "0". Information on the order of writing is provided in the section discussing each command. Upon completion of the writing of the necessary data, PPMC-112 performs the necessary internal processing and then, if the RUN terminal indicates "H", operates according to the command/data.

3-1-2. Initialization commands

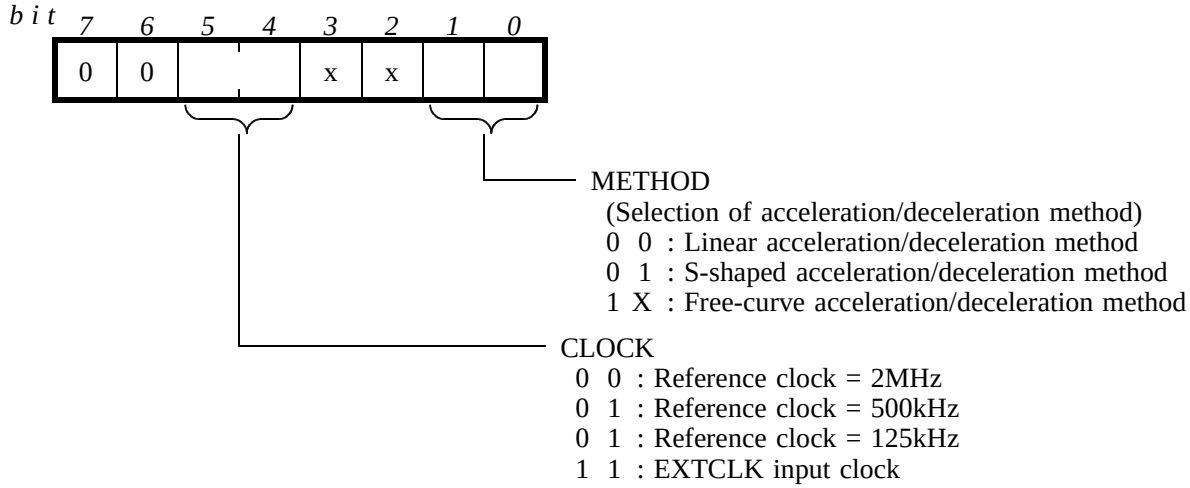
When operating PPMC-112, upon power on or resetting, the host processor is required to first issue to PPMC-112 an initial setting command.

The acceleration/deceleration method and base clock speed are chosen and conveyed in the form of an initialization command code.

If the linear acceleration/deceleration method or S-shaped acceleration/deceleration method is chosen, data necessary for acceleration/deceleration operations (i.e., number of acceleration/deceleration steps, pulse rate and pulse number of each acceleration/deceleration step) are automatically generated inside PPMC-112 by setting three (3) sets of data, namely, the starting pulse rate, pulse rate at high speed and acceleration/deceleration pulse number (number of acceleration/deceleration pulses).

If the free-curve acceleration/deceleration method is chosen, all the data necessary for acceleration/deceleration operations (i.e., number of acceleration/deceleration steps, as well as the pulse rate and pulse number for each acceleration/deceleration step) must be provided via the host processor.

<Initialization command code>



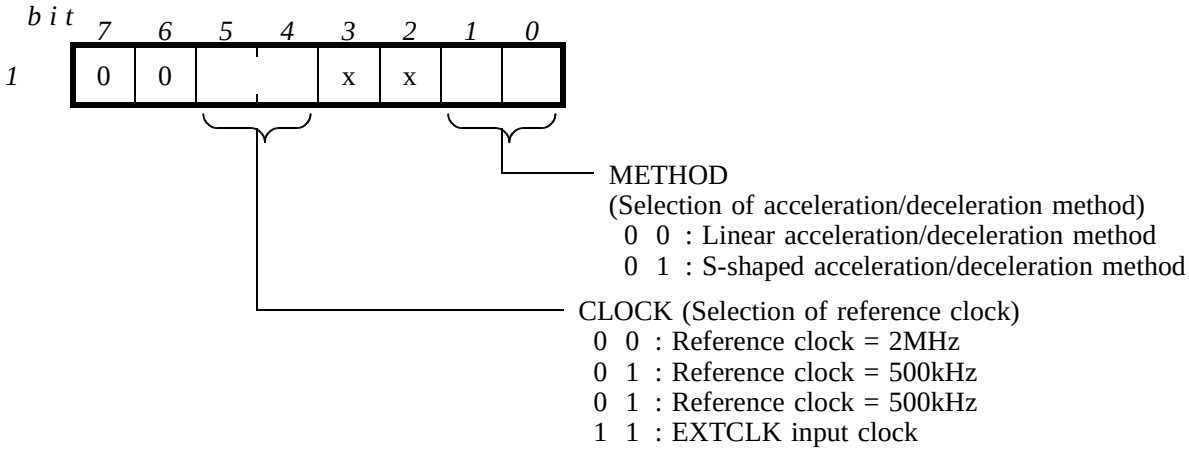
x indicates inefficacy

Fig.3-2

3-1-2-1. Initialization command for linear/ S-shaped acceleration/deceleration method

In performing an initialization command for the linear or S-shaped acceleration/deceleration method, three (3) sets of data, namely, the starting pulse rate, pulse rate at high speed and acceleration/deceleration pulse numbers, shall be fed after the command code.

<Initialization command code for linear/S-shaped acceleration/ deceleration method>



x indicates inefficacy

<Initialization data for linear/S-shaped acceleration/ deceleration method>

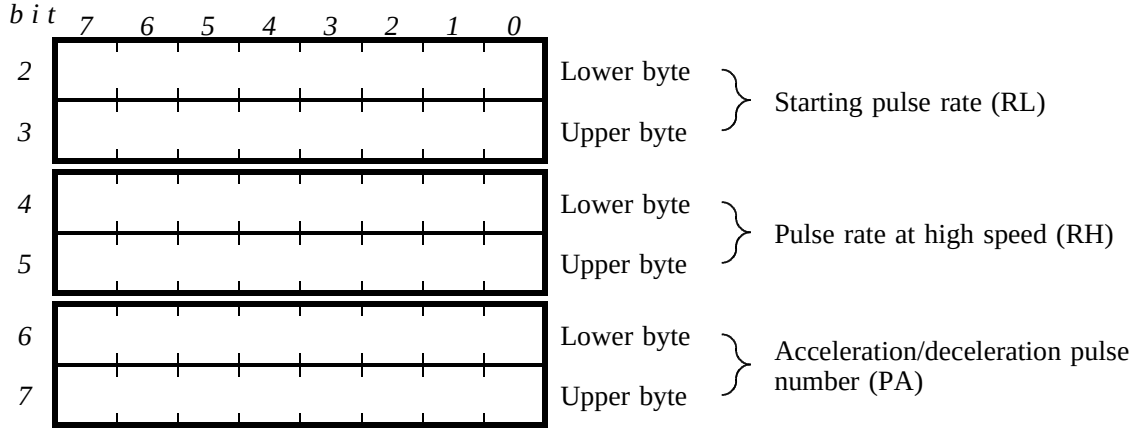


Fig.3-3

Initialization command for the linear or S-shaped acceleration/deceleration method shall be carried out by writing command codes and data in the order numbered on the left side of Fig. 3-3. Fig. 3-6 shows the same information transformed into a flow chart.

The starting pulse rate, pulse rate at high speed and acceleration/deceleration pulse number shall be provided in the form of 16-bit data, while each datum shall be divided into upper and lower bytes and the lower byte data shall be provided first.

Equations 3-1 and 3-2 show the correlation between the starting pulse rate, pulse rate at high speed and pulse output speed. Figures 3-4 and 3-5 show the correlation between each datum and acceleration/deceleration operation.

$$SH \quad \frac{Tclock}{RH} \qquad \text{-----Equation 3-1}$$

SH : High speed (ppS)
RH : Pulse rate at high speed
Tclock : Reference clock

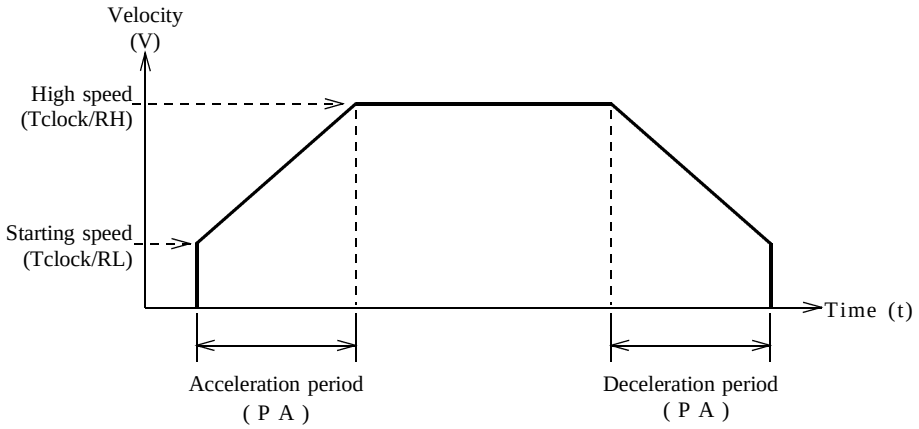
$$SL = \frac{Tclock}{RL} \qquad \text{----- Equation 3-2}$$

SL : Starting speed (ppS)
RL : Starting pulse rate
Tclock: Reference clock

Table 3-4 shows the correlation between the pulse output speed range and reference clock of PPMC-112 based on the equations above.

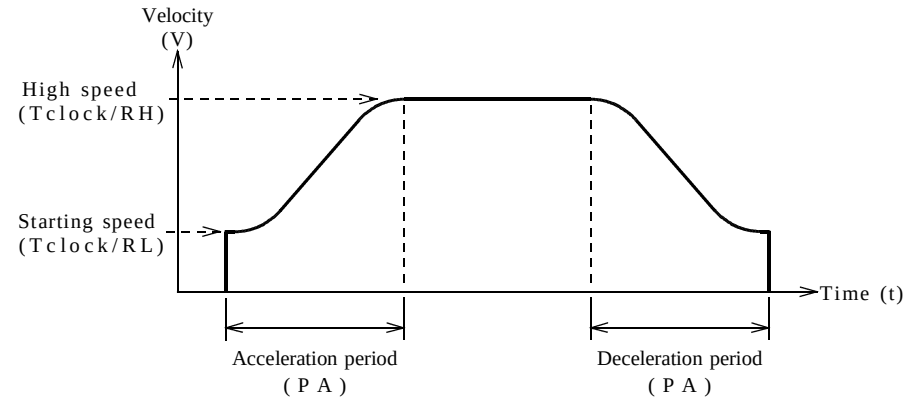
Table 3-4. Reference clock and pulse output speed range

Reference clock (Tclock)	Pulse output speed range
2MHz	30.5ppS - 250kppS
500kHz	7.63ppS - 62.5kppS
125kHz	1.91ppS - 15.6kppS



(Acceleration/deceleration operation by linear acceleration/deceleration method)

Fig. 3-4. Correlation between initialization command data and acceleration/ deceleration operation



(Acceleration/deceleration operation by S-shaped acceleration/deceleration method)

Fig. 3-5. Correlation between initialization command data and acceleration/ deceleration operation

The value of available pulse rate is subject to the restrictions represented in equations 3-3 and 3-4. Failure to satisfy these conditions results in a command error, providing error No.10. If equation 3-5 is not satisfied, error No.12 is provided.

RL = 25 (0019h) to 65,535 (FFFFh) ----- Equation 3-3
RH = 8 (0008h) to 65,534 (FFFEh) ----- Equation 3-4
RH < RL ----- Equation 3-5

Acceleration/deceleration pulse number refers to the number of operation pulses delivered during the acceleration or deceleration period. The set number as acceleration/deceleration pulse number tells how many pulses it requires from booting (start of pulse output) to the high speed or how many pulses it requires from the start of deceleration to the final stop.
The value of available pulse number is subject to the restrictions represented in equation 3-6. Failure to satisfy this condition results in a command error, providing error No.11.
In case of RH < 15, even PA=8, there are occasions that error No. 11 is to be issued. If this happens, please set the PA larger.

PA = 8 or over ----- Equation 3-6

PA : Acceleration/deceleration pulse number

Fig. 3-6 is a flow chart indicating the flow of issue of initialization command for the liner or S-shaped acceleration/deceleration method.

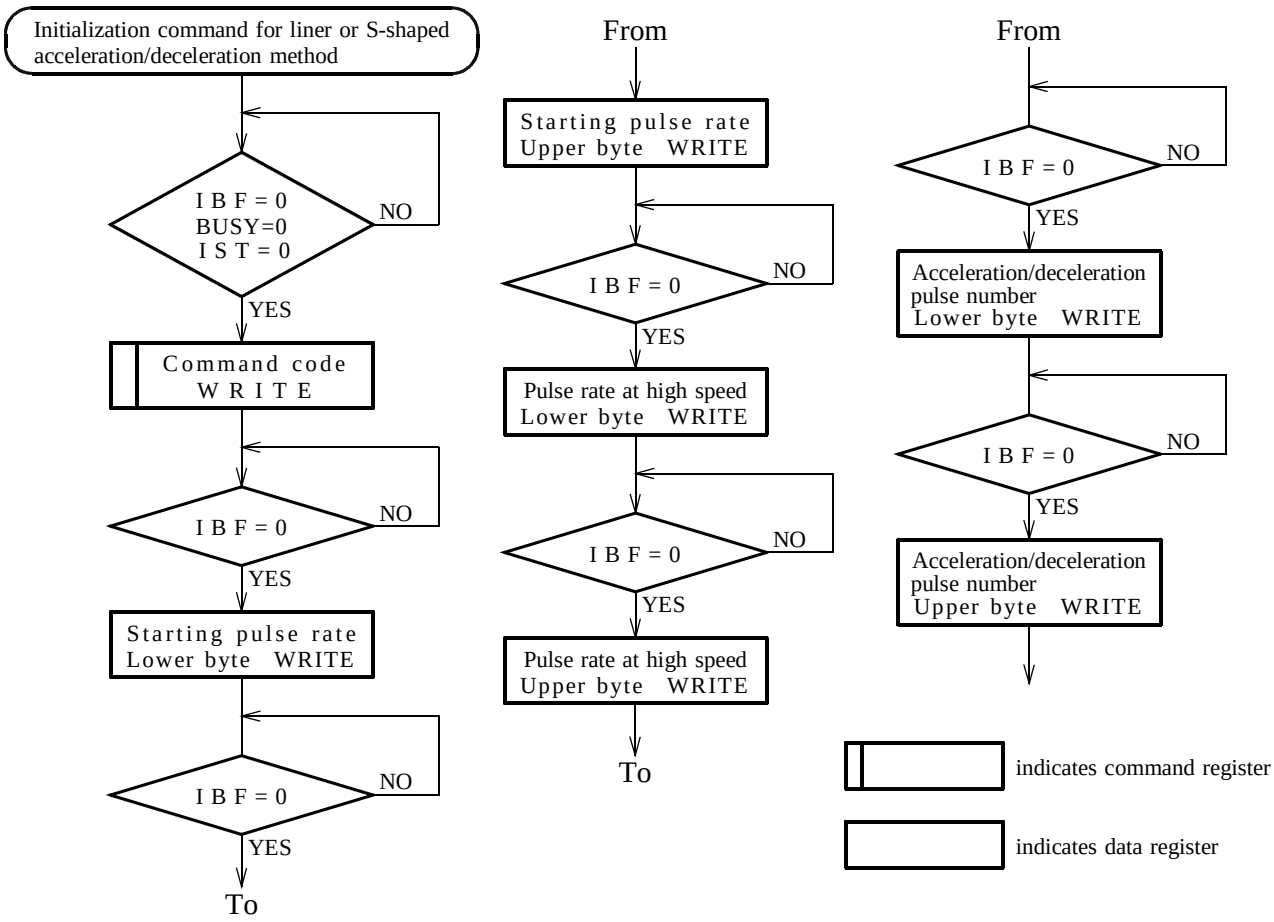
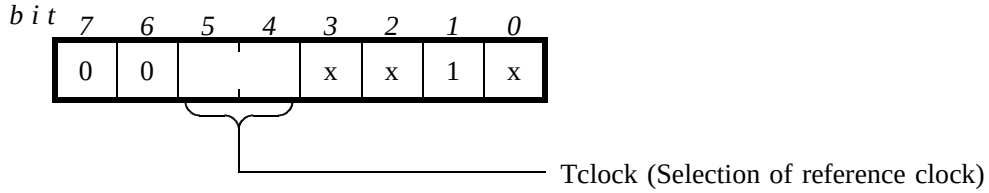


Fig.3-6. Flow Chart of initialization command for linear or S-shaped acceleration /deceleration method

3-1-2-2. Initialization command for free-curve acceleration/ deceleration method

In performing initialization command for the free-curve acceleration/deceleration method, all data necessary for acceleration/deceleration operations must be fed via host processor after the instruction code. Specifically, the number (N) of acceleration/deceleration steps, pulse rate at high speed, pulse rate [R (n)] for each acceleration/deceleration step, and pulse number [S (n)] for each acceleration/deceleration step shall be defined and fed into PPMC-112.

<Initialization command code for free-curve acceleration/ deceleration method>



Tclock (Selection of reference clock)
0 0 : 2MHz
0 1 : 500kHz
1 0 : 125kHz
1 1 : EXTCLK input clock

x indicates inefficacy

<Initialization data for free-curve acceleration/deceleration method>

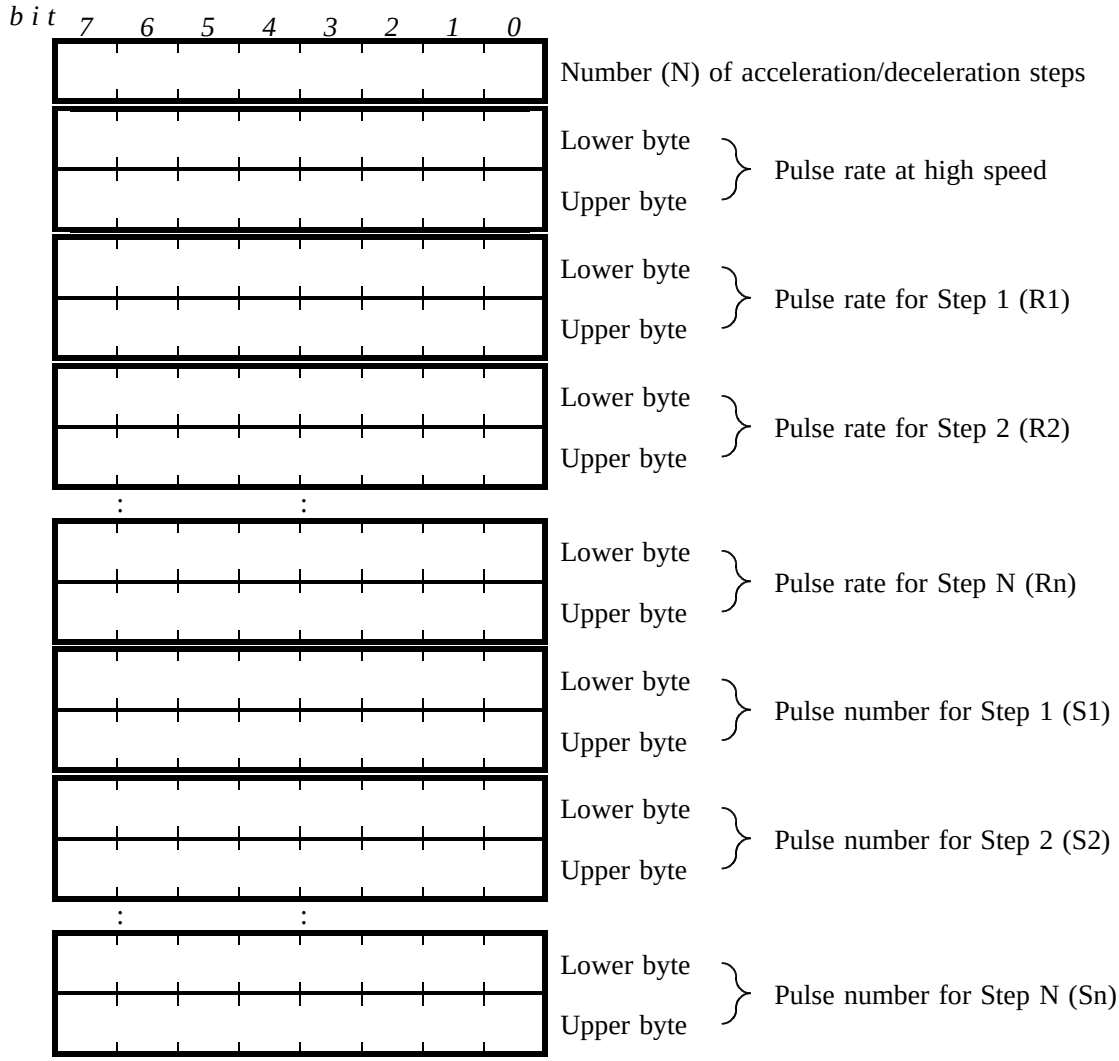


Fig.3-7

The value of the number (N) of acceleration/ deceleration steps, pulse rate [R (n)] for each acceleration/ deceleration step, and pulse number [S (n)] for each acceleration/deceleration step are subject to the restrictions represented in equations 3-7, 3-8 and 3-9.

Number (N) of acceleration/deceleration steps

N = 2 to 96 ----- Equation 3-7

Pulse rate [R (n)] for each acceleration/deceleration step

R (n), RH = 20 or over Equation 3-8

Pulse number [S (n)] for each acceleration/deceleration step

S (n) = 2 or over----- Equation 3-9

In general, relatively smooth acceleration/deceleration operation can be achieved by having small incremental speed change settings for the period immediately after booting and immediately before reaching high speed.

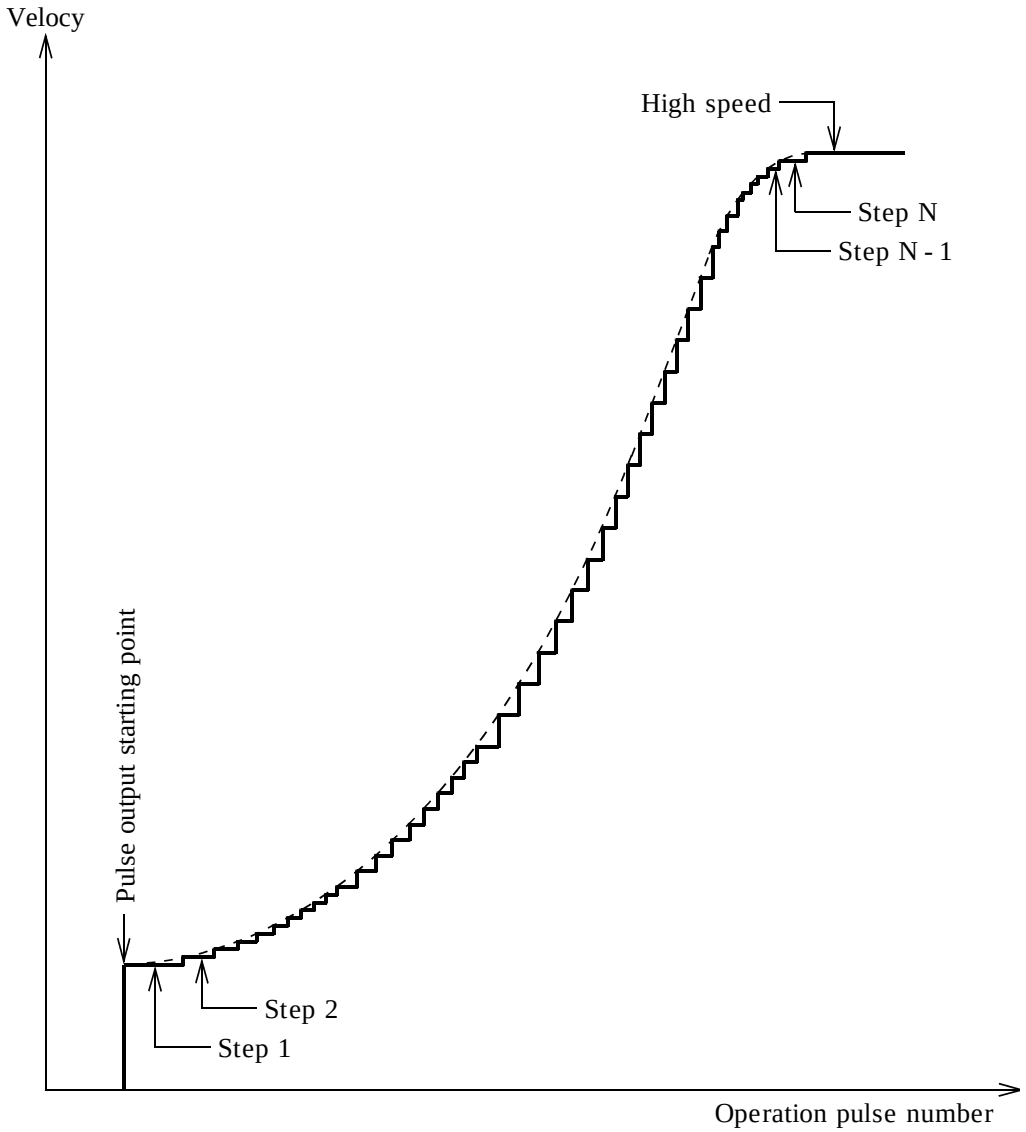


Fig.3-8. Sample acceleration curve at the time of initialization by free-curve acceleration/deceleration method

Fig.3-9 is a flow chart indicating the flow of issue of initialization command for the free-curve acceleration/deceleration method.

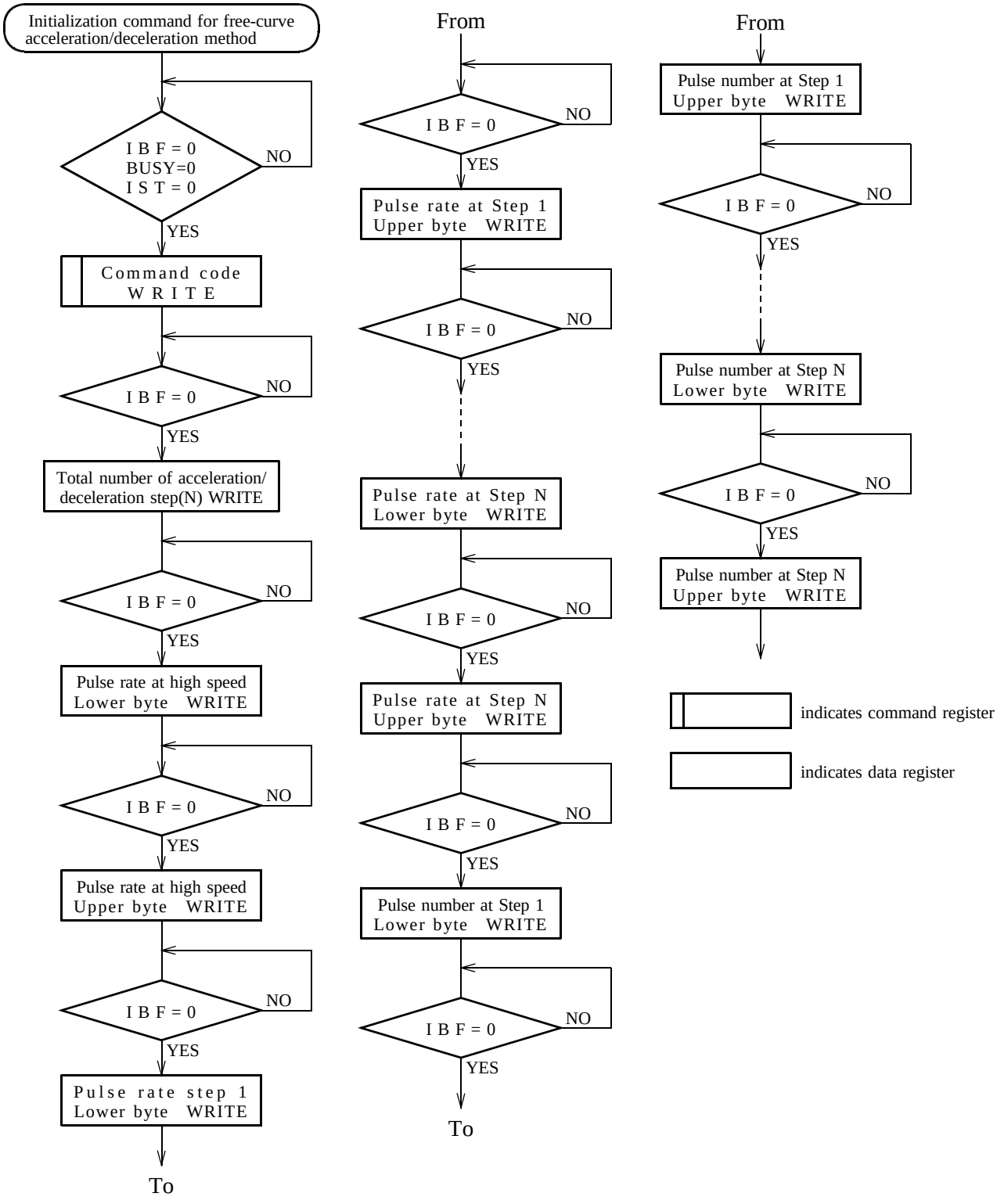


Fig.3-9. Flow chart of initialization command for free-curve acceleration/deceleration method

3-1-3. Operation command

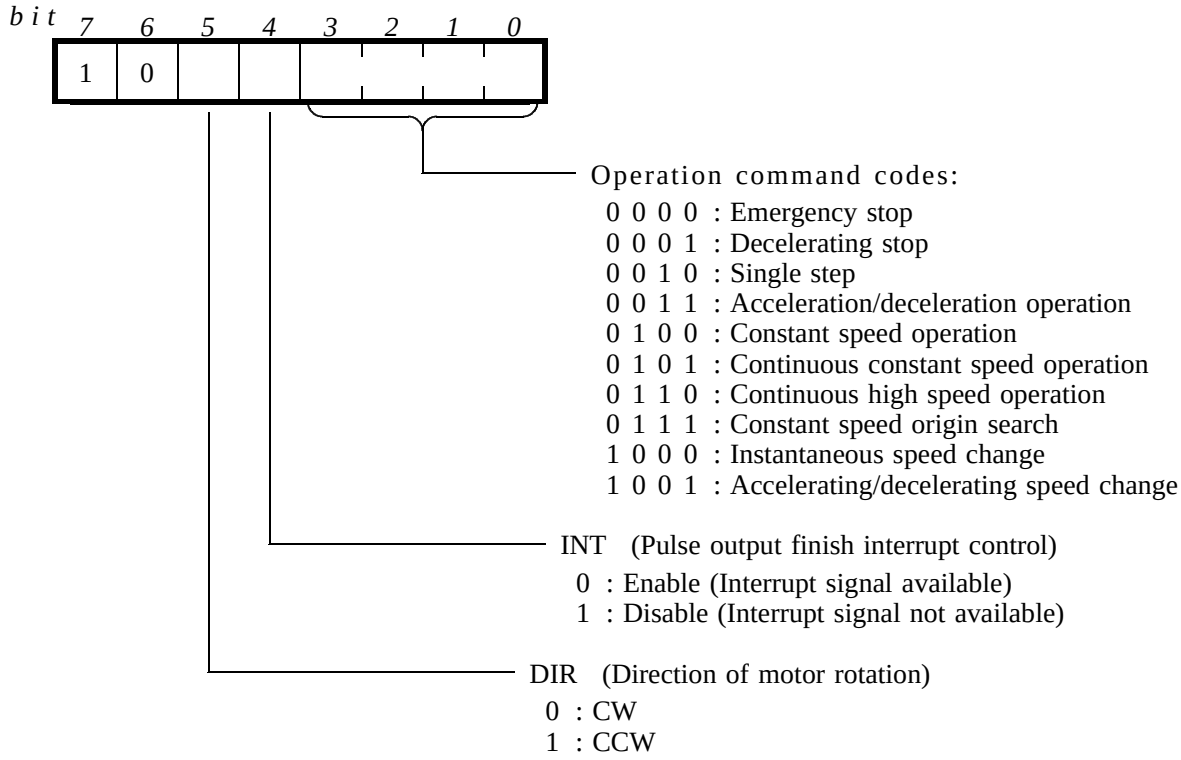


Fig.3-10. Bit configuration of operation command code

3-1-3-1. Emergency stop

Immediately upon receipt of this command during acceleration/deceleration operation or constant speed operation, PPMC-112 stops pulse output. Administration of this command when the stepper motor is operating in a speed range higher than its self-boot range may result in being out of step most likely due to inertia from the motor load.

If the INT bit of this command is "0," the interrupt signal (INT*) is output upon termination of pulse output. The DIR bit (direction of motor rotation) has no meaning to this command.

This command only carries a command code and carries no data. This command is significant only during pulse output (Busy = 1); therefore, this command must be written only after the status register's IBF and IST bits, as well as the BUSY bit, are checked.

This command must be used carefully because PPMC-112 is unable to detect any control input signals, including limit signals, from the start of receiving this command code (IST bit = "1") to the termination of pulse output (IST bit = "0").

<Emergency stop command>

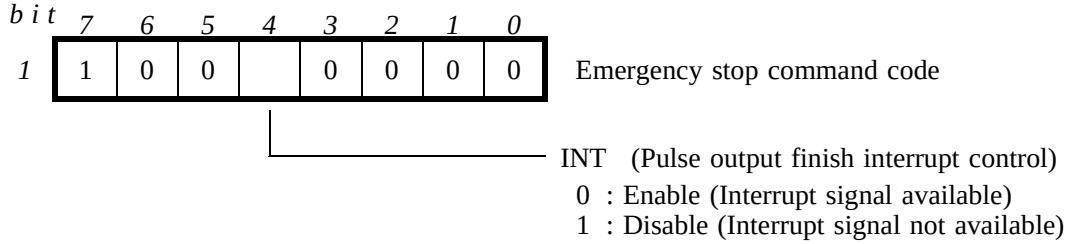


Fig. 3-11

Fig. 3-12 is a flow chart indicating the flow of issue of emergency stop command.

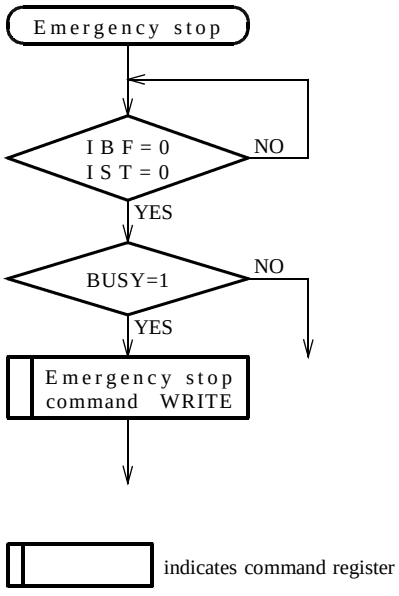


Fig.3-12. Flow chart of emergency stop command

3-1-3-2. Decelerating stop

Immediately upon receipt of this command, PPMC-112 starts deceleration and completes pulse output at the starting speed. The interrupt signal (INT*) is output if the INT bit of this command reads "0".

If the operation speed at the receipt of this command is equivalent to the starting speed, which was designated at the time of initialization, it immediately stops without deceleration. The DIR bit (direction of motor rotation) is meaningless with this command. This command only carries a command code and carries no data.

This command is significant only during pulse output (Busy = 1); therefore, this command must be written only after the status register's IBF and IST bits, as well as the BUSY bit, are checked.

This command must be used carefully because PPMC-112 is unable to detect any control input signals, including limit signals, from the start of receiving this command code (IST bit = "1") to the termination of pulse output (IST bit = "0").

<Command for decelerating stop>

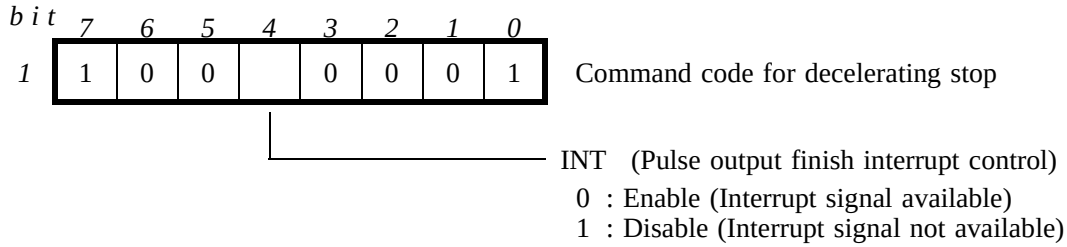


Fig.3-13

Fig.3-14 is a flow chart indicating the flow of issue of command for decelerating stop.

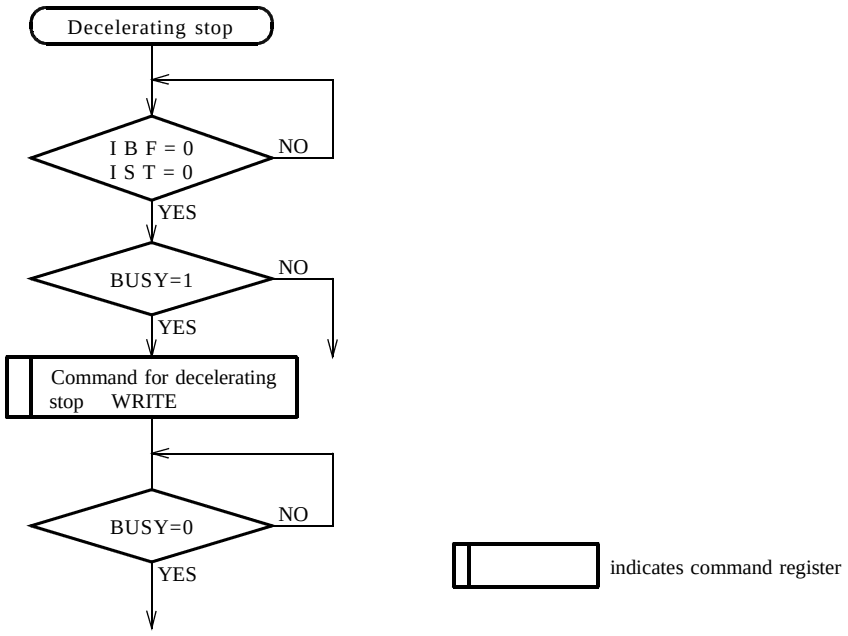


Fig.3-14. Flow chart of command for decelerating stop

3-1-3-3. Single step

This command enables movement in an increment/decrement of a single pulse by a command transmitted from the host processor. This command is used when the host processor itself intends to check the position. The timing, etc. of execution of this command must be processed on the host processor if this command must be used continually. This command does not check any RUN signals.

This command only carries a command code and carries no data. This command must be written only after the status register's IBF and IST bits, as well as the BUSY bit, are checked.

<Single step operation command>

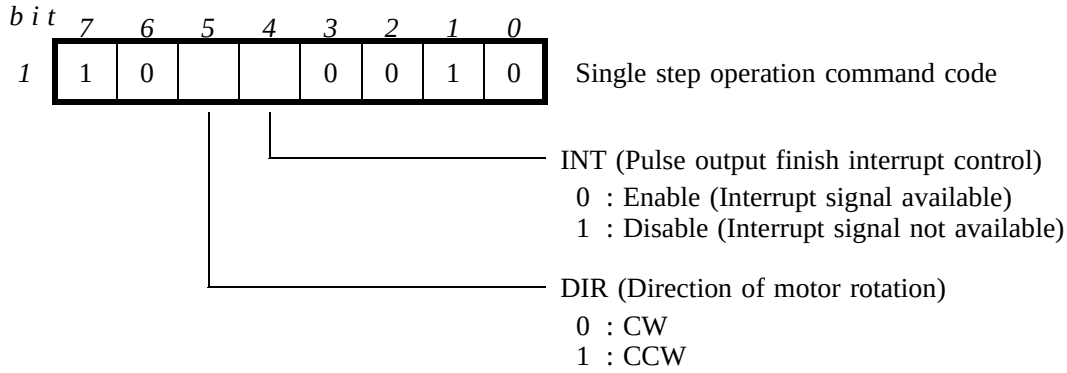


Fig.3-15

Fig.3-16 is a flow chart indicating the flow of issue of single step command.

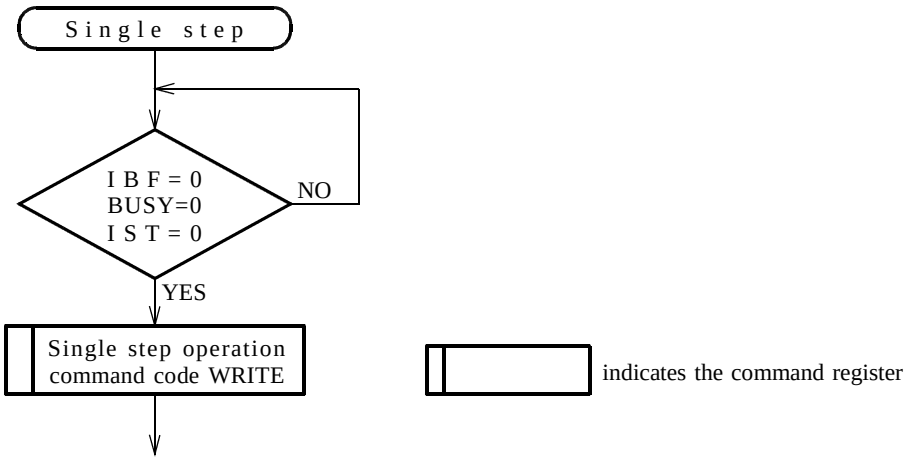


Fig.3-16. Flow chart of single step operation command

3-1-3-4. Acceleration/deceleration operation

This command is for acceleration/deceleration operation according to the acceleration/deceleration curve set at the time of initialization together with the command. Designation of a 3-byte-operation pulse number is required together with the command. Upon receipt of this command, PPMC-112 begins pulse output at the starting speed designated at the time of initialization. PPMC-112 accelerates up to high speed with the designated acceleration/deceleration pulse number. After high speed operation, once it reaches the point where deceleration begins, deceleration occurs with the designated acceleration/deceleration pulse number down to the starting speed where pulse output completes. Setting an operation pulse number smaller than a value twice the designated acceleration/deceleration pulse number leads to the formulation of triangle operation in which deceleration begins in the middle of acceleration. If the INT bit is set at "0," the interrupt signal (INT*) will be available upon termination of pulse output.

This command must be written only after the status register's IBF, BUSY and IST bits are checked. An operation pulse number must be written while confirming the IBF bit.

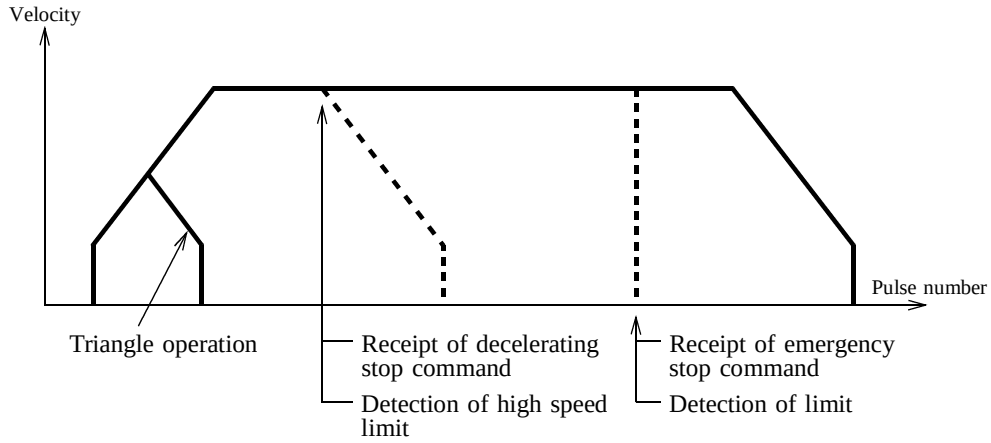


Fig.3-17. Sample acceleration/deceleration operation

<Acceleration/deceleration operation command/data>

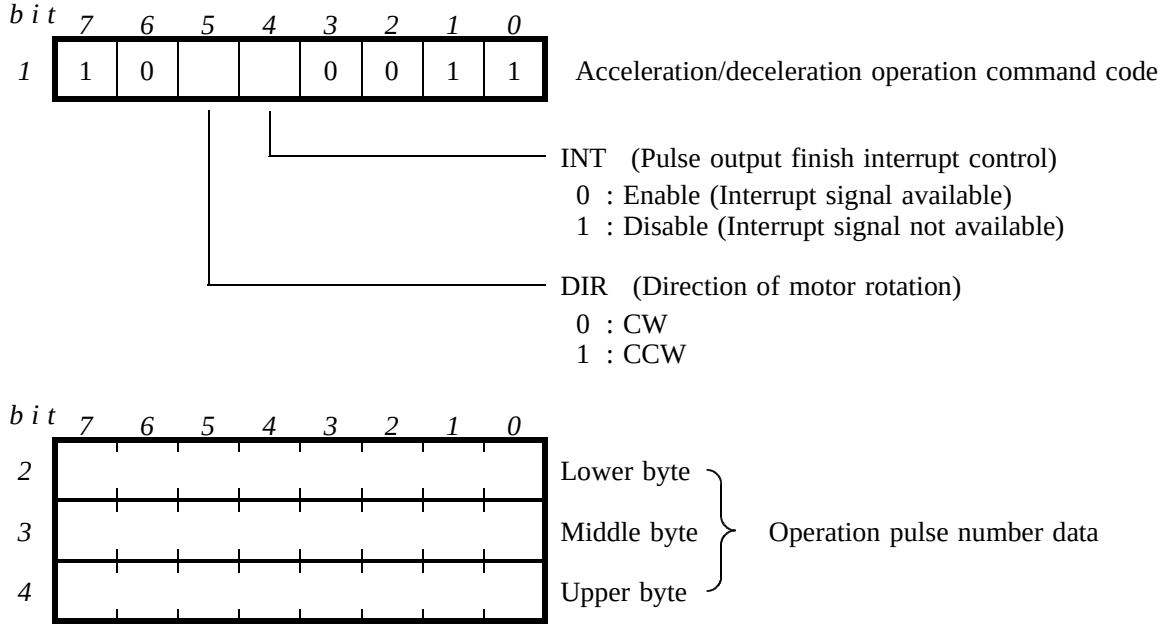


Fig.3-18

Fig. 3-19 is a flow chart indicating the flow of issue of acceleration/deceleration operation command.
In a triangular driving mode, the internal calculation algorithm can take up to around 300 microsecond to seek the deceleration starting point. In this case, the calculation time would be proportionally longer as the number of steps in the acceleration/deceleration table increases, and the number of operational pulse decreases. In serial mode, this calculation is performed after replying the acknowledgment signal to the command, therefore, if the busy check was done without giving consideration to this calculation time, the internal over-run error could happen. Also, if the number of operational pulse is small, it may be the case that the constant speed operation starts up the system quicker, and increases the overall performance consequently.

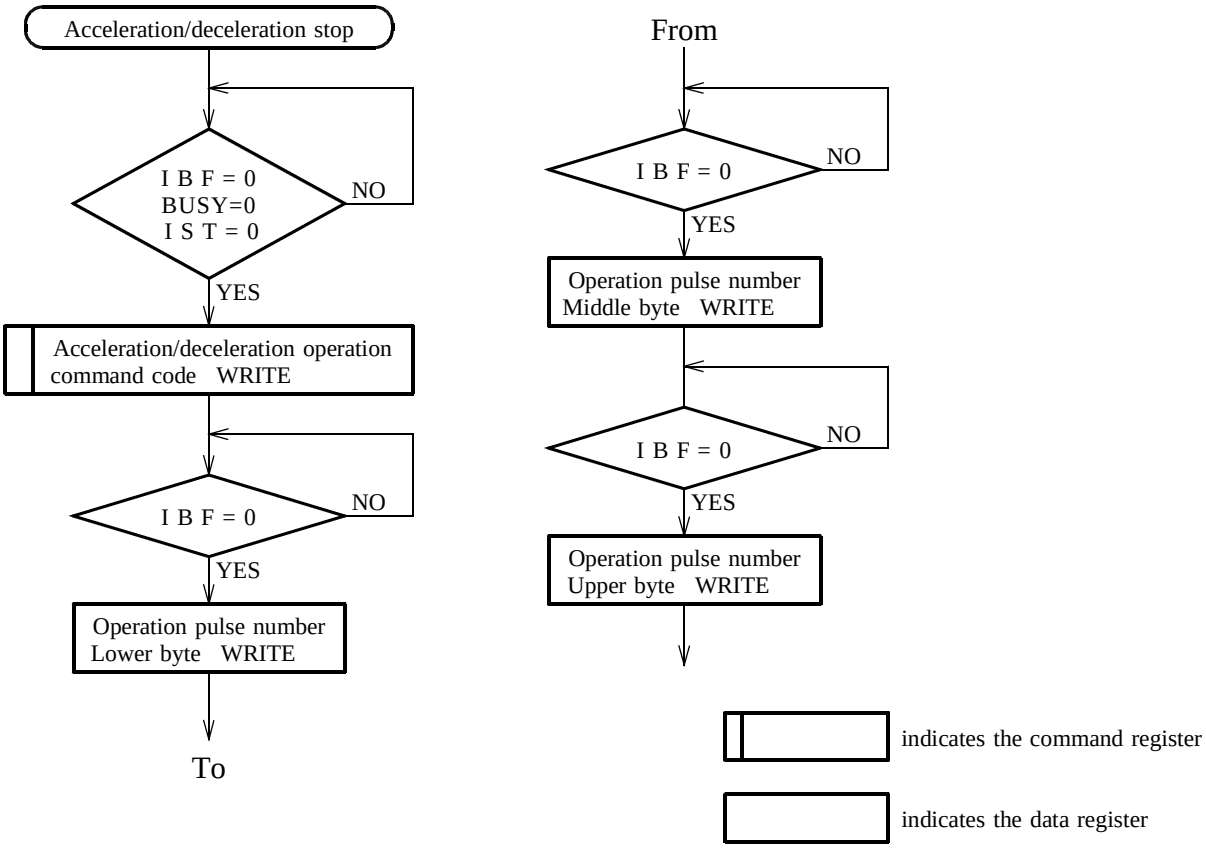


Fig.3-19. Flow chart of acceleration/deceleration operation

3-1-3-5. Constant speed operation

This command enables the output of a designated number of pulses at a designated speed. It is necessary to designate a constant speed pulse rate of two (2) bytes and an operation pulse number of three (3) bytes after the command code. The interrupt signal (INT*) will be available upon termination of pulse output if the INT bit is set at "0". This command code must be written only after the status register's IBF, BUSY and IST bits are checked. Data must be written in the correct order from the lower byte while confirming the IBF bit.

The value of constant speed pulse rate designated by this command must be within the range of the starting pulse rate at high speed, which is set at the time of initialization (RH or over), and kept 12 or over.

Designation of a constant speed pulse rate outside this range leads to a command error (command error code #16).

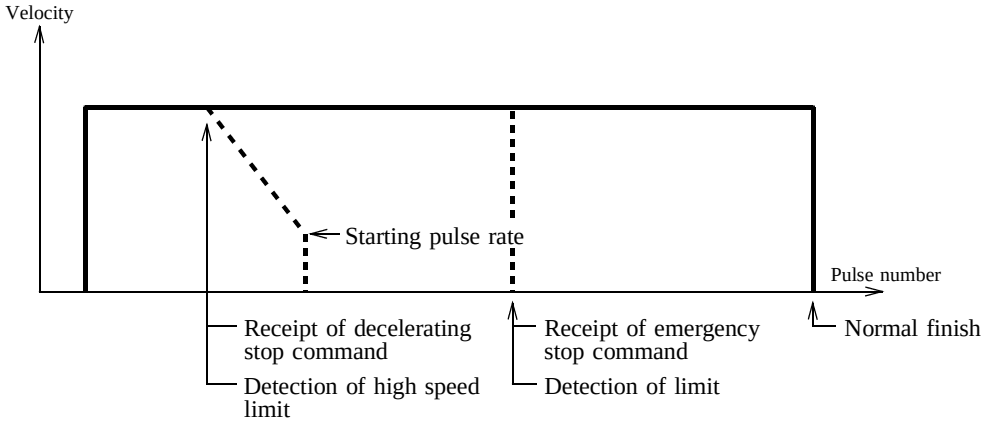


Fig.3-20. Sample constant speed operation

<Constant speed operation command/data>

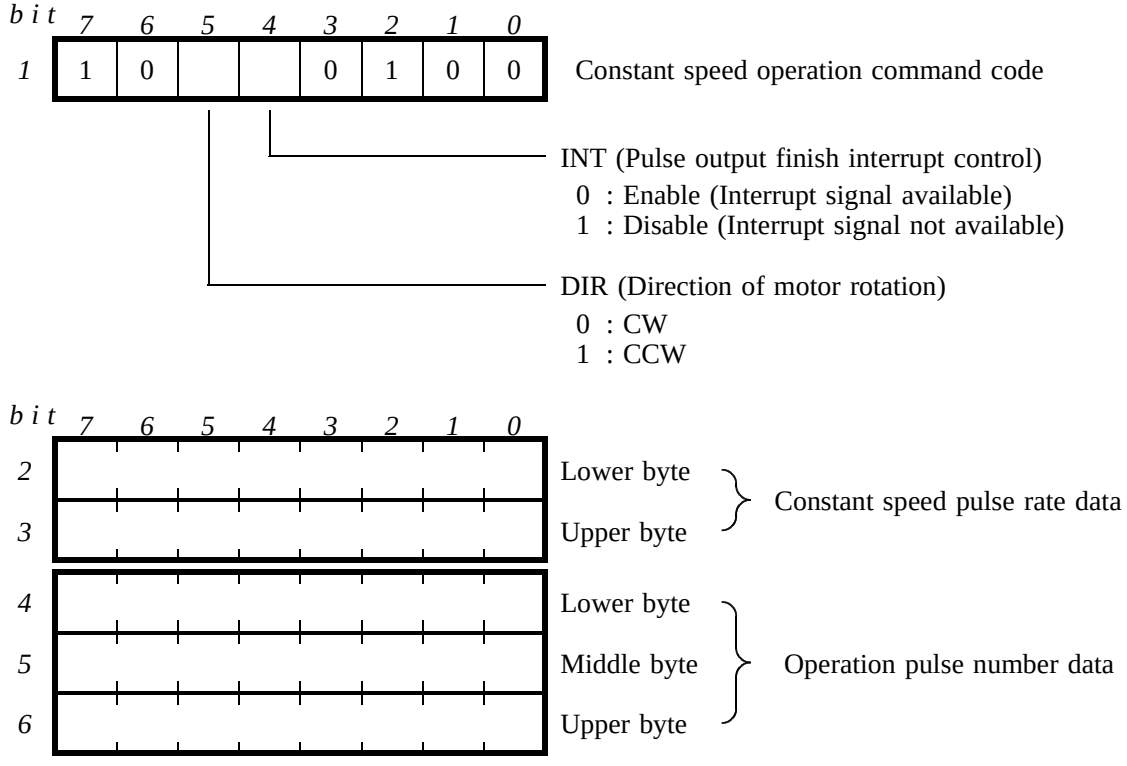


Fig.3-21

Fig. 3-22 is a flow chart indicating the flow of issue of constant speed operation command.

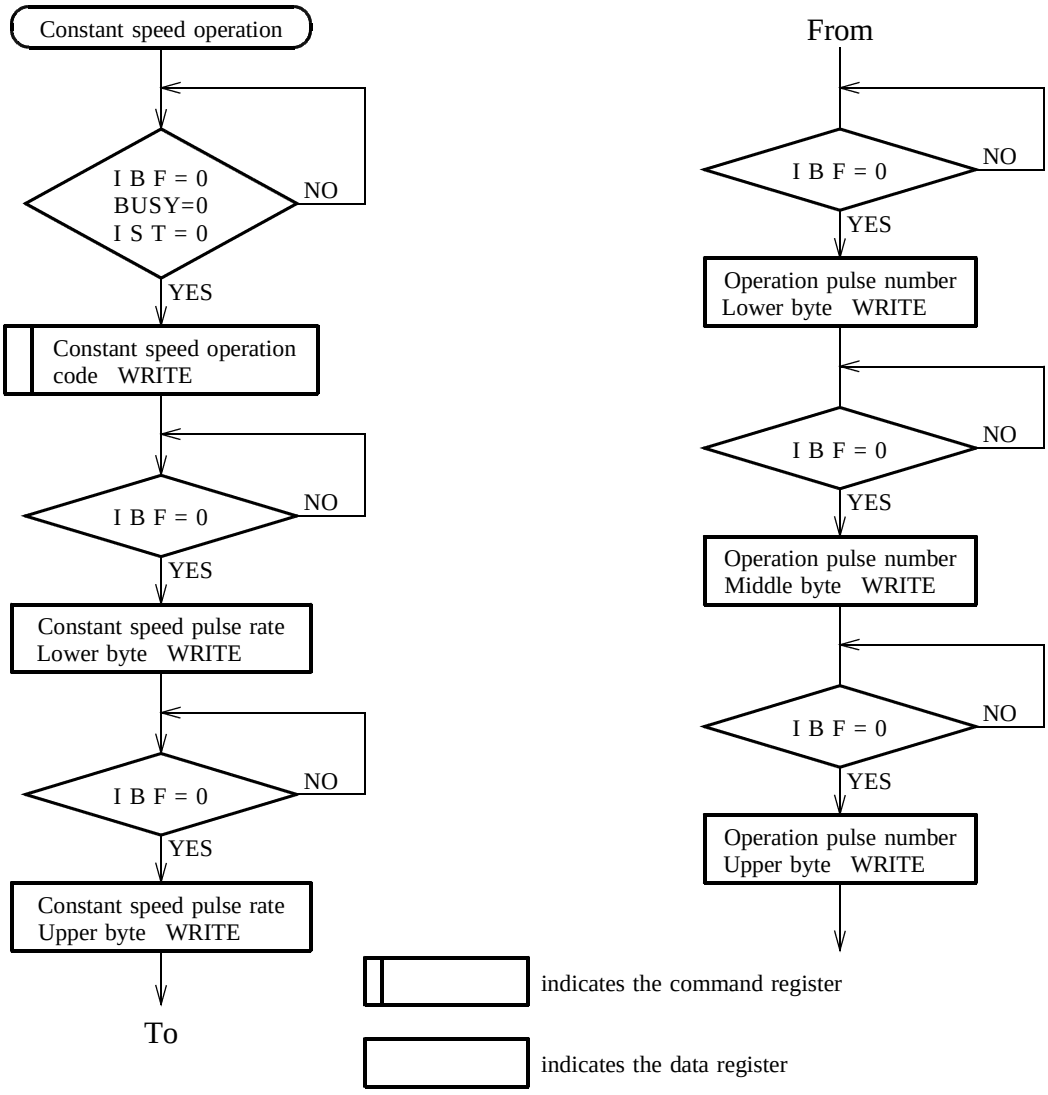


Fig. 3-22. Flow chart of constant speed operation

3-1-3-6 Continuous constant speed operation

This command enables the continuous output of pulses at a designated speed until the detection of the limit signal. It is necessary to designate a constant speed pulse rate of two (2) bytes after the command code. It makes an emergency stop once a limit signal (FL* or BL*) corresponding to the rotating direction has been detected. Output of pulses continues endlessly if there is no detection. A limit signal corresponding to the rotating direction refers to the FL* limit in the case of pulse output in the CW direction, or the BL* limit in the case of pulse output in the CCW direction. Limit signals in the direction opposite the direction of rotation shall be disregarded. The interrupt signal (INT*) will be available upon termination of pulse output if the INT bit is set at "0".

This command code must be written only after the status register's IBF, BUSY and IST bits are checked. Data must be written in the correct order from the lower byte while confirming the IBF bit.

The value of constant speed pulse rate designated by this command must be within the range of the starting pulse rate at high speed, which is set at the time of initialization (RH or over), and kept 12 or over.

Designation of a constant speed pulse rate outside this range leads to a command error (command error code #16).

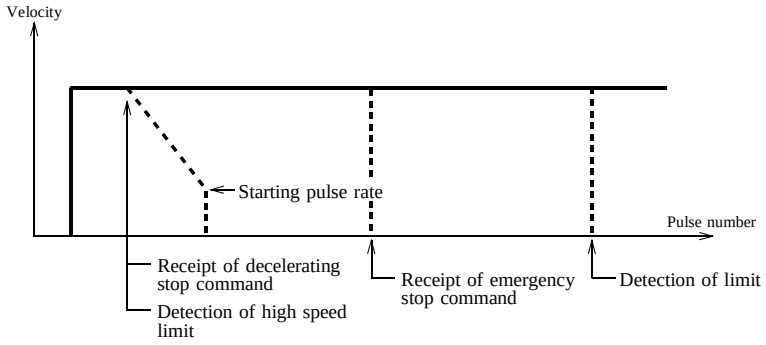


Fig.3-23. Sample continuous constant speed operation

<Continuous constant speed operation command/data>

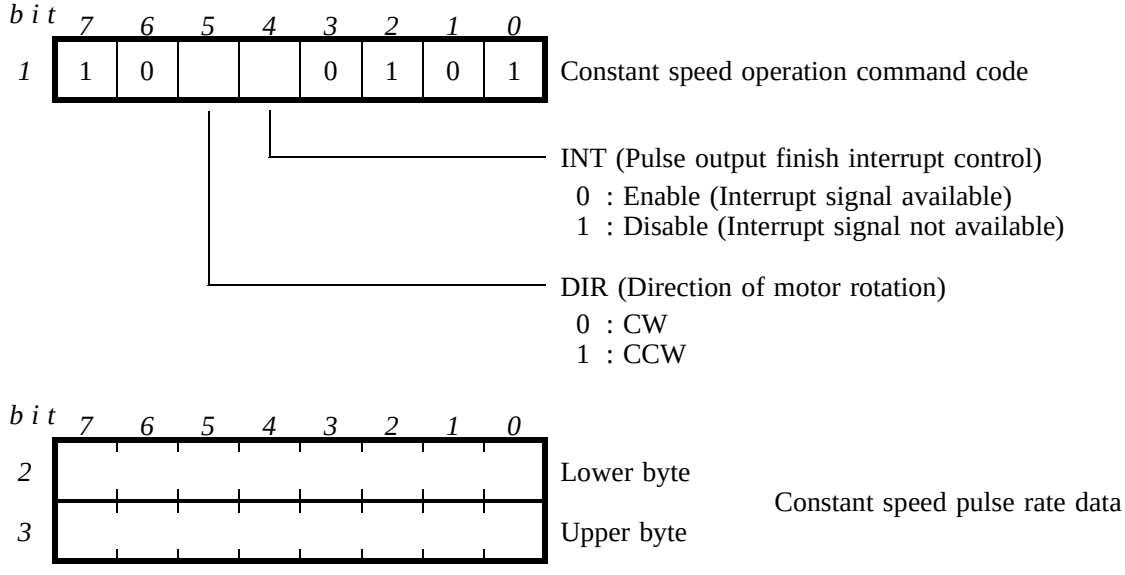


Fig.3-24

Fig. 3-25 is a flow chart indicating the flow of issue of continuous constant speed operation commands.

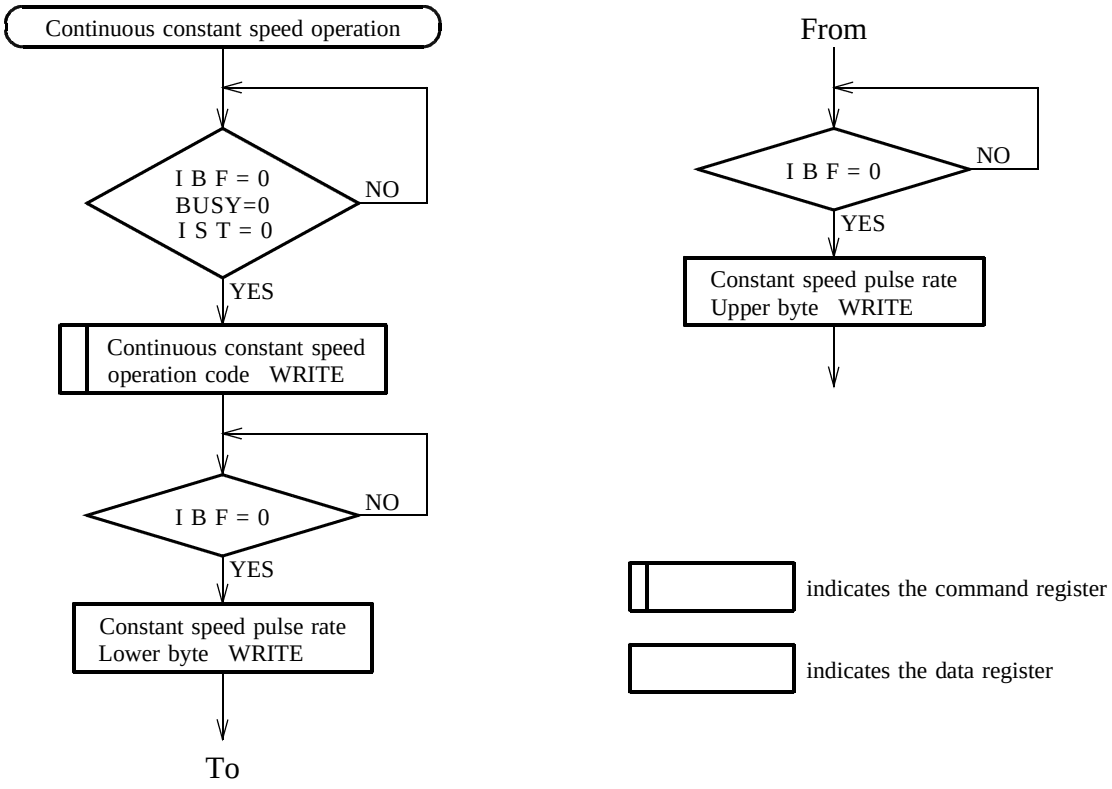


Fig.3-25. Flow chart of continuous constant speed operation

3-1-3-7. Continuous high speed operation

This command is for acceleration according to the initialization command and the continuous output of pulses at a high speed until the detection of the high speed limit signal. This command only carries a command code. Data designation is not necessary. It makes a decelerating stop once a high speed limit signal (FHL* or BHL*) corresponding to the rotating direction has been detected. Output of pulses at a high speed continues endlessly if there is no detection. A high speed limit signal corresponding to the rotating direction refers to the FHL* limit in the case of pulse output in the CW direction, or the BHL* limit in the case of pulse output in the CCW direction. High speed limit signals in the direction opposite the direction of rotation shall be disregarded. The interrupt signal (INT*) will be available upon termination of pulse output if the INT bit is set at "0".

This command code must be written only after the status register's IBF, BUSY and IST bits are checked.

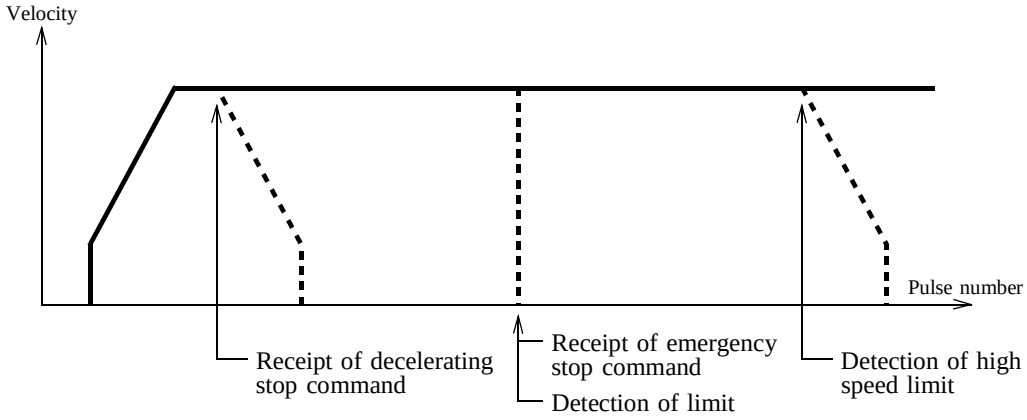


Fig.3-26. Sample continuous high speed operation

<Continuous constant speed operation command>

bit	7	6	5	4	3	2	1	0	
1	1	0			0	1	1	0	Continuous high speed operation command code

INT (Pulse output finish interrupt control)
0 : Enable (Interrupt signal available)
1 : Disable (Interrupt signal not available)

DIR (Direction of motor rotation)
0 : CW
1 : CCW

Fig.3-27

Fig. 3-28 is a flow chart indicating the flow of issue of continuous high speed operation command.

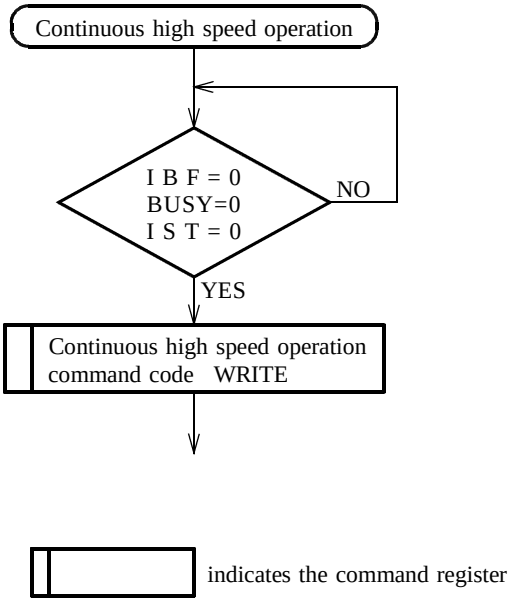


Fig.3-28. Flow chart of continuous high speed operation

3-1-3-8. Constant speed origin search operation

This command is for the continuous output of pulses at a designated speed until the detection of the origin signal. It is necessary to designate a constant speed pulse rate of two (2) bytes after the command code. Pulse output is terminated when the origin signal (ORG*) is detected, but will continue endlessly if there is no detection. The interrupt signal (INT*) will be available upon termination of pulse output if the INT bit is set at "0". However, the current position data will not be cleared following the detection of origin. This command code must be written only after the status register's IBF, BUSY and IST bits are checked. Data must be written in the correct order from the lower byte while confirming the IBF bit.

The value of constant speed pulse rate designated by this command must be within the range of pulse rate at thigh speed, which is set at the time of initialization (RH or over), and kept 12 or over. Designation of a constant speed pulse rate outside this range leads to a command error (command error code #16).

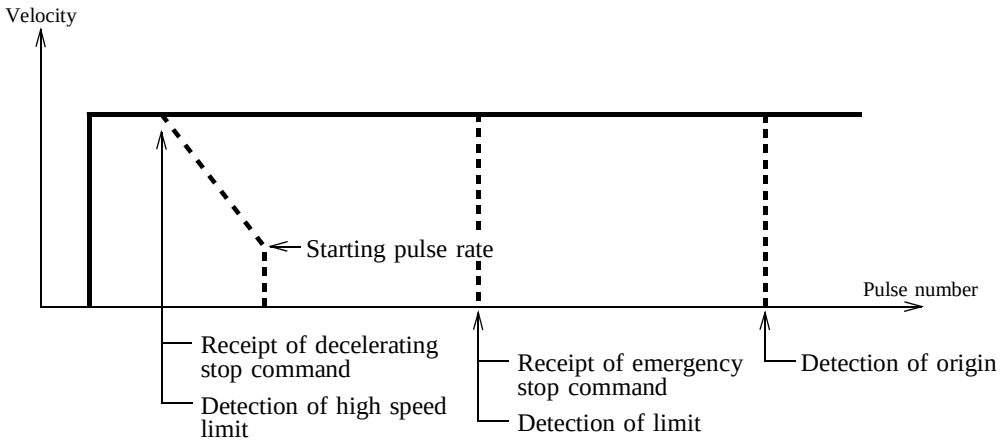


Fig.3-29. Sample constant speed origin search operation

<Constant speed origin search operation command/data>

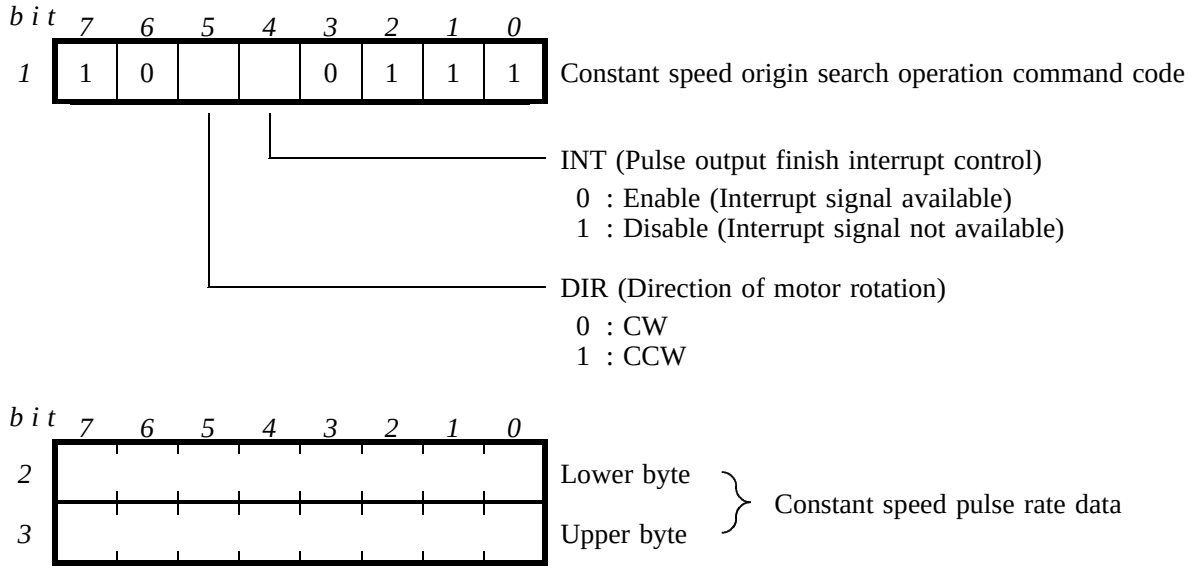


Fig.3-30

Fig. 3-31 is a flow chart indicating the flow of issue of constant speed origin search operation command.

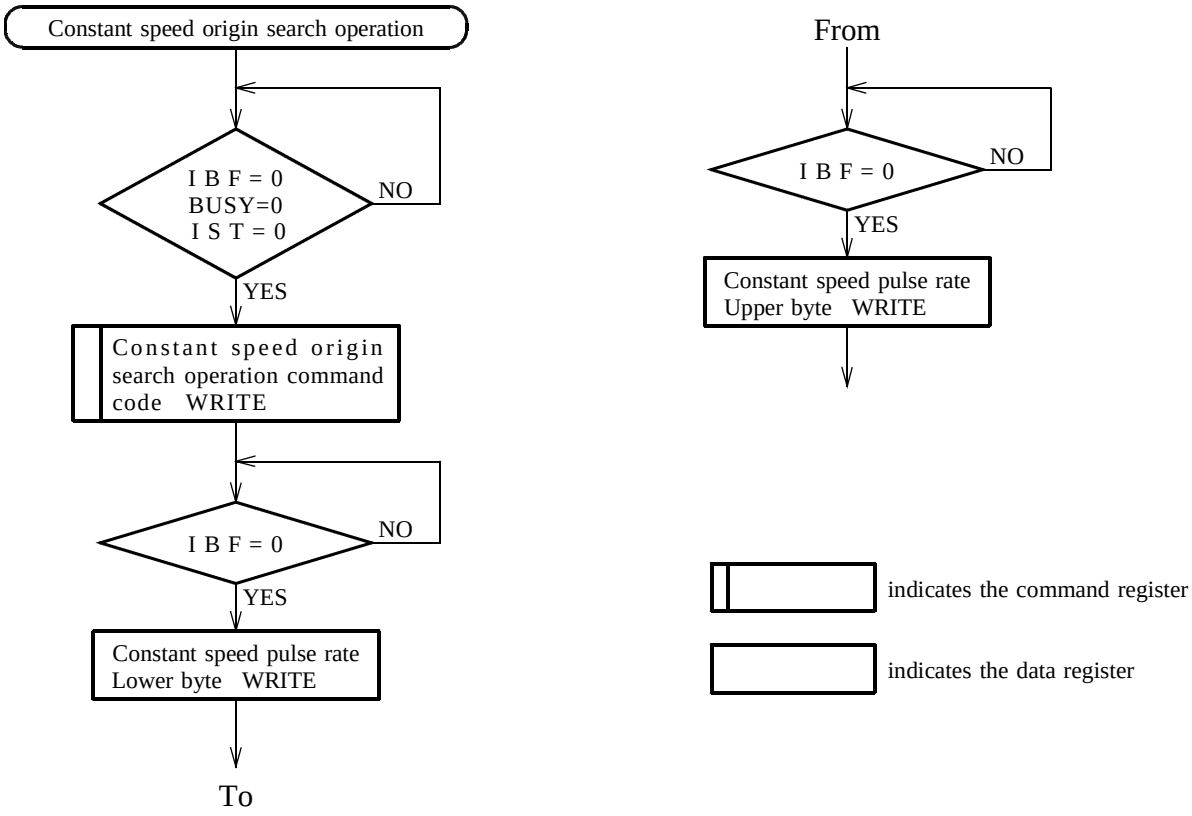


Fig.3-31. Flow chart of constant speed origin search operation

3-1-3-9. Instantaneous speed change

This command is used to instantaneously change the operation speed to any designated speed. The command does not affect the number of operation pulses.

This command code must be written only after the status register's IBF, BUSY and IST bits are checked. Data must be written in the correct order from the lower byte while confirming the IBF bit.

The value of constant speed pulse rate designated by this command must be within the range of the starting pulse rate set at the time of initialization and the pulse rate at high speed (RH or over). Designation of a constant speed pulse rate outside this range leads to a command error (command error code #16). In addition, in case that the base clock speed is 2MHz, the maximum speed must be set at 25 or over to safely execute this command.

If this command is received during pulse output by the acceleration/deceleration operation command, no further acceleration/deceleration operation will be executed unless the new speed change command comes in. Therefore, it will stop after sending out pulses at the speed set at the initialization period. Fig.3-32 shows how this command will be carried out.

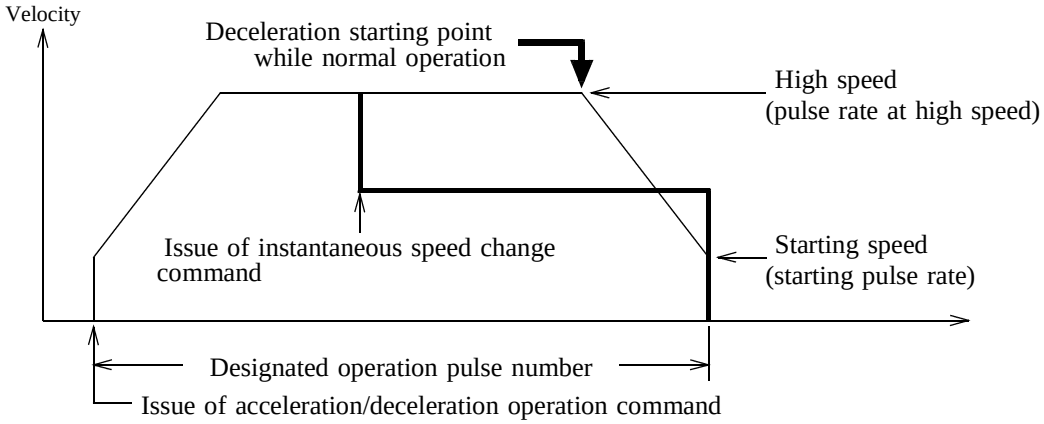


Fig.3-32.

<Instantaneous speed change command/data>

bit	7	6	5	4	3	2	1	0	
1	1	0	0	0	1	0	0	0	Instantaneous speed change command code
2									Lower byte
3									Upper byte

Change pulse rate data

Fig.3-33

This command must be used carefully because the PPMC-112 is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to the actual speed change (IST bit = "0").

Fig. 3-34 is a flow chart indicating the flow of issue of instantaneous speed change command.

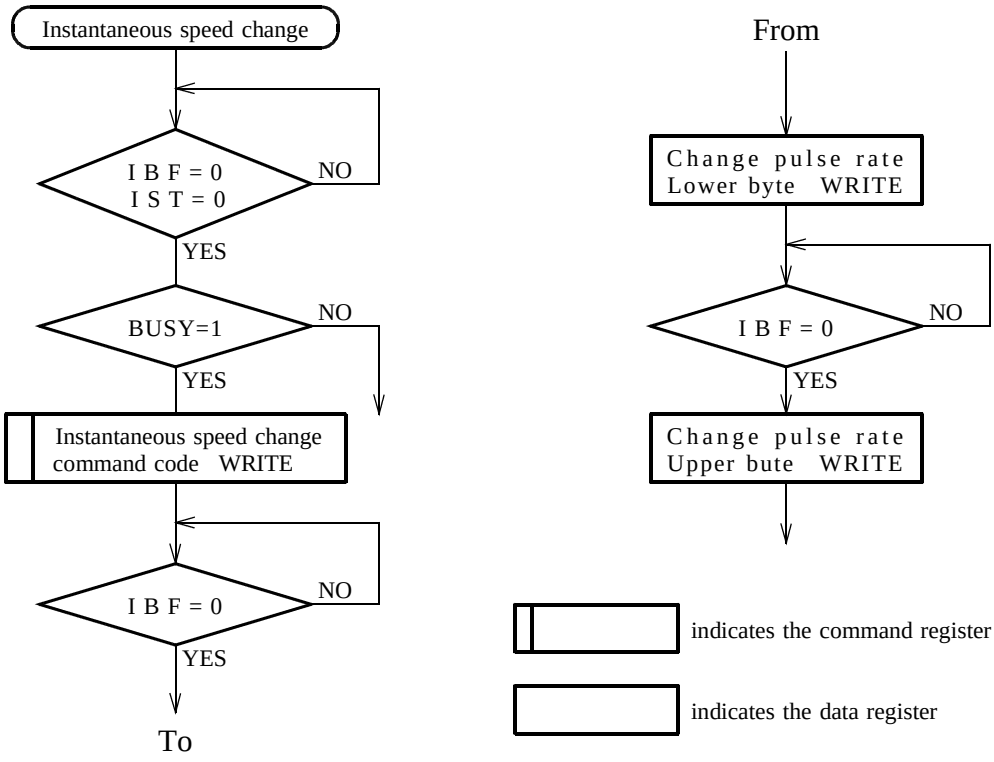


Fig.3-34. Flow chart of instantaneous speed change

3-1-3-10. Accelerating/decelerating speed change

This command changes a designated operation speed according to the acceleration/deceleration curve set at the time of initialization. The command does not affect the number of operation pulses.

This command code must be written only after the status register's IBF, BUSY and IST bits are checked. Data must be written in the correct order from the lower byte while confirming the IBF bit.

The value of the constant speed pulse rate designated by this command must be within the range of the starting pulse rate set at the time of initialization and the pulse rate at high speed (RH to RL). Designation of a constant speed pulse rate outside this range leads to a command error (command error code #16).

Furthermore, if it operates at the slower than the start up speed following the constant speed operation command, the command causes error (command error code 16). On top of that, if the base clock is 2MHz, the maximum speed rate for this command to be executed safely must be 25 or over.

If this command is received during pulse output by the acceleration/deceleration operation command, no further acceleration/deceleration operation will be executed after acceleration/deceleration speed change unless new speed change command comes in. Fig.3-35 shows how the command will be carried out.

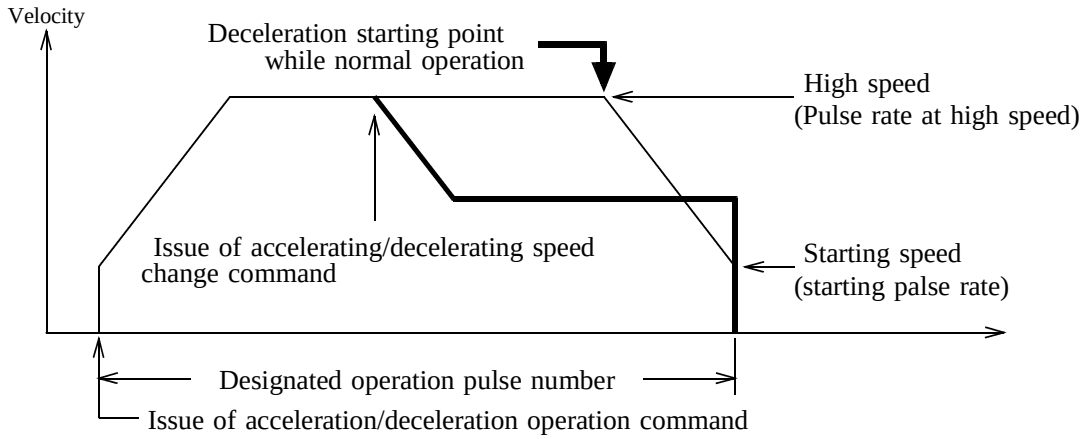


Fig.3-35.

<Accelerating/decelerating speed change command/data>

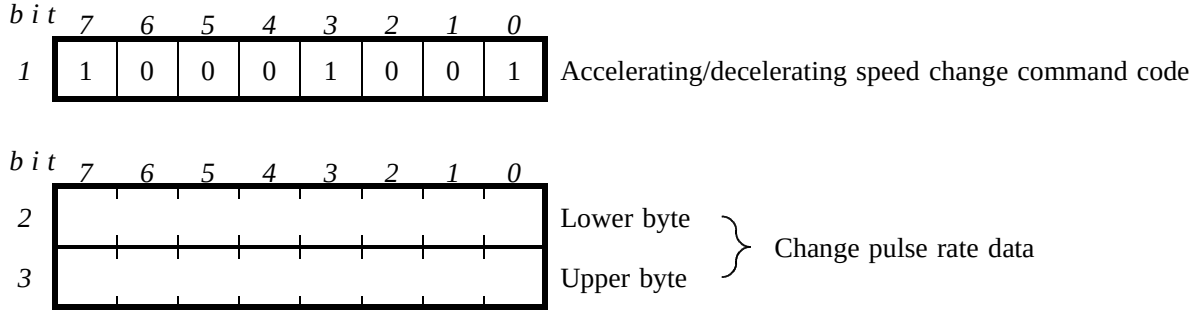


Fig. 3-36

This command must be used carefully because the PPMC-112 is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to the actual speed change (IST bit = "0").

Fig. 3-37 is a flow chart indicating the flow of issue of accelerating/decelerating speed change command (i.e., command to change speed through acceleration/deceleration).

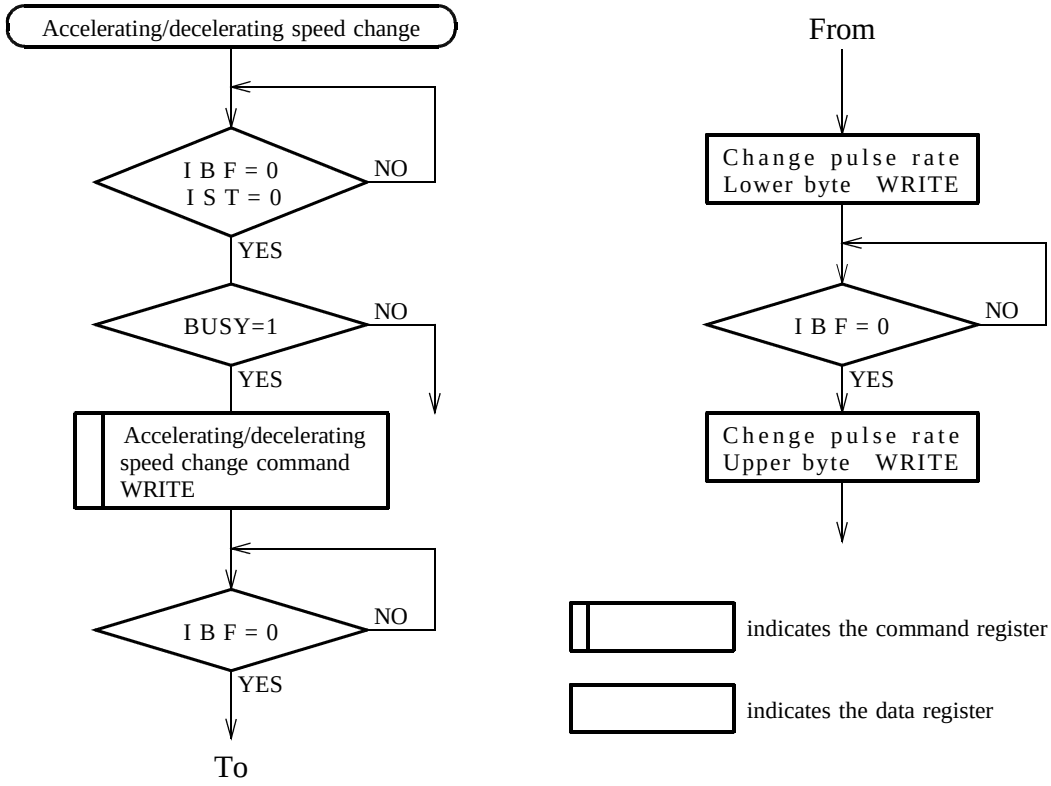


Fig.3-37. Flow chart of accelerating/decelerating speed change

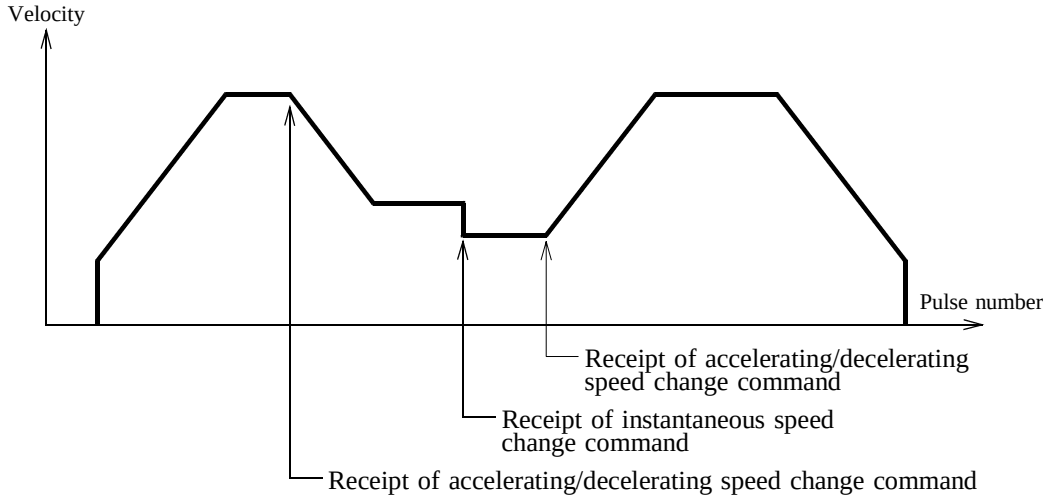


Fig.3-38. Sample speed change in accelerating/ decelerating speed change operation

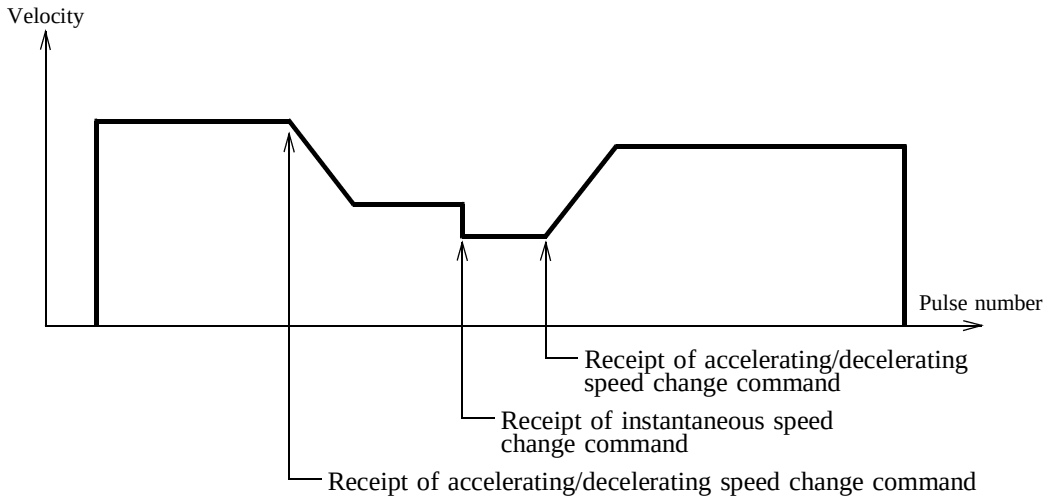


Fig. 3-39 (Sample speed change in constant speed operation)

3-1-4. Auxiliary command (Internal register read command)

This command enables examining of the internal conditions of the PPMC-112 and the conditions of external input signals. As shown in Fig. 3-40, there are seven (7) internal register read commands. Reading data, except for current position and acceleration/deceleration table, is possible during pulse output.

<Internal register read command>

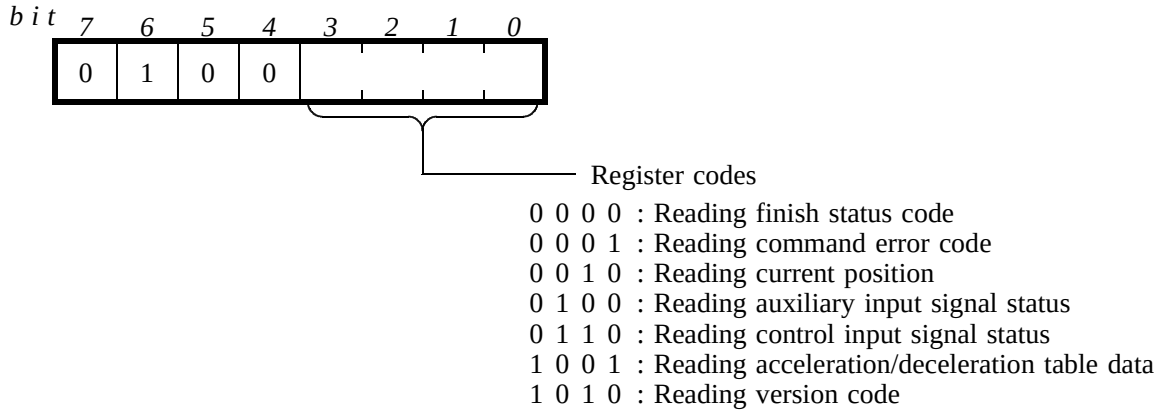


Fig.3-40. Internal register read command bit configuration

3-1-4-1. Finish status code read command

This command enables reading of the cause of pulse output. This command, which carries a command code alone, reads out a 1-byte finish status code after the command code is written.

When this command is issued for interlock release interrupt, "00h" will be read instead of finish status code.

<Finish status code read command/code>

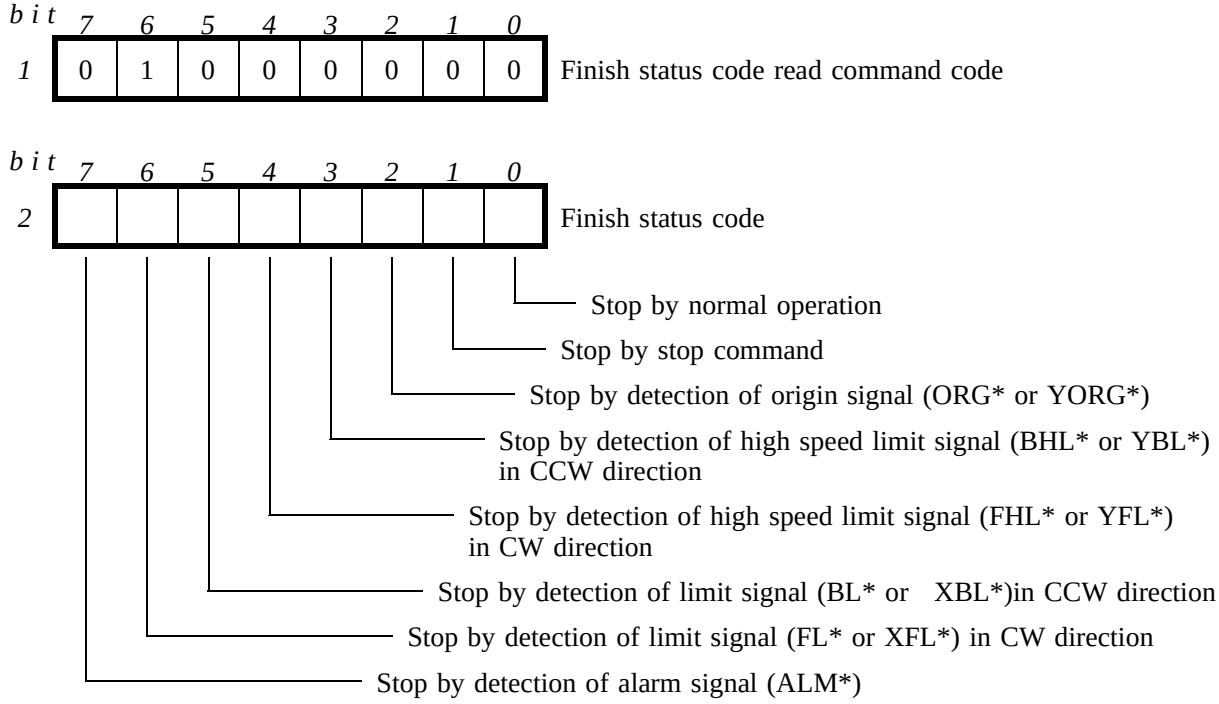


Fig.3-41

Each finish status code is registered with the internal register of the PPMC-112 upon termination of pulse output and is maintained during the next pulse output operation. The immediately preceding finish status code can be read for reference during pulse output; however, the preceding finish status code shall be replaced with the most recent finish status code upon termination of the pulse output.
This command must be used carefully during pulse output because the PPMC-112 is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to when the finish status code is registered with the output buffer inside the PPMC-112 (OBF bit = "1").
The details of each bit of finish status code are as follows:

(1) Bit 0 [Stop by normal operation]
Bit 0 indicates "1" upon termination of pulse output when the output of operation pulse number, which was designated at the issue of acceleration/deceleration operation command or constant speed operation command, has been fully completed.

(2) Bit 1 [Stop by stop command]
Bit 1 indicates "1" upon termination of pulse output with the receipt of instantaneous stop command or decelerating stop command during pulse output.

(3) Bit 2 [Stop by detection of origin signal (ORG* or YORG*)]
Bit 2 indicates "1" upon termination of pulse output with the detection of the origin limit signal (ORG* or YORG*) during origin search.

(4) Bit 3 [Stop by detection of high speed limit signal (BHL* or YBL*) in CCW direction]
Bit 3 indicates "1" upon termination of pulse output with the detection of the high speed limit signal (BHL*) or the limit signal (with SYNC-101) in the CCW direction during pulse output for the CCW direction.

(5) Bit 4 [Stop by detection of high speed limit signal (FHL* or YFL*) in CW direction]
Bit 4 indicates "1" upon termination of pulse output with the detection of the high speed limit signal (FHL*) or the limit signal (with SYNC-101) in the CW direction during pulse output for the CW direction.

(6) Bit 5 [Stop by detection of limit signal (BL* or XBL*) in CCW direction]
Bit 5 indicates "1" upon termination of pulse output with the detection of the limit signal (BL* or XBL*) in the CCW direction during pulse output for the CCW direction.

(7) Bit 6 [Stop by detection of limit signal (FL* or XFL*) in CW direction]
Bit 6 indicates "1" upon termination of pulse output with the detection of the limit signal (FL* or XFL*) in the CW direction during pulse output for the CW direction.

(8) Bit 7 [Stop by detection of alarm signal (ALM*)]
Bit 7 indicates "1" upon termination of pulse output with the detection of the alarm signal (ALM*) during pulse output.

The issue of finish status read command clears interrupt signal (INT*) resulting from the alarm input signal, the interlock release interruption or the pulse output termination. In case of the interlock release interruption, issuing the finish status read command changes status register bit5 (INTI bit) to "0".
This command code must be written only after the status register's IBF and IST bits are checked. A finish status code must be read after the OBF bit is checked.

Fig. 3-42 is a flow chart indicating the flow of issue of finish status read command.

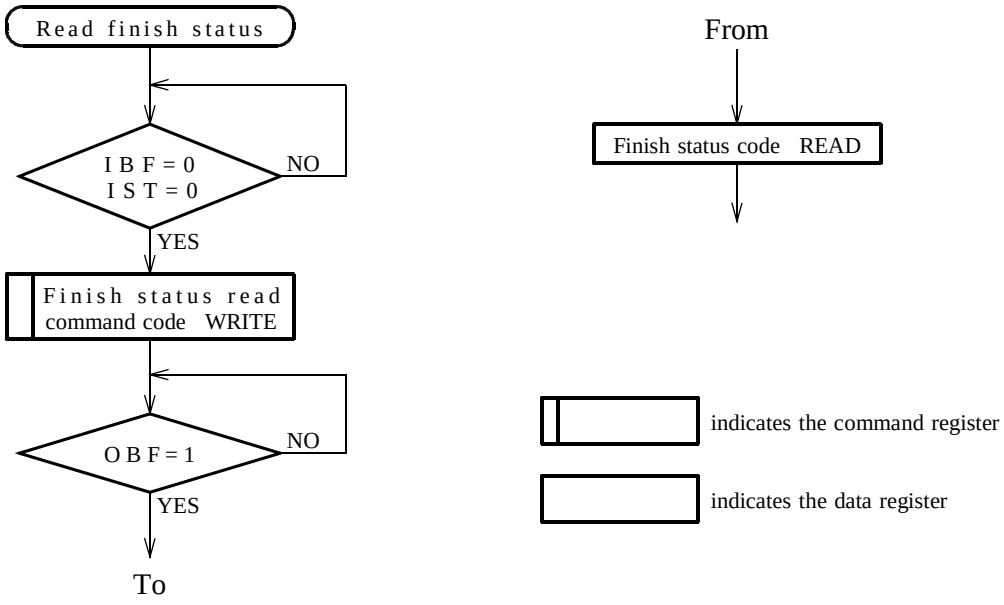


Fig.3-42. Flow chart of finish status read

3-1-4-2. Error code read command

This command enables reading of the cause of command error. This command can be used before, during or after pulse output.

This command, which carries a command code alone, reads out a 1-byte command error code upon writing of the command code. This command code must be written only after the status register's IBF and IST bits are checked. An error code must be read after the OBF bit is checked.

If a wrong command code or data is provided from the host processor to the PPMC-112, while bit 5 (INTE bit) and bit 7 (ERR bit) of the status register indicates "1".

Each error code is overwritten (replaced) every time a command is received from the host processor. The error code, therefore, reads "00h" once a correct command is provided after the occurrence of an error. Likewise, bit 7 (ERR bit) of the status register is revised every time a correct command is received from the host processor.

This command must be used carefully during pulse output because the PPMC-112 is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to when the finish status code is registered with the output buffer inside the PPMC-112 (OBF bit = "1").

Please refer to Table 3-3 Error codes.

<Error code read command/code>

bit	7	6	5	4	3	2	1	0	
1	0	1	0	0	0	0	0	1	Command error code read command code

<Data to be read>

bit	7	6	5	4	3	2	1	0	
2									Error code

Fig. 3-43

Fig. 3-44 is a flow chart indicating the flow of issue of error code read command, and Table 3-3 is a list of error codes.

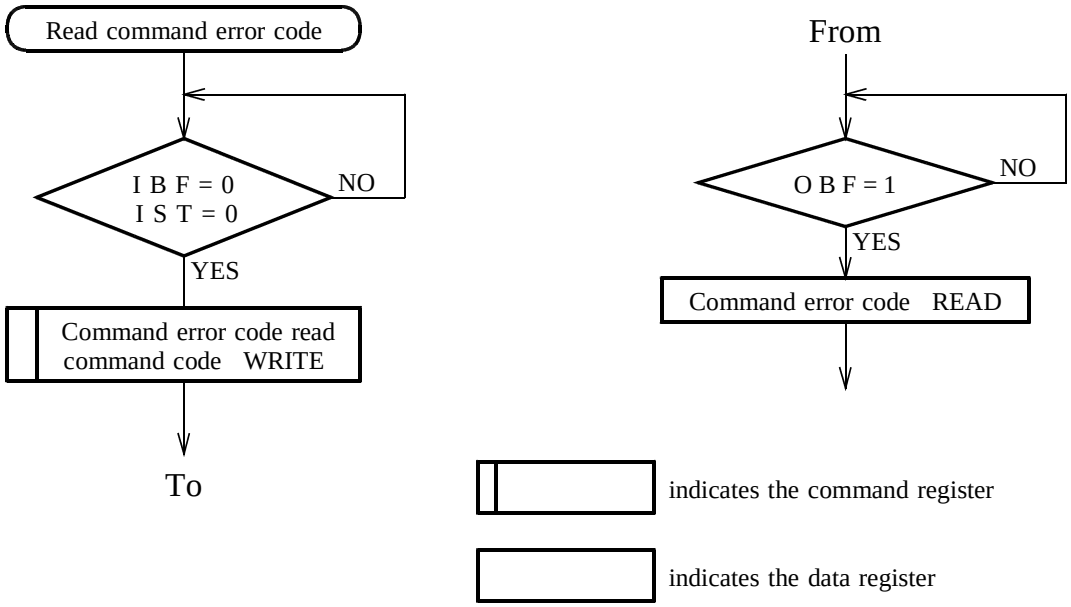


Fig. 3-44. Flow chart of error code read

3-1-4-3. Current position read command

This command is used to obtain the reading (value) of the current position counter inside the PPMC-112. This command can be used only when there is no pulse output. This command, which carries a command code alone, reads out a 24-bit datum on the current position upon writing of the command code.

This command code must be written only after the status register's IBF, BUSY and IST bits are checked. The 24-bit current position data must be read, one byte at a time, in the correct order starting with the lower byte, then the middle byte and finally the upper byte, while checking the OBF bit.

<Current position read command code/data>

bit	7	6	5	4	3	2	1	0	
1	0	1	0	0	0	0	1	0	Current position read command code

<Data to be read>

bit	7	6	5	4	3	2	1	0		
1									Lower byte	Current position data
2									Middle byte	
3									Upper byte	

Fig. 3-45

The current position counter of the PPMC-112 is a 24-bit UP/DOWN counter with binary complement indication and the starting value of "000000h." The value of this counter increments when there is an output of pulse in the CW direction, and when the value overflow "7FFFFFh". In reverse, if it is in the CCW direction, it starts at "800000h" and overflows to "7FFFFFh". The data on this current position counter, which is cleared every time when the operation command comes in, enables current position control by means of absolute position. Table3-5 shows the correlation between the direction of pulse output and increment/decrement in counter reading.

Table 3-5. Correlation between the direction of pulse output and increment/decrement in counter reading

Reading of current position counter	Correlation between the direction of pulse output and increment/decrement in counter reading
7 F F F F F h	In case of output of pulse in CCW direction
7 F F F F E h	
7 F F F F D h	↓
:	
0 0 0 0 0 2 h	
0 0 0 0 0 1 h	
0 0 0 0 0 0 h	Counter reads "000000h" after resetting
F F F F F F h	
F F F F F E h	↑
:	
8 0 0 0 0 2 h	
8 0 0 0 0 1 h	
8 0 0 0 0 0 h	In case of output of pulse in CW direction

In general, the constant speed origin search command seeks the point where origin signal (ORG*) is established, at that point, using the current position setting command, the position is given the starting value of "000000h" on the current position data. Position setting control shall be carried out using this position as the base point.

Fig. 3-46 is a flow chart indicating the flow of issue of the position read command.

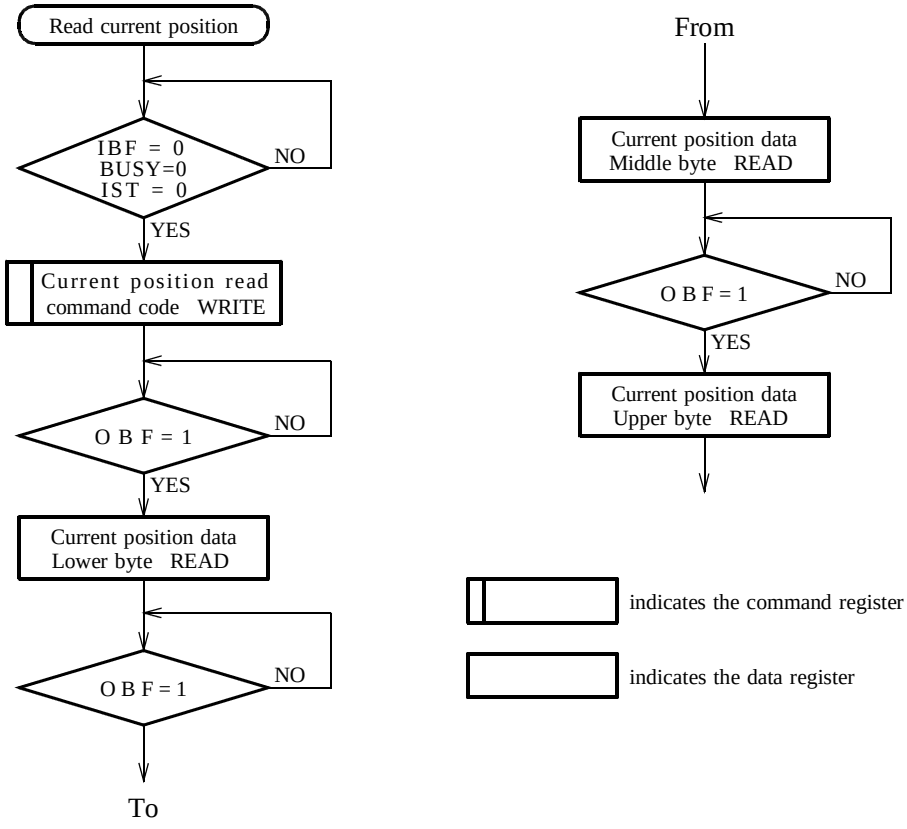


Fig.3-46. Flow chart of current position read command

3-1-4-4. Auxiliary input signal status code read command

This command is used to read the conditions of auxiliary input signals AUXI0 through AUXI3. There is a delay of approximately 20 microsecond in reading an auxiliary input signal status code. This command, which carries a command code alone, reads out a 1-byte auxiliary input signal status code upon writing of the command code. Bits 4 to 7 are "0". (In serial mode, AUXI0 to AUXI5 are valid, bits 6 and 7 are "0".)

This command code must be written only after the status register's IBF and IST bits are checked. The auxiliary input signal status code data must be read while checking the OBF bit.

This command can be used before, during or after pulse output

<Auxiliary input signal status code read command/code>

<Data to be read >

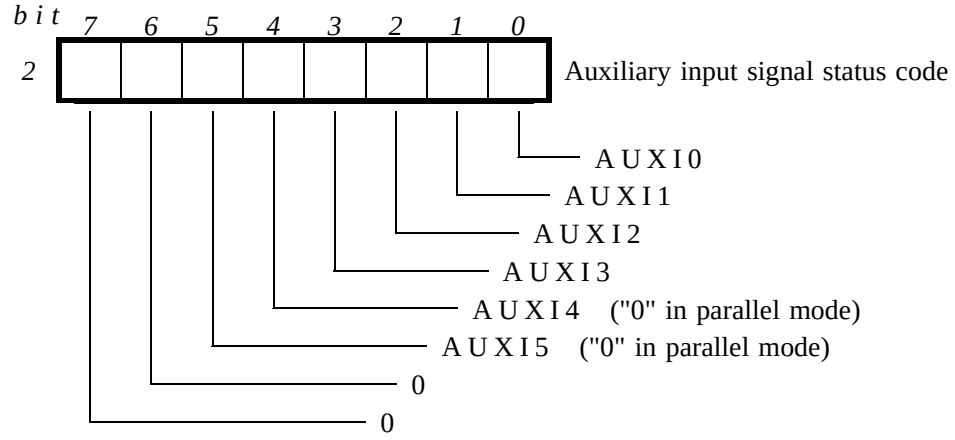


Fig.3-47

This command must be used carefully during pulse output because the PPMC-112 is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to when the auxiliary input signal status data is registered with the output buffer inside the PPMC-112 (OBF bit = "1").

Fig. 3-48 is a flow chart indicating the flow of issue of the auxiliary input signal status read command.

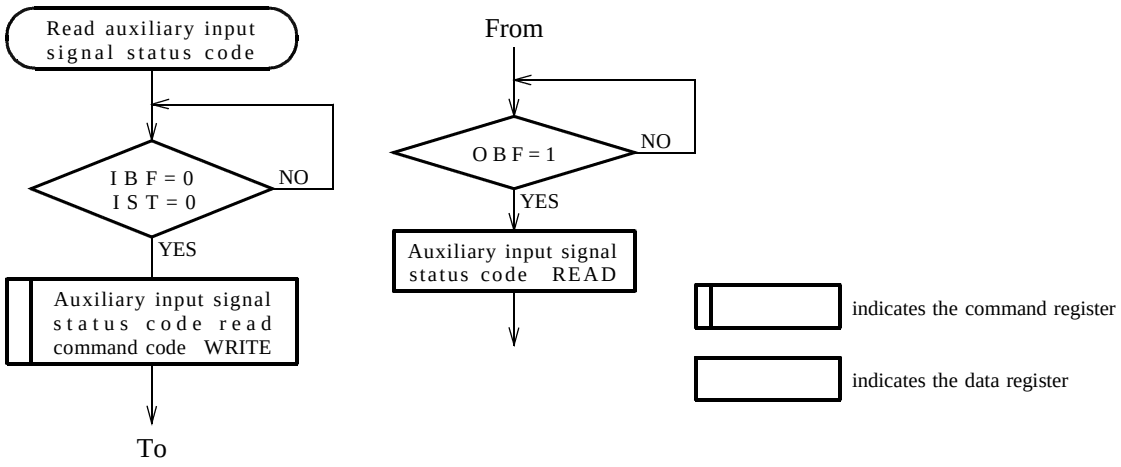


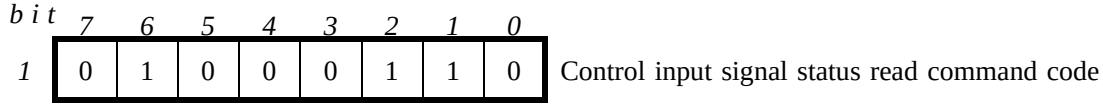
Fig. 3-48. Flow chart of auxiliary input signal status read

3-1-4-5. Control input signal status read command

This command is used to read the conditions of various input signals of the PPMC-112, including limit input signals, origin signals, alarm signals and RUN signals. This command reads the condition of each input terminal at the time of this command. Therefore, bits 3 and 4 do not indicate "0" in the case of a decelerating stop at the high speed limit since it has passed the point of detection of high speed limit. Except in case of RUN signal, in terms of reading each bit, "0" indicates that there is an input signal, while "1" indicates absence of input signals. This command, which carries a command code alone, reads out a 1-byte control input signal status code upon writing the command code.

This command code must be written only after the status register's IBF and IST bits are checked. The control input signal status must be read while checking and confirming the OBF bit.

<Control input signal status read command/code>



<Data to be read>

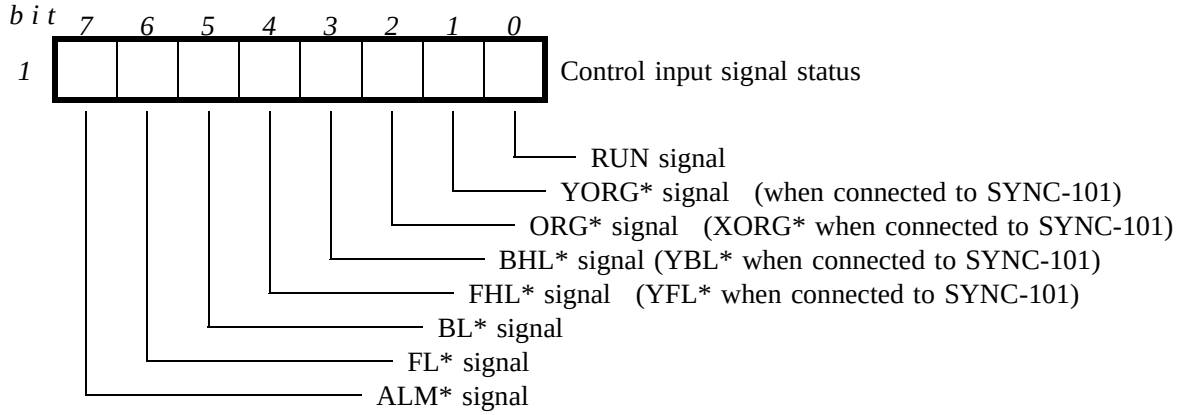


Fig.3-49

This command must be used carefully during pulse output because the PPMC-112 is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to when the control input signal status data is registered with the output buffer inside the PPMC-112 (OBF bit = "1").

Fig. 3-50 is a flow chart indicating the flow of issue of the control input signal status code read command.

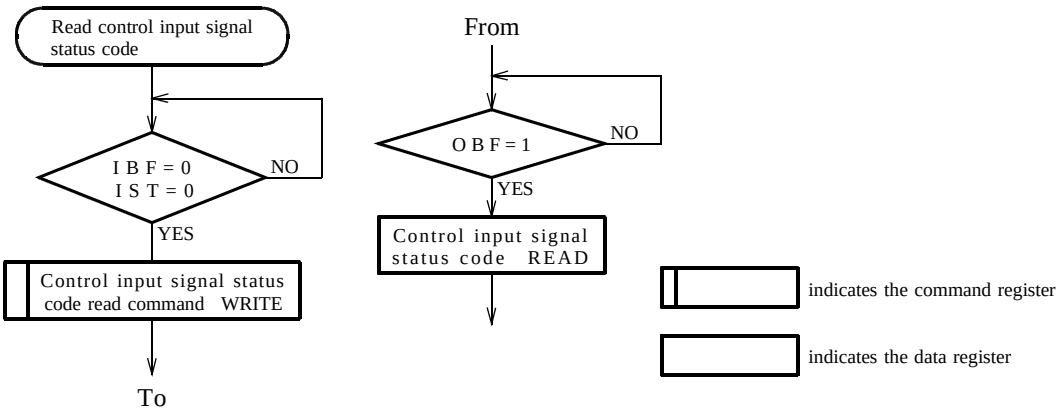


Fig.3-50. Flow chart of control input signal status code read

3-1-4-6. Acceleration/deceleration table read command

This command reads out the PPMC-112 internal acceleration/deceleration table generated at the initialization setting. It is also possible to partly modify the read out data, and then upload it again using the free curve acceleration/deceleration initial setting command. Before this command to be written, the status register BUSY, IBF and IST bits must be verified. And before this command to be read, OBF bits must be verified.

<Acceleration/deceleration table read command/code>

bit	7	6	5	4	3	2	1	0	
	0	0	0	0	x	x	1	x	acceration/deceleration table data read command code

<Data to be read>

bit	7	6	5	4	3	2	1	0	
1									Number (N) of acceleration/deceleration steps
2									Lower byte } Pulse rate at high speed
3									Upper byte
4									Lower byte } Pulse rate for Step 1 (R1)
5									Upper byte
6									Lower byte } Pulse rate for Step 2 (R2)
7									Upper byte
:	:			:					
									Lower byte } Pulse rate for Step N (Rn)
									Upper byte
									Lower byte } Pulse number for Step 1 (S1)
									Upper byte
									Lower byte } Pulse number for Step 2 (S2)
									Upper byte
	:			:					
									Lower byte } Pulse number for Step N (Sn)
									Upper byte

Fig. 3-51

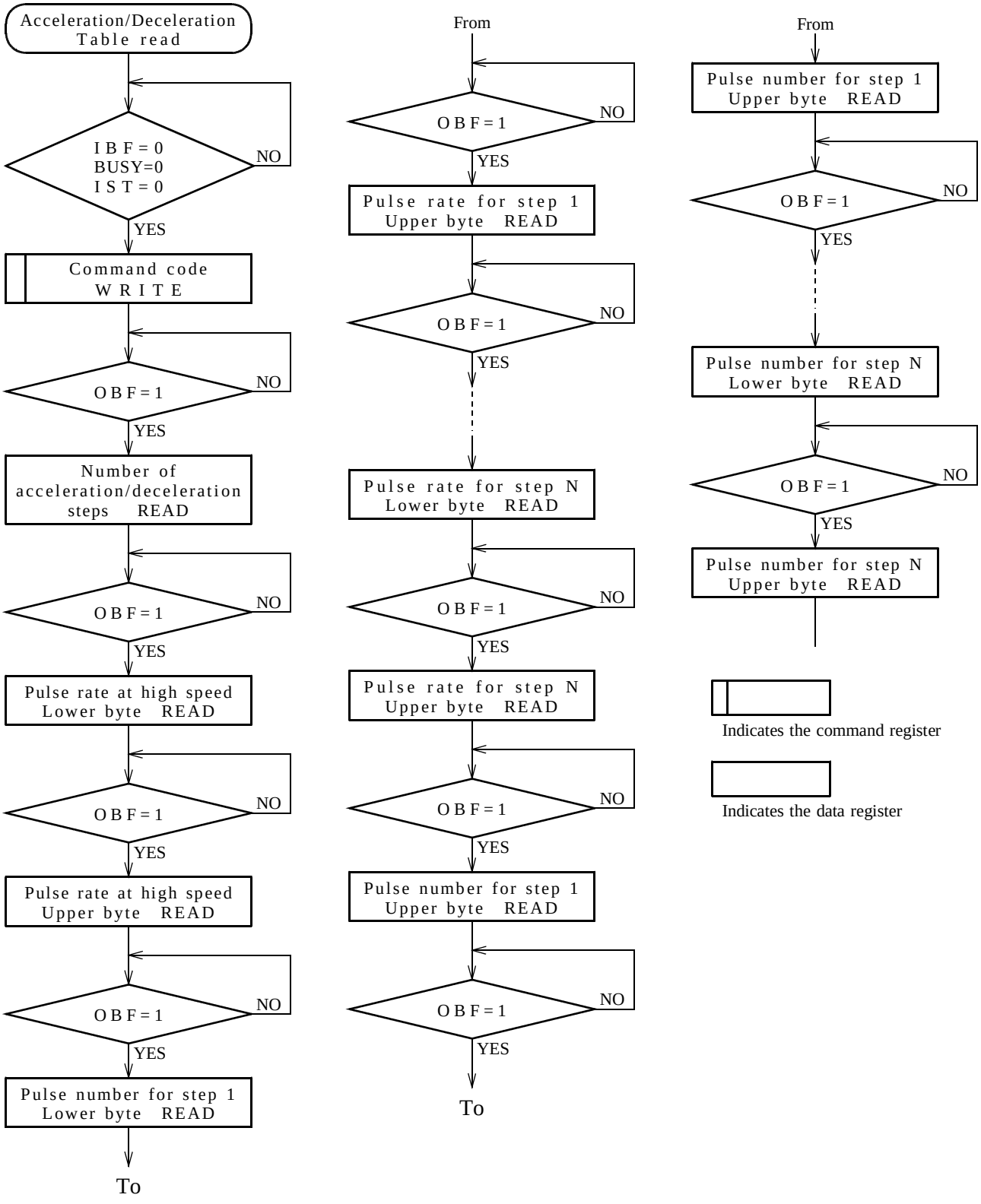


Fig.3-52. Flow chart of Acceleration deceleration table data read command

3-1-4-7. Version code read command

This command reads PPMC-112 version Information. This information is expressed in ASCII 1 byte code. This current version code is "02h" ("42h" in serial mode), and when SYNC-101 is connected, the version code is "12" ("62h" in serial mode). This command consists of only command codes, and after the issuance, 1 byte data is to be read. Before this command is to be written, the status code register's IBF and IST bits must be verified. Before this command is to be read, the OBF bit must be verified.

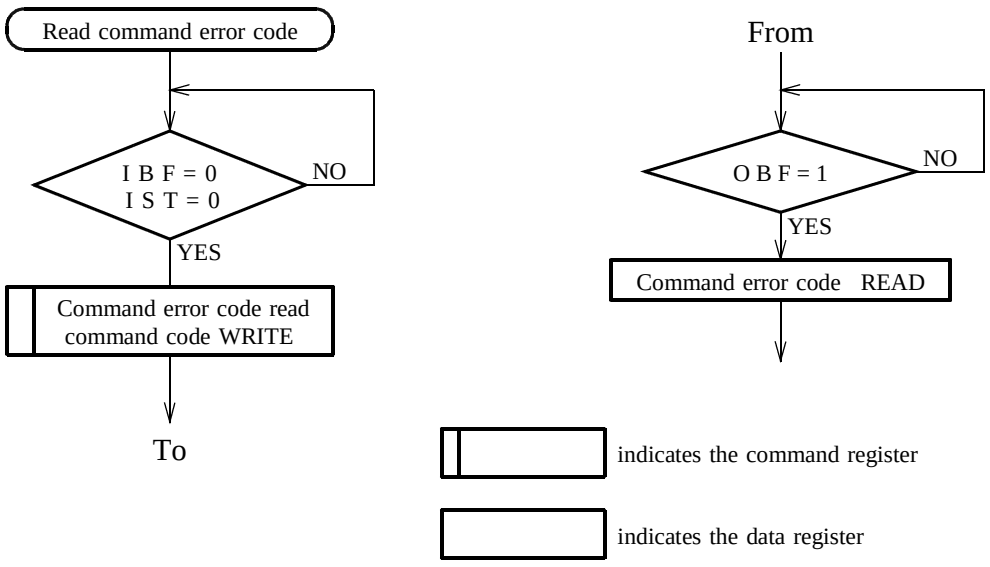
<Version code read command/code>

bit	7	6	5	4	3	2	1	0	
1	0	1	0	0	0	0	0	1	Version code read command code

<Data to be read>

bit	7	6	5	4	3	2	1	0	
1	0	0	0	0	0	0	0	1	Version code (SYNC-101 not conneced)

Fig.3-53



F i g . 3 - 5 4 . Flow chart of Version code read

3-1-5 Auxiliary commands

These commands are used for current position setting, auxiliary output port output, high speed limit effective speed setting, and interlock release position setting.. There are four (4) commands as shown in Fig. 3-55. The auxiliary output command can be used before, during or after pulse output, while the current position setting command, high speed limit effective speed setting command and interlock release position setting command can be used only when there is no pulse output.

<Auxiliary command>

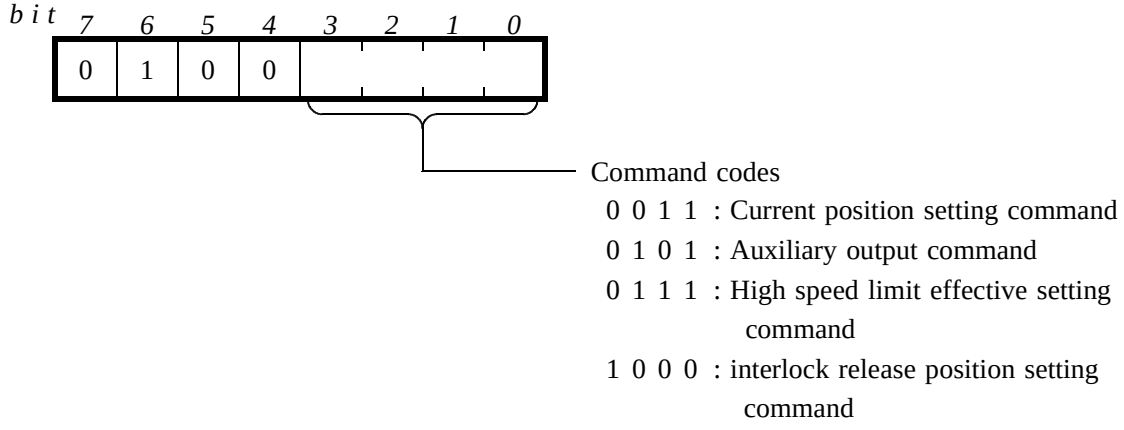


Fig. 3-55. Auxiliary command bit configuration

3-1-5-1. Current position setting command

This command is used to set the current position of the motor. This command can be used only when there is no pulse output. The reading shows "0" after resetting.

This command code must be written only after the status register's IBF, IST and BUSY bits are checked. 3-byte data on the current position setting must be written in the correct order starting with the lower byte, while checking the IBF bit.

<Current position setting command/data>

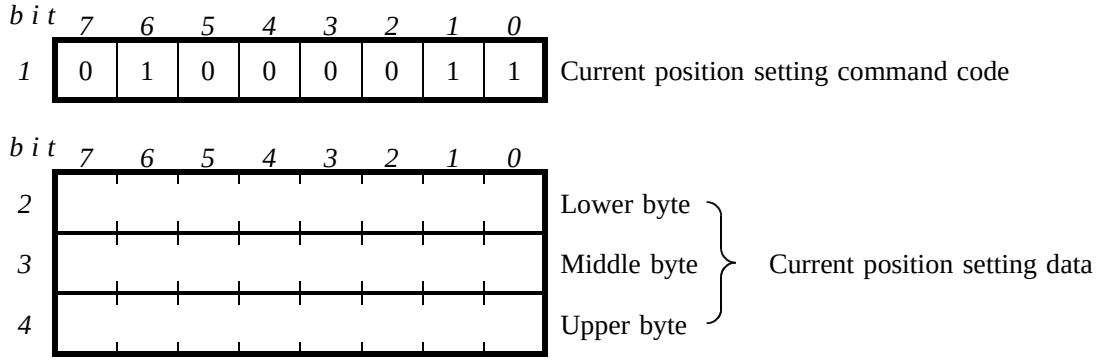


Fig. 3-57

Fig. 3-58 is a flow chart indicating the flow of issue of the current position setting command.

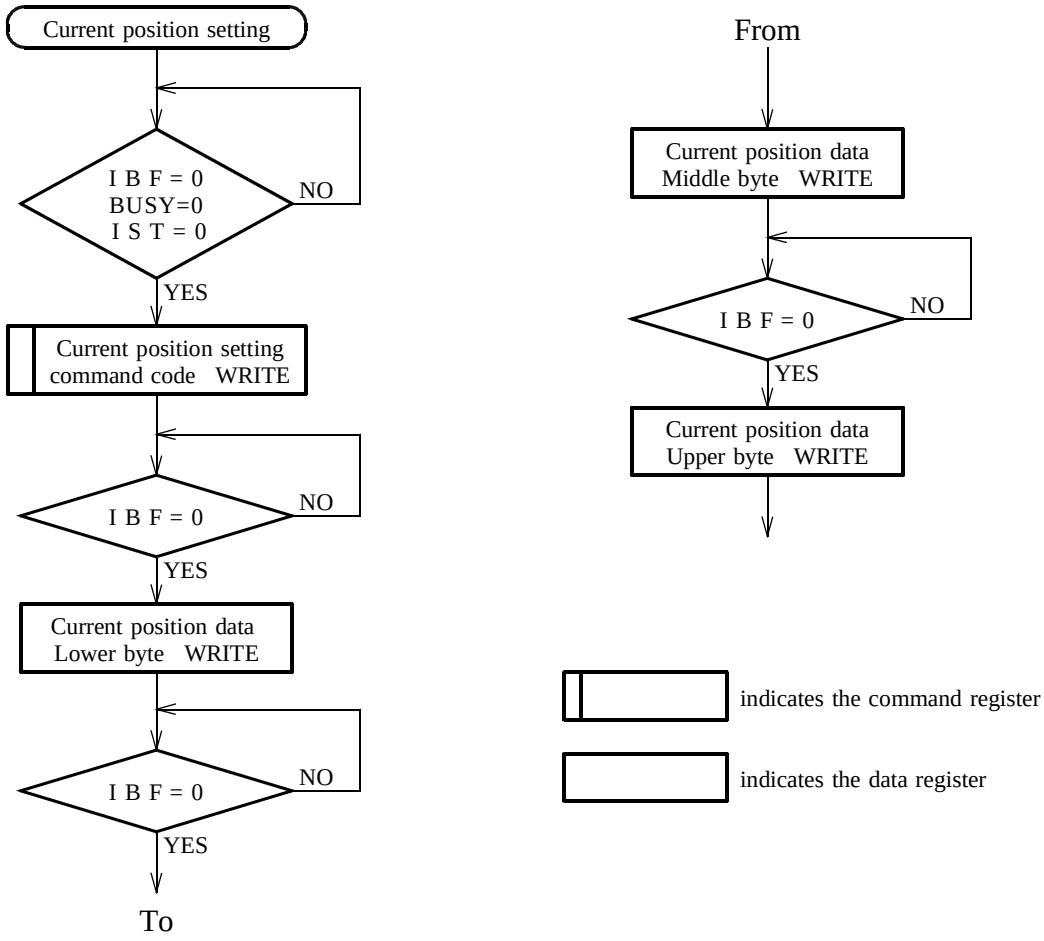


Fig.3-58. Flow chart of current position setting command

3-1-5-2. Auxiliary output command

This command is used to set the conditions of signal output via auxiliary output terminals AUXO0 through AUXO7. There is a delay of approximately 40 microsecond between the receipt of this command for auxiliary output and the actual change of conditions at the output terminal. The auxiliary output signal shifts to the "H" level once after resetting, and then it shifts to "L" upon internal initialization finish. This command is effective even during pulse output by the PPMC-112.

This command code must be written only after the status register's IBF and IST bits are checked. The auxiliary output data must be written while checking the IBF bit.

<Auxiliary output command/data>

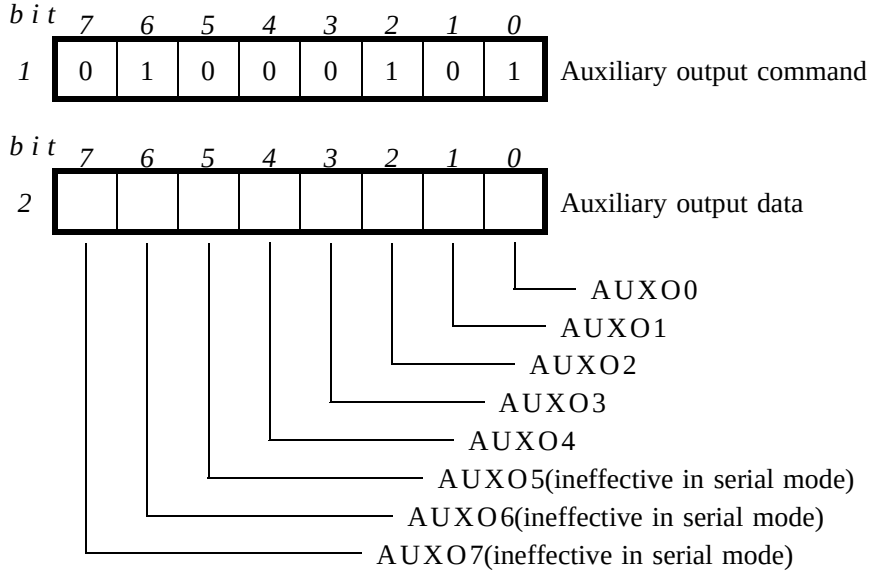


Fig.3-59

This command must be used carefully during pulse output because the PPMC-112 is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to the output of an auxiliary input signal (IST bit = "0").

Fig. 3-60 is a flow chart indicating the flow of issue of the auxiliary output command.

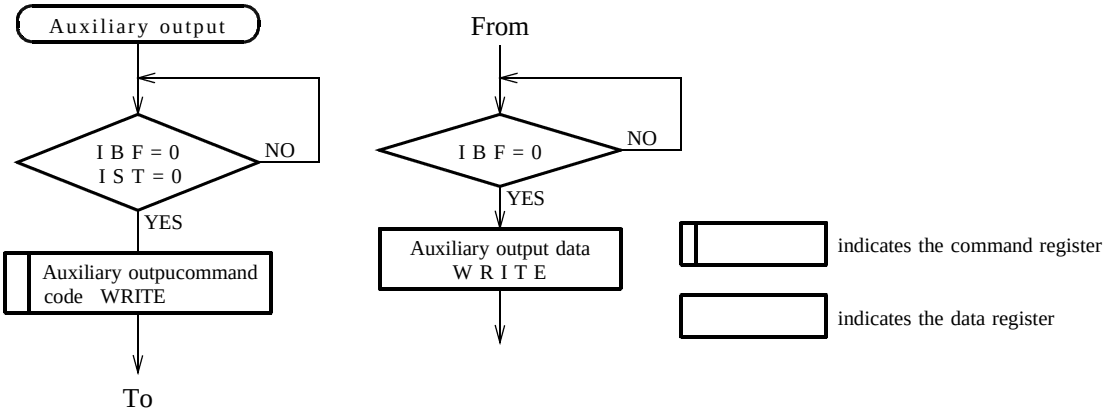


Fig.3-60. Flow chart of auxiliary output command

3-1-5-3. High speed limit effective speed setting command

This command is used to set a range of speed which allows high speed limit signals (BHL* and FHL*) of the PPMC-112 effective. This command can be used only when there is no pulse output. It is necessary to set a 16-bit effective speed pulse rate after the command code.

This command code must be written only after the status register's IBF, IST and BUSY bits are checked. 16-bit data on the pulse rate must be written in the correct order starting with the lower byte and then the upper byte, while checking the IBF bit.

Detection of a high speed limit signal corresponding to the direction of rotation during pulse output at any speed equivalent to or exceeding the speed set by this command leads to decelerating stop even during pulse output by any command. Contrarily, if a high speed limit signal corresponding to the direction of rotation is detected during pulse output at any speed lower than the speed set by this command, the high speed limit signal shall be disregarded and the designated pulse output shall be continued even during pulse output by any command except when pulse output is performed by the continuous high speed operation command (command for high speed operation up to the high speed limit). Detection of a high speed limit signal during pulse output by the continuous high speed operation command leads to an unconditional decelerating stop, regardless of the default value or the setting by the high speed limit effective speed setting command. The default value of high speed limit effective speed is the value of pulse rate at high speed that is set at initialization setting.

If the PPMC-112 engages in pulse output by either of the three (3) commands for constant speed operation, continuous constant speed operation or constant speed origin search, it continues the designated pulse output without making a decelerating stop even if a high speed limit signal (BHL* or FHL*) is detected because it operates within high speed limit effective speed normally. Rotation of the stepper motor by any of these three (3) operation commands implies a rotation speed not exceeding the self-starting frequency of the stepper motor used; therefore, there is only a rare occurrence of dislocation due to becoming out of step when the rotation of the stepper motor comes to a stop. If, however, the instantaneous speed change command or accelerating/decelerating speed change command is received when the stepper motor is rotating by one of the aforementioned constant speed operation commands, the stepper motor may continue to rotate at a speed equivalent to or exceeding its self-starting frequency until it reaches the point where the instantaneous speed change signal (BL* or FL*) is set. Pulse output comes to an immediate stop if the PPMC-112 detects a limit signal (BL* or FL*), in which case the out-of-step condition of the stepper motor may cause dislocation.

This high speed limit effective speed setting command is provided to prevent such dislocation due to the stepper motor being out of step.

Figures 3-61 and 3-62 show examples of operations while setting an effective speed for the high speed limit using this command.

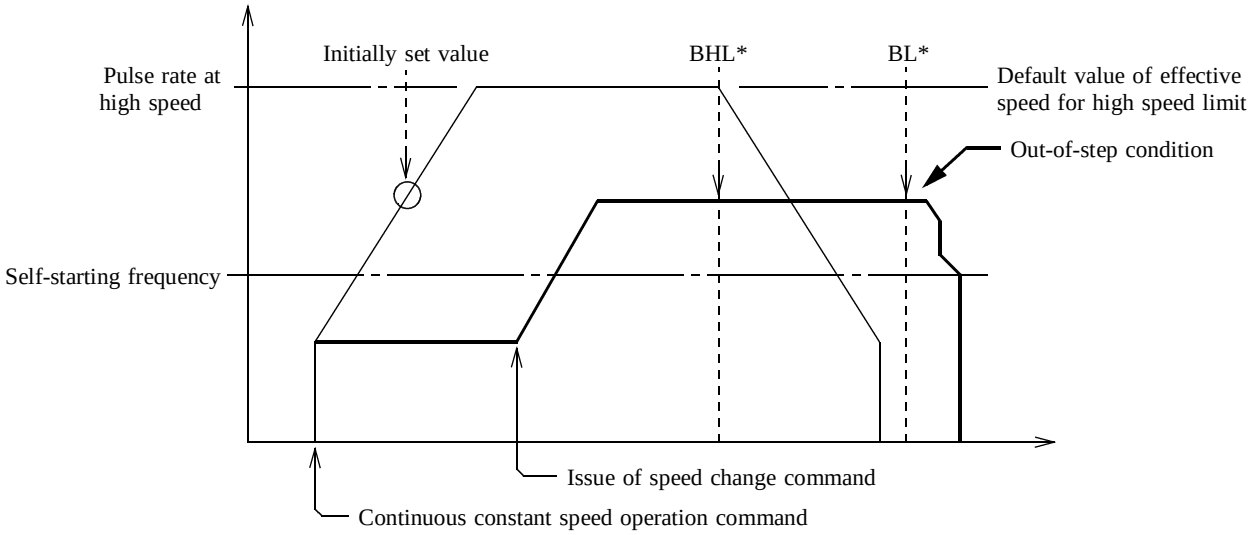


Fig.3-61. When effective speed for high speed limit is not set

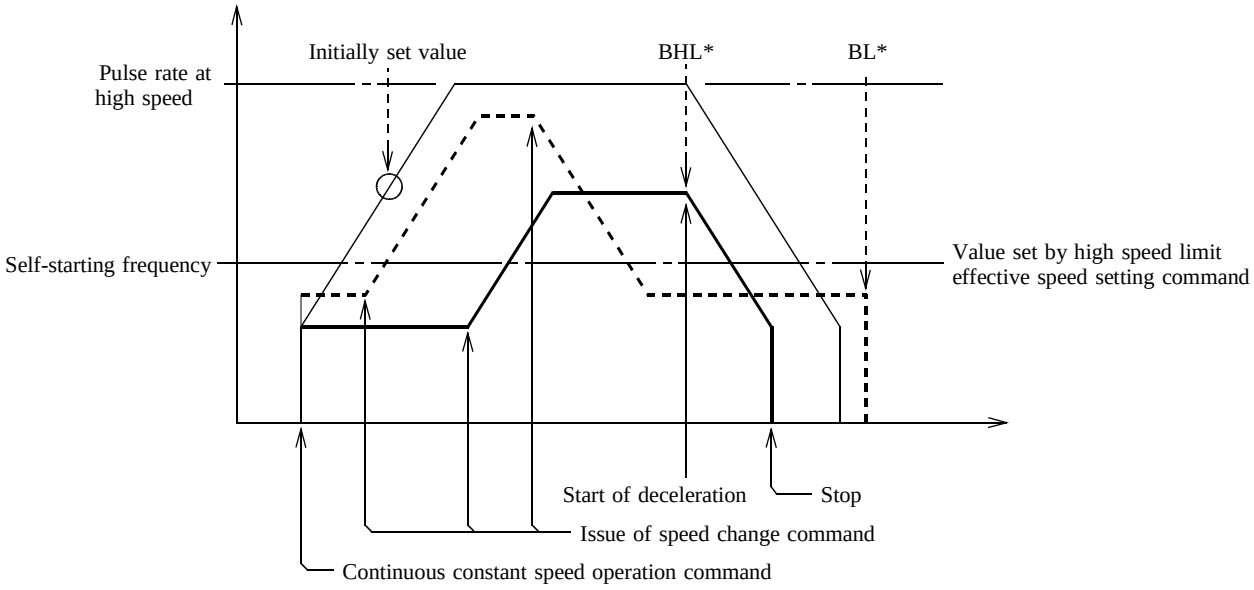


Fig.3-62. When parameters for setting effective speed for high speed limit are set without exceeding self-starting frequency

<High speed limit effective speed setting command/data>

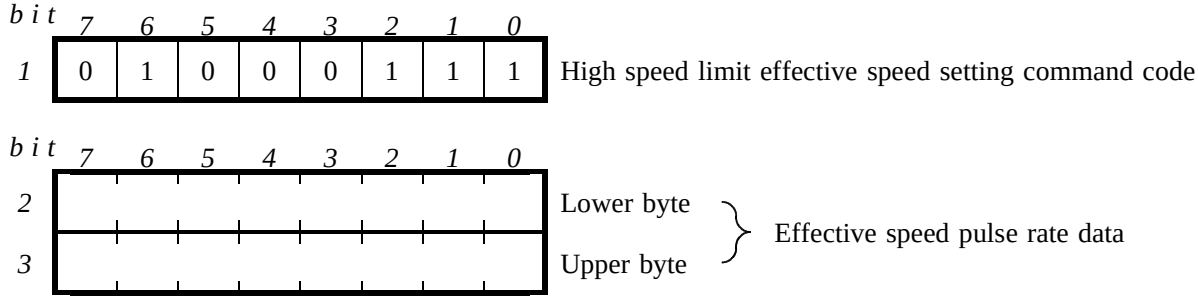


Fig. 3-63

The high speed limit signal FHL* is effective during CW pulse output, while the BHL* signal is effective during CCW pulse output. The mode of stop upon detection of a high speed limit signal varies as detailed in Table 3-6, depending on three (3) conditions: namely, (1) operation command, (2) value of pulse rate set for effective speed for the high speed limit, and (3) pulse output speed at the time of detection of the high speed limit signal.

Table 3-6. Mode of stop upon detection of high speed limit

Command	Operational state at the detection of high speed limit			
	Start up	Acceleration	High speed limit effective speed or over	Deceleration
Constant speed operation	Invalid	x	Valid	x
Accelerating/ decelerating operation	Valid	Valid	Valid	Invalid
Continuous constant operation	Invalid	x	Valid	x
Constant speed origin search	Invalid	x	Valid	x
Continuous high speed operation	Valid	Valid	Valid	Invalid
After speed alteration command	x	Valid	Valid	Invalid
Single step	Invalid	x	x	x

Valid : It decelerates and halts
Invalid : Command is ignored.
x : Not applicable

When connected to SYNC-101, high speed limit is used as Y axis limit (FL, BL), therefore, high speed limit setting becomes necessary. Fig 3-64 is a flow chart indicating the flow of issue of the high speed limit effective speed setting command.

Fig. 3-64 is a flow chart indicating the flow of issue of the high speed limit effective speed setting command.

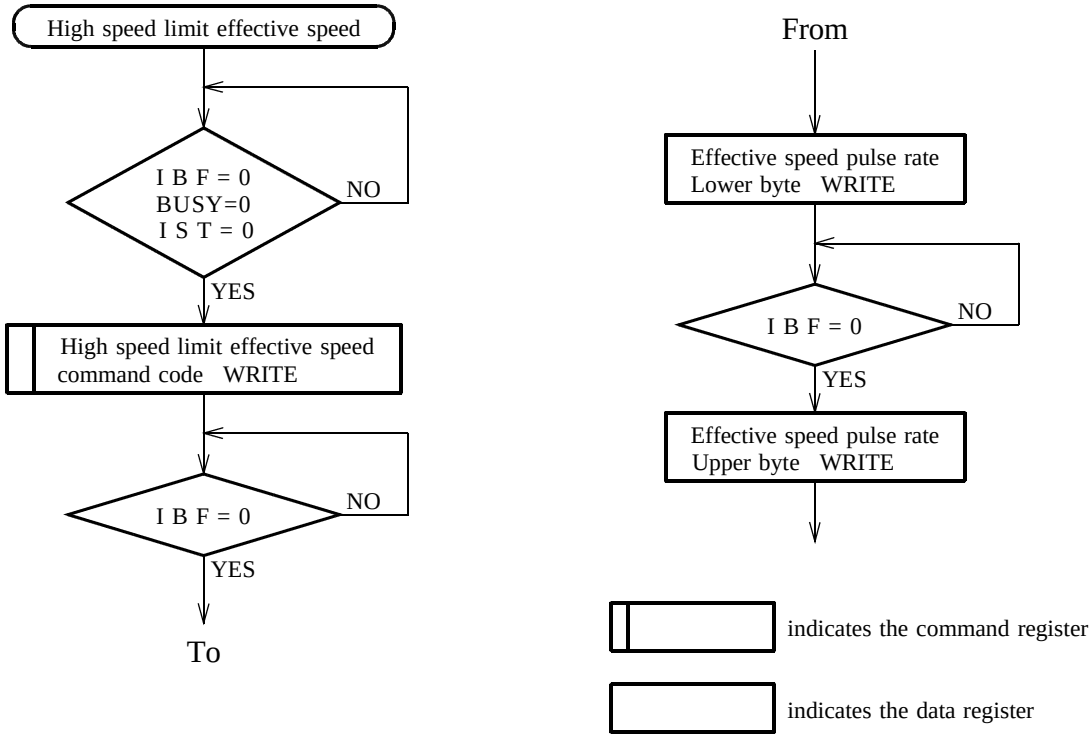


Fig.3-64. Flow chart of high speed limit effective speed setting

3-1-5-4. Interlock release position setting command

This command is used to set the position at which interlock signal INTLK* turns to be "H," and only executable while pulse output is suspended. The execution of this command turn INTLK* signal to "L," and when the following acceleration/deceleration or constant speed operation command drives the axis from starting point to the designated release point which is set by this command, INTLK* signal changes to "H." If the number of data set by this command is smaller than 20, the command will be processed as command error (Error Code 12), and the INTLK* signal won't be released. Alternatively, if the value set by this command is bigger than the operational pulse of following operational commands, it will be released after the execution of following operational commands.

Before writing this command code, status register IBF, IST, and BUSY bits must be verified, and when writing interlock release position setting data, first IBF bits must be verified, then 3 byte data from the lower byte in order can be written.

<Interlock release position setting command/data>

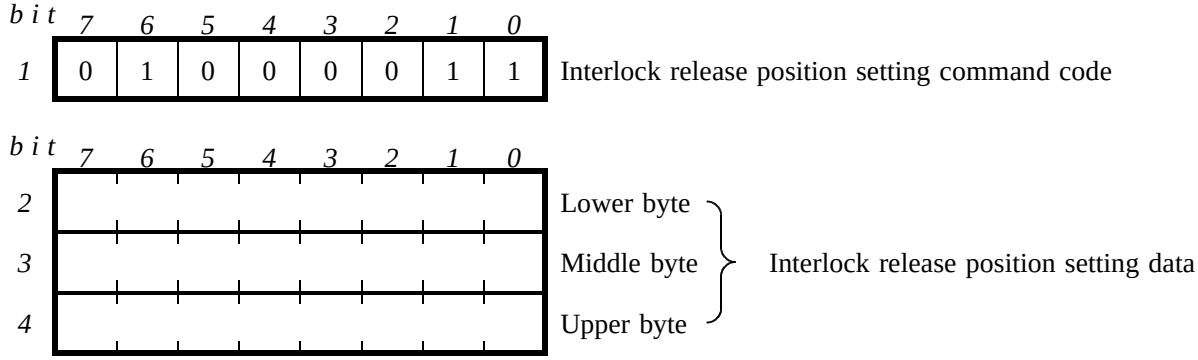


Fig.3-65

Fig. 3-66 is a flow chart indicating the flow of issue of the Interlock release position setting command.

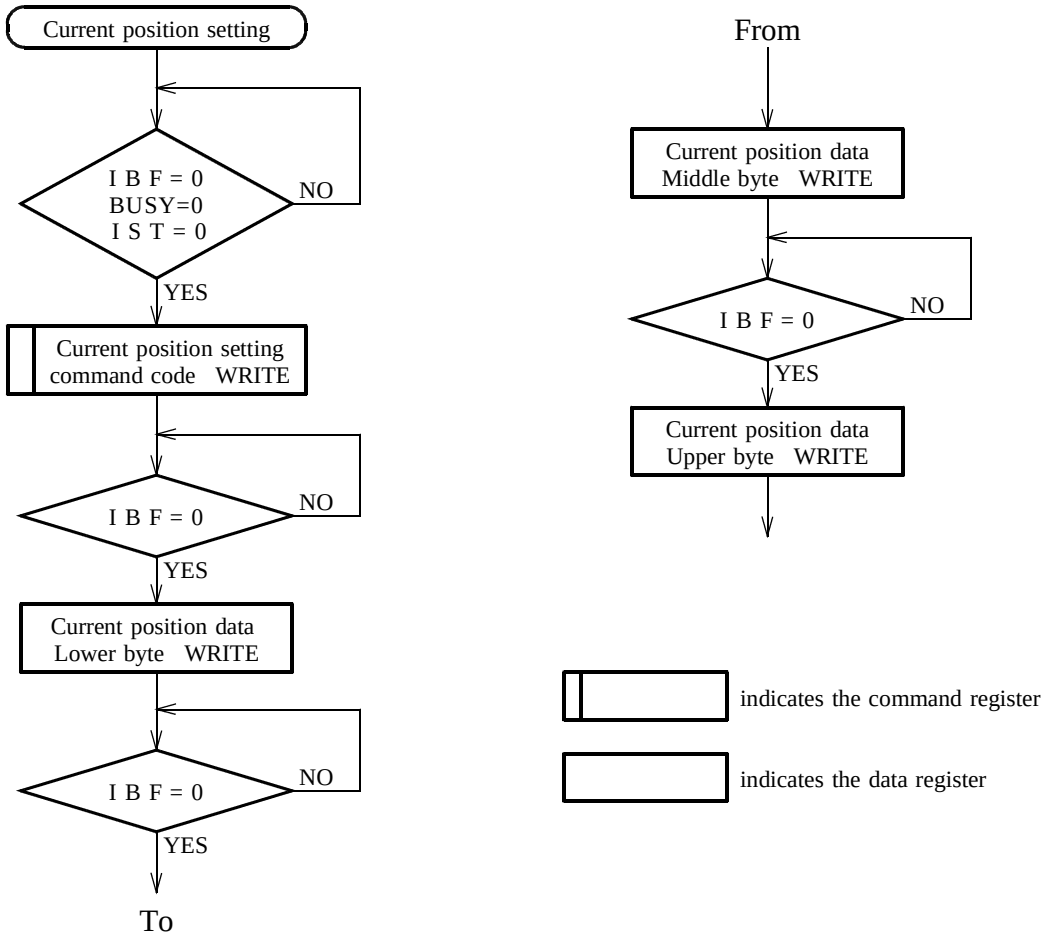


Fig. 3-66. Flow chart of interlock release position setting command

3-1-5-5 Pulse width setting command

This is the command to set the pulse width of Pout output, so that PPMC-112 can be used to drive various kind of motors. Fig.3-67 shows the control command.

<Auxiliary output command/data>

bit	7	6	5	4	3	2	1	0	
1	0	1	0	0	0	1	0	1	Pulse width setting command code

bit	7	6	5	4	3	2	1	0	
2									Pulse width data

Fig.3-67

Pulse width data is given in the form of binary data 1-byte code based on the base clock pulse width as a unit. When the given pulse width data is "0" or bigger than the initial setting high speed rate, the error code 17 is returned. The default value is 4 clock 2 microsecond (2MHz clock selection).

3-1-6. SYNC-101 start control command

When PPMC-112 and SYNC-101 are used together in parallel mode, before start driving PPMC-112, SYNC-101 is to be given the interpolation command. PPMC-112 outputs pulse following its own commands, but at the same time it needs SYNC-101's operational information to generate directional signal output for X and Y axis, and limit signal checking. Therefore, the SYNC-101 start control command is available.

The following information is necessary: In the circular interpolation command, the start quadrant number and rotation direction; On linear interpolation command, the operate direction quadrant number; In single axis operation, axis selection and its direction, and whether it is in origin search or not. These information is compacted to 1 byte code in this command.

This command needs to be executed before giving operational command to PPMC-112. Following this command, PPMC-112 sets the directional signal, and generates the limit checking data. In circular interpolation operation, it watches the quadrant change signal, and when it happens, it reverses the X axis or Y axis directional signal.

This command consists of only command code, and lacks data part. It is only valid while halted (BUSY=0.) This command needs to be written after checking status register IBF and IST bits, and busy bits. This command is the same as SYNC-101 control command. For the details of SYNC-101, please refer to SYNC-101 specification.

<SYNC-101 Start control command/data>

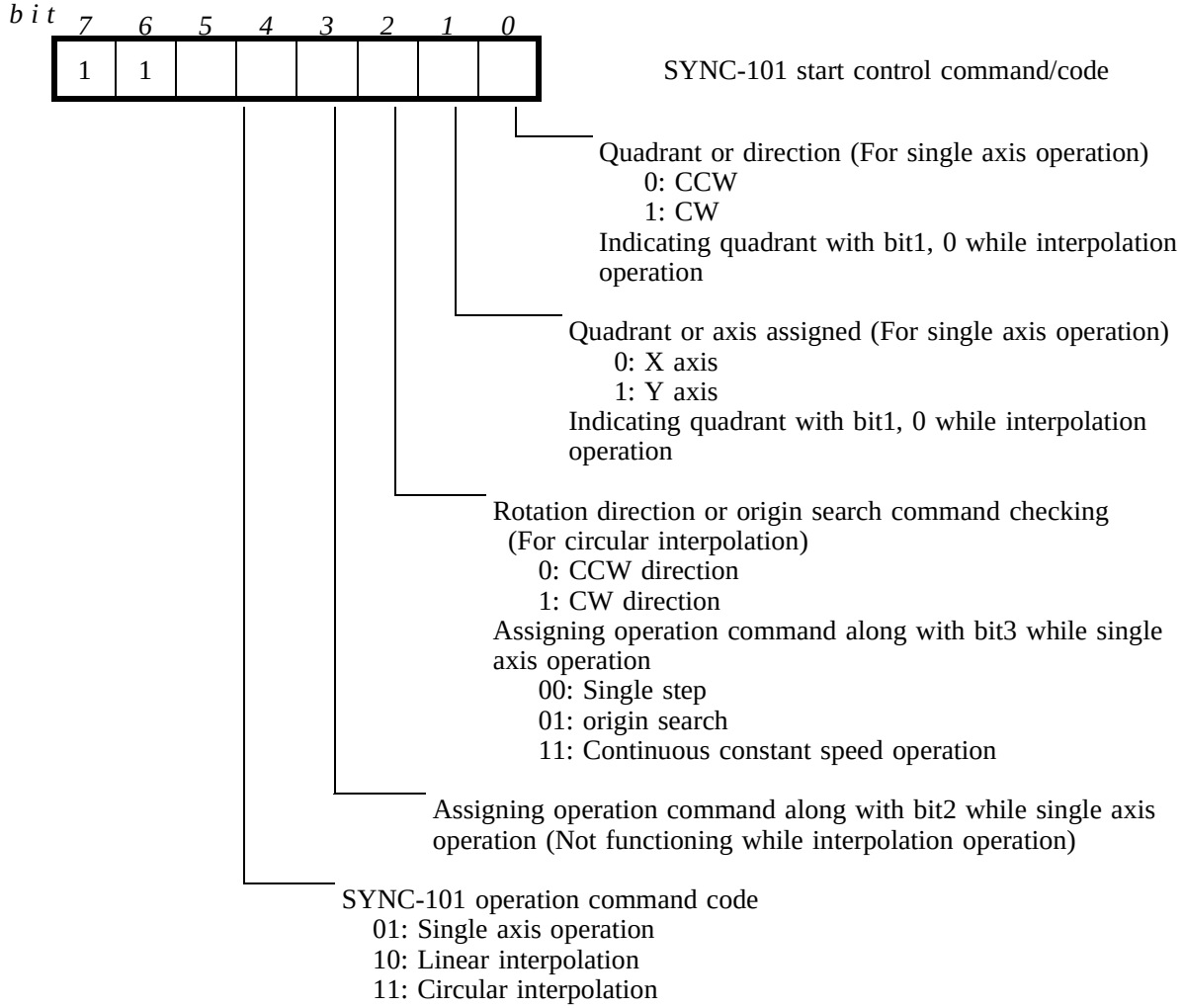


Fig.3-68

3-2. PPMC-112 control in serial mode

In serial mode, PPMC-112 operates according to the command codes and data, which are given from the host processor control frame via communication line. The actual contents of command cods are basically the same as those in parallel mode. For the details of commands and operations, please refer to parallel mode description in section 3-1 (page 3-1).

In this section, the communication protocol and control frame structure, and the difference from the parallel mode commands are explained.

3-2-1. Communication protocol

PPMC-112 has two kinds of communication mode, one is 9-bits binary communication mode, and the other is 8-bits ASCII mode communication. The physical layer of communication is handled via RS-232C, RS-422, or RS-485. In case of multi-drop, lines such as RS-422 or RS-485 can be used. The logical control of communication is handled by half polling protocol, and in any communication mode, it will be driven from the master processor.

The communication speeds which are supported are 125kbpS, 62.5kbpS, 31.25kbpS in binary mode, and 83.33kbpS, 41.67kbpS and 19.2kbps in serial mode. Fig.3-69 shows example of system layout. These communication modes and baud rates are set by MOD0 to MOD2, PPMC-112 mode setting input. For the details, please refer to the table 3-6 and chapter 2 section 2-3-3 (page 2-11.)

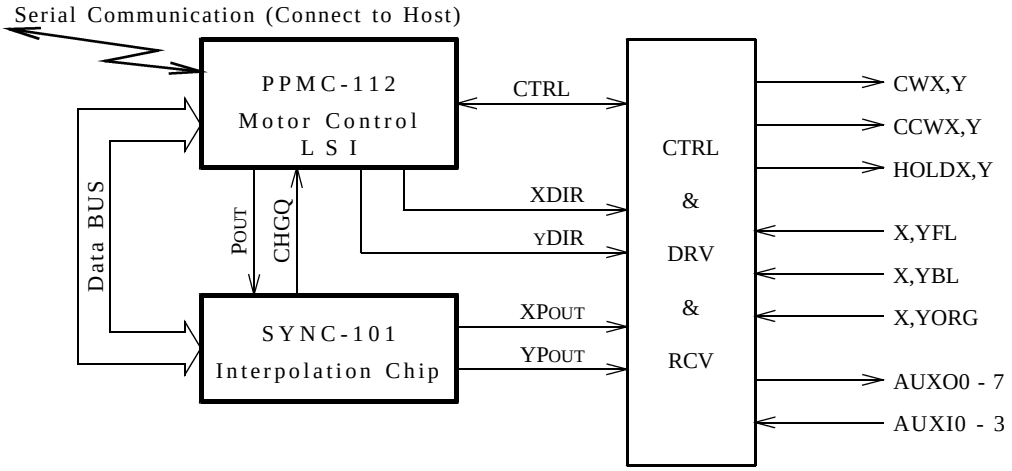


Fig.3-69. Sample system configuration

Table 3-6. Communication protocol and communication speed

MOD2	MOD1	MOD0	Operation baud rate/communication mode and baud rate
x	0	0	Parallel mode
0	0	1	Binary mode 31.25kbpS
0	1	0	Binary mode 62.5kbpS
0	1	1	Binary mode 125 kbpS
1	0	1	ASCII mode 19.2kbpS
1	1	0	ASCII mode 41.67kbpS
1	1	1	ASCII mode 83.33kbpS

3-2-2. Frame structure

The communication frame consists of the following three parts. The first byte is control code including address, the following part is variable length data section, and for the last part is 1 byte check sum is added.

The frame such as busy check (polling frame) needs high speed communication, therefore the special frame without data part is available.

The control code has a special internal structure, and a system that enables multi-drop communication to take place at high speed. In 9-bits binary mode, bit 8 is "1," and in 8-bits ASCII mode, bit 7 is "0".

This structure helps PPMC-112 to detect the start of the frame easily.

Frame structure

Control command	Data section	Check sum

Fig. 3-70

3-2-2-1. 9-bits binary mode

This communication mode protocol depends on the PPMC-112's special hardware. Therefore, 8-bits UART, which is normally used, is not applicable in this case. Our company offers master controller MWSC-101 to use this high speed communication protocol. This device has a physical layer to process this special protocol, as well as layer 1 and 2. Therefore, users do not necessarily have detailed information on this protocol. (Our company is preparing the specification for this protocol, so please tell us if you need one.)

The basic structure of the frame is as stated in the previous section. Compared to the ASCII mode which is explained in the next chapter, the higher speed operation is realized by sending/receiving binary data as they are (in ASCII mode, 1 byte binary data needs to be divided to 2 byte for sending/receiving them.) thus improving the overall system efficiency.

3-2-3. 8-bits ASCII mode

In this section, we explain the ASCII mode communication protocol that is indigenous to PPMC-112. This protocol can utilize the normal UART hardware that is employed in personal computers, thus requires no special hardware.

Table 3-7 shows command codes list in ASCII serial mode.

Table 3-7. List of ASCII serial mode command codes

Command	Commamd/ Data		Function
Initialization	1, 2	00CCxxDD	CC: Base clock assigned DD: Acceleration/ deceleration mode assigned. Start speed rate at acceleration/ deceleration operation (Normally set to self start frequency). High speed rate at acceleration/ deceleration operation (Set to maximum operation speed). Set the number of pulse from start speed to high speed
	3, 4	Start pulse rate (L)	
	5, 6	Start pulse rate (H)	
	7, 8	High speed pulse rate (L)	
	9, 10	High speed pulse rate (H)	
	11, 12	Acc/ dec pulse rate (L)	
	13, 14	Acc/ dec pulse rate (H)	

x : Invalid

Command		Commamd/ Data		Function
Drive Command	Instantaneous stop	1, 2	10xI0000	Immediately halts the pulse output
	Decelerate and stop	1, 2	10xI0001	Deceleration to start speed and halts
	Single step	1, 2	10xI0010	Output a pulse to the designated direction
	Acceleration/	1, 2	10DI0011	Acceleration/ deceleration from start speed to high speed. Number of drive pulse is assigned in 3 bytes. Input data from lower byte and up in order
	deceleration	3, 4	Drive pulse number (L)	
	operation	5, 6	Drive pulse number (M)	
		7, 8	Drive pulse number (H)	
	Constant speed	1, 2	10DI0100	Constant speed drive at assigned speed. Pulse rate is assigned in 2 bytes. Number of drive pulse is assigned in 3 bytes
	operation	3, 4	Constant pulse rate (L)	
		5, 6	Constant pulse rate (H)	
		7, 8	Drive pulse number (L)	
		9, 10	Drive pulse number (M)	
		11, 12	Drive pulse number (H)	
	Continuous	1, 2	10DI0101	Constant speed drive till limit at assigned speed. Pulse rate is asigned in 2 bytes
	constant speed	3, 4	Constant speed pulse rate (L)	
	operation	5, 6	Constant speed pulse rate (H)	
	Continuous	1, 2	10DI0110	It deceleration and halts following acceleration/ deceleration operation, or high speed limit detection
	high speed			
	operation			
	Constant	1, 2	10DI0111	Constant speed drive at assigned speed to the origin point
	speed	3, 4	Constant pulse rate (L)	
	origin search	5, 6	Constant pulse rate (H)	
	Immediate	1, 2	10001000	Change to the assigned speed immediately. Target pulse rate is assigned in 2 bytes
	speed	3, 4	Target pulse rate (L)	
	change	5, 6	Target pulse rate (H)	
	Acceleration/	1, 2	10001001	Accelerates/ decelerates to the assigned speed. Target pulse rate is assigned in 2 bytes
	deceleration	3, 4	Target pulse rate (L)	
	for speed change	5, 6	Target pulse rate (H)	

I : Finish interrupt assigned. 0 = interrupt assigned

D : Drive direction. 0 = CW, 1 = CCW

Command		Commamd/ Data		Function
Auxiliary command	Finish status	1, 2	01000000	Reads finish status rgister
	Error code	1, 2	01000001	Reads error code register
	Current position reading	1, 2	01000010	Reads current position data (return 3 bytes data)
	Current position setting	1, 2	01000011	Sets the current position. Current position is set in 3 bytes. Input data from lower bytes in order
		3, 4	Current position (L)	
		5, 6	Current position (M)	
		7, 8	Current position (H)	
	Auxiliary input	1, 2	01000100	Read auxiliary input port status
	Auxiliary output	1, 2	01000101	Change auxiliary output port status. Input 1 byte of output port bit pattern
		3, 4	Auxiliary data	
	Control input	1, 2	01000110	Reads status of control input port (limit signal)
	High speed limit	1, 2	01000111	Sets the effective speed for the high speed limit. Effective speed is assigned in 2 bytes. Input data from lower byte in order
	effective speed	3, 4	Effective speed (L)	
	setting	5, 6	Effective speed (H)	
	Interlock	1, 2	01001000	The interlock release position is set by the number of pulse from start position. When it reaches to assigned value, interlock signal change to "H". Position is set by 3 bytes data inputting from lower byte in order
	release	3, 4	Interlock release position (L)	
	position	5, 6	Interlock release position (M)	
	setting	7, 8	Interlock release position (H)	
	Acceleration/ deceleration	1, 2	01001001	Reads accelerate/ decelerate table data
	table reading			
	Version reading	1, 2	01001010	Reads version code
	Pulse width setting	1, 2	01001011	Pout pulse width setting
		3, 4	Pulse width	
	Error counter reading	1, 2	01001100	Reads error counter
Busy check		0	1000AAAA	No command code. Only set address by AAAA (*1)

In this table, only data parts are shown from Fig. 3-70 of ASCII frame structure. However, *1 busy check does not have data section, but only control code.

3-2-3-1. The structure of control code

Only the control code has bit 7 (MSB) as “1”, and has the structure shown in the table below. This protocol takes into consideration the possibility of supporting other devices. Bit 6 is set to “0” when PPMC-112 is selected. Bit 3 to 0 assign slave address. Bit 5 and 4 shows frame class.

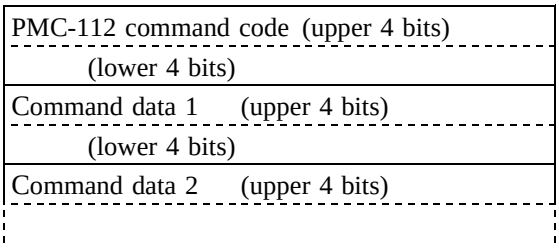
Table 3-8. The structure of control code

Bit	Value	Descriptions	
		Master transmit frame	Slave reply frame
7	1	Shows control code (Except control code = 0)	
6	0	Device selection bit (PPMC-112 = 0)	
5,4 Frame Class	0 0	Busy check frame	Busy status reply
	0 1	Command data frame	Acknowledge, ready reply
	1 0	Not defined	Reply with data
	1 1	Not defined	Reply with assign data
3,2,1,0	Device address (Selected by DVADR3-DVADR0)		

3-2-3-2. The structure of data section

Data section has variable length, and there are also some frames without data section. Normally, 1 byte binary data is expressed in 2 byte ASCII codes. In this case, the data structure is the same as one that is translated in ASCII from PPMC-112 parallel mode command code in a straight manner. Therefore, all of the bit 7 (MBS) of data section is “0.”

The special data that can be expressed in only 1 byte (convertible to 7 bits), that is, finish status, error code, auxiliary input and version code, they are not going through normal ASCII conversion process, but the special conversions are applied.



Data section starts from command code to PPMC-112, then the necessary data is added. Command code and data are all divided into upper 4 bits and lower bits, and converted to ASCII 2 bytes.

Fig. 3-71 the structure of ASCII data section

Table 3-7 ASCII serial mode command list shows only the data section of the above table.

* Control code, bit 7 =1
* Data section and check sum, bit 7=0
* Check sum is calculated by binary adding data from control code to the end of ASCII converted data section, then reversing all bits, and setting bit 7=0.

3-2-3-3. Check sum calculation

Check sum is calculated by binary adding data from control code to the end of ASCII converted data section, then reversing all bits, and setting MSB (bit 7) to "0".

3-2-3-4. Control protocol

In both master fame and slave frame, control code bit 5 and 4 shows frame class. (Section 3-2-3-1) Communication procedure is as follows.

1. Master driven transmit frame

The only transmit frames from the master are these 2: busy check (polling) frame and PPMC-112 operation data command frame.

Polling frame: No data section, and consists of 2 bytes of only control code and check sum. Special frame only available in serial mode. In case of serial mode, there is no status register and interrupt signal as parallel mode. And in multi-drop communication, slave side can not transmit without knowing the status of transmit circuit. Therefore, the master always needs to watch the status of PPMC-112 by polling.

Command data frame: Command code and data to drive PPMC-112 is on here.

It is possible to use all the available commands in parallel mode except ones for SYNC-101 control.

SYNC-101 control command is explained in chapter 3 section 2-4.

2. Reply frame from slave

PPMC-112 (Slave) replies 4 class of frames.

Reply to the polling frame: when PPMC-112 is outputting pulse, it replies busy, and when PPMC-112 is halted, it replies ready. To the polling frame that is accepted immediately after PPMC-112 stop output, the frame added finish status is replied. When PPMC-112 is in operation (busy) and it is immediately after the interlock release, this special data value is set to "00h."

Reply to the data demand command: Among the auxiliary commands, status or data reading commands and current position data command, which demand various status or data, are replied with data added frame. The content of replied data is the same as the ones in parallel mode.

Reply to operation command and parameter data setting command: PPMC-112 judges if the command is right and if it is acceptable, then in the case of right executable command, it replays acknowledge frame, and in other case, special data (error code) added replay frame is sent back.

The control command sent while PPMC-112 is waiting for the command data section is recognized as the start of new frame, thus the received control code and command up to that point are discarded, and no error process routine is executed.

3-2-3-5. Communication error prevention process

PPMC-112 adds check sum to each frame to prevent communication error. When there is check sum error in the received data, error code "W" is replied.

Internal UART detects framing error and over run error, but these error codes are recorded internally, and no reply is sent back. This is because when several PPMC-112 is connected to the same line, this kind of hardware error can not be immediately judged if it was the communication to that particular PPMC-112.

Therefore, host processor waits enough time that is considered to be normal before receiving the reply, then execute the time out error process. If the case like this is often observed, hardware or noise environment may need to be improved. In some cases, decreasing the communication speed may be considered to be effective, but can damage the overall system performance. We are preparing to offer the MS-DOS driver for the PPMC-112 control in ASCII mode.

3-2-3-6. ASCII mode error control

In parallel mode, error codes are binary code from "00h" to "14h." In ASCII mode, the codes are converted to alphabetical codes and replied as 1 byte code. In case of hardware communication error, the error code is not replied as explained above, but the error code reading command can confirm this code.

Table 3-9 shows ASCII serial mode error code table for PPMC-112.

Table 3-9. ASCII serial mode error code list

Error code		Descriptions of errors
16 Hex	ASCII	
41	A	
42	B	Received command not defined.
43	C	No initialization command provided.
44	D	Not operable due to limit signal or alarm signal
45	E	Not operable as operation pulse number "0" is designated.
46	F	Received halt, decelerate and halt, or speed change command whilst at halt
47	G	Received data not preceded by command
48	H	(Not applicable)
49	I	Not operable as origin search command is received while origin signal is already fed.
4A	J	Received the command, which is unable to process during BUSY status.
4B	K	Initial set rate data is abnormal. (Start pulse rate must be 25 or over, high pulse rate must be 8 or above) or external mode initial setting rate is abnormal.
4C	L	Excessively small number of pulse at initial setting (acceleration/deceleration pulse number must be 8 or over.)
4D	M	Abnormal initial rate data (RH = RL or RH > RL)
4E	N	Abnormal steps of acceleration/deceleration in performed initialization command for the free-curve acceleration/deceleration method.
4F	O	Received speed change command while decelerating due to detection of high speed limit.
50	P	Received deceleration command while decelerating.
51	Q	Speed that exceeds the speed range is designated. (>RL <RH)
52	R	Pulse width setting is "0" or bigger than the one at high speed operation.
53	S	Not controllable due to excessively small value of interlock setting.(<20)
55	U	No acceleration/deceleration is operable as speed range is out of acceleration/deceleration range
56	V	SYNC-101 control data error
57	W	Check sum error
58	X	Communication hardware error

3-2-4. SYNC-101 control command in ASCII mode

In serial communication mode, apart from previously stated PPMC-112 control command and busy check command, command codes for combined operation with SYNC-101 is available. SYNC-101 is connected to PPMC-112 external bus, and indirectly controlled through this bus.

When combined with SYNC-101, following 4 basic commands are available for SYNC-101 operation.

1. Circular interpolation operation command

   This is constant speed or acceleration/deceleration circular interpolation command. Start quadrant, start phase angle, rotation radius, rotation direction, and drive pulse number have to be given. In constant speed operation, pulse rate is also needed.

2. Linear interpolation operation command

   This is the linear interpolation operation command for constant speed operation or acceleration/deceleration operation. Quadrant assignment, Drive direction angle, drive pulse have to be given. In constant speed operation, pulse rate is also needed.

3. Single axis operation command

   This is the command for X or Y axis. There are 3 kinds of 6 commands: Single step, Origin search, and continuously constant speed operation.

4. Current position read command

   This command reads the halt position following the termination of operation. It returns X and Y axis coordinates (and finish phase angle at halt in circular interpolation operation).

3-2-4-1. Circular interpolation operation command

Circular interpolation operation command gives data such as start quadrant position, rotation direction of circular movement, number of drive pulse. The actual operation consists of PPMC-112 operational command and SYNC-101 interpolation command.

In circular interpolation operation, the output pulse from PPMC-112 is used as master pulse for SYNC-101, and it delivers the pulse in at synchronous timing to X and Y axis so that they operate in a way that the composition of X and Y axis movement goes along the rim of its assigned radius circle. In this case the speed of contact point on the circle is consistent with the PPMC-112 output pulse rate. Therefore, if it is the constant speed operation, it goes along the circle at constant speed, and if it is acceleration/deceleration operation, it starts slowly on the circle, and accelerates gradually to high speed operation, then decelerate towards the stopping point on the circle, and halts.

Table 3-10. Circular interpolation command

Sequence	Name	Descriptions
1	Control code	1001aaaa (aaaa is device address)
2,3	Command word	bit7,6,5,4=1111, bit 3: acceleration/deceleration = 1, constant speed = 0 bit2: CW=0, CCW=1, bit1, 0:Start quadrant. For example, constant speed first quadrant start CW, then ASCII code is "F", "0".
(4,5)	Pulse rate L	Same pulse rate as one given to PPMC-112. 16 bits binary data is converted4 byte ASCII to feed. (Inserted only in case of constant speed operation)
(6,7)	Pulse rate H	
8,9/4,5	Drive pulse # L	Same pulses number as one given to PPMC-112. 24 bits binary data is converted to 6 bytes ASCII to feed.
10,11/6,7	Drive pulse # M	
12,13/8,9	Drive pulse # H	
14,15/10,11	Circle radius L	Pulse unit circular radius is converted to 4 bytes ASCII code for feeding. Max value is 32,767.
16,17/12,13	Circle radius H	
18,19/14,15	Start phase angle L	0 to pi/2 start position expressed in 1/32,768 radian as a unit, which has phase degree 16 bits binary data, are converted to 4 bytes ASCII code.
20,21/16,17	Start phase angle H	
22/18	Check sum	Control code, command, and data check sum

Device address aaaa matches to DVADR3 to 0 input.

Start quadrant: 00=1st quadrant, 01=2nd quadrant, 10=3rd quadrant, 11=4th quadrant

Start phase degrees: Within the quadrant assigned by the command code, the degree measured towards CCW direction (counter clock wise)

For the command code and data section, binary data is converted to ASCII 2 byte (No description in the above table).

3-2-4-2. Linear interpolation operation command

Linear interpolation operation command sets the each X and Y axis operation direction, operation pulse number and operation mode. Same as circular interpolation operation, the actual operation consists of PPMC-112 operation command and SYNC-101 interpolation command.

In this command, the pulse delivered to X and Y axis is given at constant proportion so that they go along the designated operation direction. That is the same as in the case of circular interpolation operation, the combined operation speed to that direction is consistent with master pulse speed.

Table 3-11 Linear interpolation command

Sequence	Name	Descriptions
1	Control code	1001aaaa (aaaa is device address)
2,3	Command word	bit7,6,5,4=1110, bit 3: acceleration/deceleration = 1, constant speed = 0 bit2: No meaning bit1, 0:Start quadrant
(4,5)	Pulse rate L	Same pulse rate as one given to PPMC-112. 16 bits binary data is converted4 byte ASCII to feed. (Inserted only in case of constant speed operation)
(6,7)	Pulse rate H	
8,9/4,5	Drive pulse # L	Same pulses number as one given to PPMC-112. 24 bits binary data is converted to 6 bytes ASCII to feed.
10,11/6,7	Drive pulse # M	
12,13/8,9	Drive pulse # H	
14,15/10,11	Drive direction L	16 its binary data of 0 to pi/2 drive direction degree data which uses 1/32,768 radian as a unit is converted to 4 bytes ASCII code and used.
16,17/12,13	Drive direction H	
18/14	Check sum	Control code, command, and data check sum (bit 7=0)

Drive direction quadrant: 00=1st quadrant, 01=2nd quadrant, 10=3rd quadrant, 11=4th quadrant

Drive direction degree: Within the quadrant assigned by the command code, the degree measured towards CCW direction (counter clock wise)

3-2-4-3. Single axis operation command

Single axis operation command is used to adjust the origin point, or adjust the error in the interpolation operation. There are 3 kinds of command: Single step, constant speed origin search, and continuously constant speed operation (limit search.) This command is executed after selecting the axis and drive direction. Following this command, instead of PPMC-112 Pout, from SYNC-101 XPO or YPO, the same speed pulse is to be output.

Table 3-12. Single axis operation command

Sequence	Name	Descriptions
1	Control code	1001aaaa (aaaa is device address)
2,3	Command word	bit7,6,5,4=1101, bit 3,2: drive command bit1= axis selection, bit0=drive direction
(4,5)	Pulse rate L	Same pulse rate as one given to PPMC-112. 16 bits binary data is converted4 byte ASCII to feed. (Inserted only in case of constant speed operation)
(6,7)	Pulse rate H	
8/4	Check sum	Control code, command, and data check sum (bit 7=0)

Drive command: 00=single step, 01=origin search, 11=continuously constant speed operation (up to limit)
Axis selection; Select X or Y axis. X axis =0, Y axis=1.
Drive direction: Assign drives direction. For both axis, +direction=0, -direction=1.

3-2-4-4. Current position reading command

When combined with SYNC-101, PPMC-112 reacts to the current position reading command by returning X, Y axis present coordinate and phase degree (valid in circular interpolation), which are generated by SYNC-101 operation. The current position reading that is applicable only to PPMC-112 does not cause error, but there is no real meaning in circular interpolation operation.

Table3-13. Current position reading command

Sequence	Name	Descriptions
1	Control code	1001aaaa (aaaa is device address)
2,3	Command word	bit7,6,5,4=1100, bit 3,2,1,0=000, ASCII code is "C1"
4	check sum	Control code, command, and data check sum

SYNC-101 output data to this command is shown in Table 3-14.

Table 3-14. Reply for the current position reading command

Sequence	Name	Descriptions
1	Control code	1010aaaa (aaaa is device address)
2,3	X axis coordinate L	X axis coordinate output in 24 bit data of 2 binary format, ASCII 6 bytes.
4,5	X axis coordinate M	In circular interpolation operation, origin point is set at the center of the circle,
6,7	X axis coordinate H	and in linear interpolation operation, the start point is set as the origin point.
8,9	Y axis coordinate L	Y axis coordinate output in 24 bit data of 2 binary format, ASCII 6 bytes.
10,11	Y axis coordinate M	In circular interpolation operation, origin point is set at the center of the circle,
12,13	Y axis coordinate H	and in linear interpolation operation, the start point is set as the origin point.
14,15	Current position phase degree L	16 its binary data of 0 to pi/2 drive direction degree data which uses 1/32,768 radian as a unit is converted to 4 bytes ASCII code and used.
16,17	Current position phase degree H	
18	Check sum	Control code, command, and data check sum (bit 7=0)

Current position phase degree is the CCW direction degree within each quadrant, which is the same method used in circular interpolation. In circular interpolation operation, to which quadrant this phase degree is categorized, is judged by bye the sign of its coordinate data. The output data is the ASCII data that is converted from binary data with a meaning in the description.

3-2-4-5. Change in limit input

When interpolation processor SYNC-101 is connected, PPMC-112 watches X and Y axis limit status. However, in this case, each limit signal means XFL* (X axis CW limit) and XBL* (X axis CCW limit) instead of FL* and BL*, YFL* (Y axis CW limit) and YBL* (Y axis CCW limit) instead of high speed limit FHL* and BHL*, thus no high speed limit is connectable. (Please refers to the chapter 2, the descriptions of terminal signals.) Therefore, the meaning of finish status bit changes accordingly. (Please refers to next section.)

3-2-5. Differences in ASCII mode

In ASCII mode communication, to communicate in 8-bits code, the ASCII code conversion is used as explained in 3-2-3-2 section of this chapter. PPMC-112 can omit this ASCII conversion for higher speed communication as explained in 3-2-3-4 section. In this section, we explain the actual detail of this procedure.

3-2-5-1. Busy check command

To the busy check command, PPMC-112 responds with busy if it is the case, and if the operation has been finished, replies once with finish status. After that, while at halts, ready frame is replied. This command has a special frame prepared to enable high speed polling communication, and has no data section. The reply frame to this signal also does not carry data section if it is busy or ready. And, for the high speed polling system, high speed polling mode that is executed by HSP* signal input is available. When this signal is “L”, PPMC-112 does not read check sum byte to verify the normal communication, and simply returns busy or finish status. If host interface employs the same system, polling time at busy status can be reduced to half. This is based on the premise of very few communication error, Therefore to use this mode, a user needs to check the communication error conditions in advance.

Table 3-15. Busy check

Sequence	Name	Descriptions
1	Control code	1000aaaa (aaaa is device address)
2	Check sum	Control code check sum

Table 3-16. Reply in case of busy

Sequence	Name	Descriptions
1	Control code	1000aaaa (aaaa is device address)
4	Check sum	Control code check sum

Table 3-17. Reply in case of ready

Sequence	Name	Descriptions
1	Control code	1001aaaa (aaaa is device address)
2	Check sum	Control code and command word check sum

Table 3-18. Replay in case of finish operation

Sequence	Name	Descriptions
1	Control code	1011aaaa (aaaa is device address)
2	Finish status	ASCII code "0" to "7"
3	Check sum	Control code and command word check sum

This frame is replied only once after receiving the busy check command immediately after operation termination. From the second time, only acknowledgment is replied to busy check.

Table 3-19. Reply in case of interlock release position is passed

Sequence	Name	Descriptions
1	Control code	1011aaaa (aaaa is device address)
2	Status	ASCII code " " (space code "20h")
3	Check sum	Control code and command word check sum

This frame replies only once to the busy check immediately after passing the interlock release position. From the second time, normal busy status is replied until the end of operation.

3-2-5-2. Finish status code

PPMC-112 finish status code register that explains the cause of operation termination consists of 8 bits, but if there is no overlap of bits, there are only 8 kinds of code. Even if there is an overlap in the actual operation, the finish status register only holds the last cause of termination. However, in the case of halt due to limit, there are occasions that several limits are on at the same time. In this case, the smaller reply code ones are privileged. Therefore this code is converted to following 1 byte code before transmission. The replied status codes and their meanings are shown in Table 3-20.

Table 3-20

Code		Meaning of status code
16 Hex	ASCII	
30	0	Halt in normal operation
31	1	Halt due to halt command
32	2	Halt due to the detect of origin (ORG*) signal (or YORG*)
33	2	Halt due to the detect of CCW high speed limit (BHL*) signal (or YBL*)
34	4	Halt due to the detect of CW high speed limit (FHL*) signal (or YFL*)
35	5	Halt due to the detect of CCW direction limit (BL*) signal (or XBL*)
36	6	Halt due to the detect of CW direction limit (FL*) signal (or XFL*)
37	7	Halt due to the detect of alarm (ALM*) signal

3-2-5-3. Auxiliary input/output command

In the auxiliary input/output command, data is expressed in bits format. As for the input, 6 bits are used and 7 bit is “0”, therefore no ASCII conversion is made, and replied as it is.

As for the output, auxiliary output uses 5 bits for data, but in this case ASCII conversion is made and 2 bytes codes are replied.

3-2-5-4. Error counter reading command

This command is special command of the serial mode, and can read the value of internal error counter and the description of the last error. The error counter has 16 bits, and communication error code has 8 bits. Following the issuance of this command, the error counter is cleared. The detail of the replied data is shown in table 3-21 and Fig. 3-72.

Table 3-21. Reply to the error counter reading command

Sequence	Name	Descriptions
1	Control code	1010aaaa (aaaa is device address)
2, 3	Error counter (L)	ASCII converted 16 bits error counter value
4, 5	Error counter (H)	ASCII converted 16 bits error counter value
6	Last error	Last detected error code
7	Check sum	Control code, command, and data check sum (bit 7=0)

Last error means the status of serial communication device.

<Communication error code>

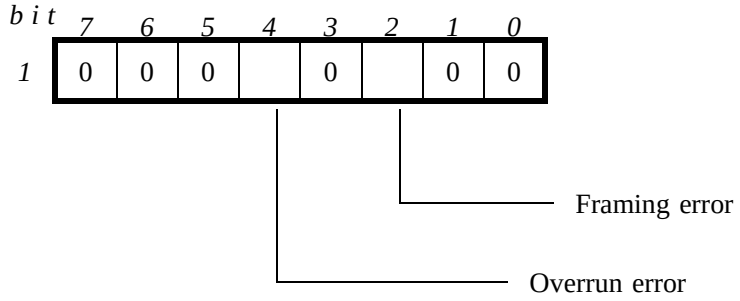


Fig. 3-72 Communication error code