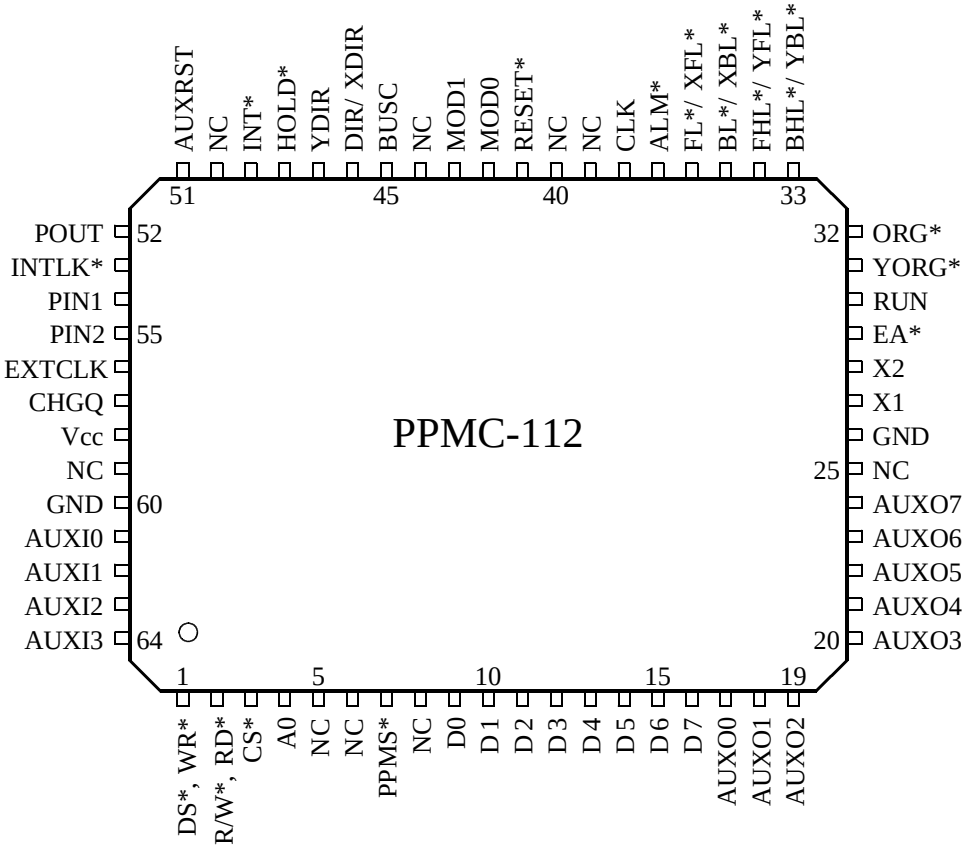
2. TERMINAL ASSIGNMENT

PPMC-112 is with a 64-pin QFP package, but the terminal signal assignment differs greatly in I/O areas in serial and parallel mode. Fig. 2-1 shows the terminal assignments in the parallel mode, which is the same as the former series. Fig. 2-2 shows serial mode terminal assignment. Table 2-1 and Table 2-2 are the terminal signal tables for each mode.

This chapter provides a detailed description of these signals.



(Top View)

Fig.2-1. PPMC-112 parallel mode terminal assignment

2. TERMINAL ASSIGNMENT

Table 2-1. Terminal Signal Table (Parallel interface)

Pin number	Signal	I/O	Description
1	DS/WRS	I	Data strobe, Write strobe
2	R/W, RDS	I	Read/Write, Read strobe
3	CS*	I	Chip select input
4	A0	I	Address 0
5	NC		
6	NC		
7	PPMS*	I	SYNC-101 recognition input (connected: "L")
8	NC	O	
9	D0	I/O	Host interface data bus bit 0
10	D1	I/O	Host interface data bus bit 1
11	D2	I/O	Host interface data bus bit 2
12	D3	I/O	Host interface data bus bit 3
13	D4	I/O	Host interface data bus bit 4
14	D5	I/O	Host interface data bus bit 5
15	D6	I/O	Host interface data bus bit 6
16	D7	I/O	Host interface data bus bit 7
17	AUXO0	O	Auxiliary output bit 0
18	AUXO1	O	Auxiliary output bit 1
19	AUXO2	O	Auxiliary output bit 2
20	AUXO3	O	Auxiliary output bit 3
21	AUXO4	O	Auxiliary output bit 4
22	AUXO5	O	Auxiliary output bit 5
23	AUXO6	O	Auxiliary output bit 6
24	AUXO7	O	Auxiliary output bit 7
25	NC	O	
26	GND		Connect to GND (Power 0 voltage)
27	X1	I	Crystal oscillator terminal 1 (16MHz)
28	X2	I	Crystal oscillator terminal 2 (16MHz)
29	EA*	I	Connect to 5V power
30	RUN	I	Output starting permission signal ("H": start)
31	YORG*	I	Y axis origin point setting (synchronous operation)
32	ORG*	I	Origin point (base point) input (In synchronous operation X axis origin point to be used)
33	BHL*	I	CCW direction high speed limit input
	YBL*	I	Y axis CCW direction limit input (synchronous)
34	FHL*	I	CW direction high speed limit input
	YFL*	I	Y axis CW direction limit input (synchronous)
35	BL*	I	CCW direction limit input
	XBL*	I	X axis CCW direction limit input (synchronous)
36	FL*	I	CW direction limit input
	XFL*	I	X axis CW direction limit input (synchronous)
37	ALM*	I	Alarm signal input
38	CLK	O	system clock (4MHz) output
39	NC	O	

Pin number	Signal	I/O	Description
40	NC	O	
41	RESET*	I	Reset input
42	MOD0	I	Connect to OV
43	MOD1	I	Connect to OV
44	NC	I	
45	BUSC	I	Host bus interface selection "H":DS+RW "L"*RD+WR
46	DIR	O	Rotation direction output ,"H":CCW"L":CW
	XDIR	O	X axis rotation direction signal output
47	YDIR	O	Y axis rotation direction signal output "H": CCW, "L": CW
48	HOLD*	O	Motor hold signal output, "L" 2mS after halt
49	INT*	O	Interrupt signal
50	NC	O	
51	AUXRST	O	SYNC-101 control signal
52	Pout	O	Pulse output (True logic)
53	INTLK*	O	Interlock output
54	Pin1	I	Pulse count input terminal 1, Connect to Pout
55	Pin2	I	Pulse count input terminal 2, Connect to Pout
56	EXTCLK	I	External clock input for the pulse generation.
57	CHGQ	I	Quadrant change input for the circular interpolation operation (Connect to 0v when not in use)
58	Vcc		5V power input
59	NC	I	
60	GND		0V power
61	AUXI0	I	Auxiliary input, bit 0
62	AUXI1	I	Auxiliary input, bit 1
63	AUXI2	I	Auxiliary input, bit 2
64	AUXI3	I	Auxiliary input, bit 3

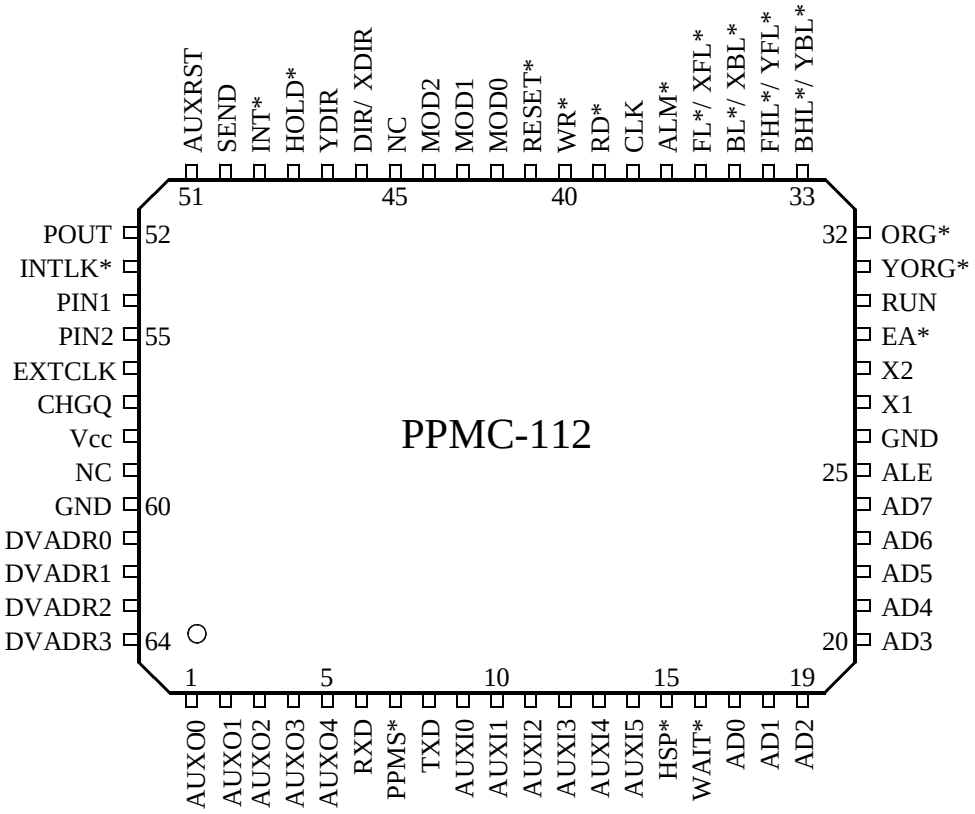
* in the table indicates negative logic.

O : Output

I : Input

NC : No connection

The input terminals which is not in use, and NC terminals in input mode, should be pulled up to VCC with 10kohm or pulled down to GND.



(Top View)

Fig.2-2. PPMC-112 serial mode terminal assignment

Table 2-2. Terminal - Signal Table (Serial interface)

Pin number	Signal	I/O	Description
1	AUXO0	O	Auxiliary output bit0
2	AUXO1	O	Auxiliary output bit1
3	AUXO2	O	Auxiliary output bit2
4	AUXO3	O	Auxiliary output bit 3
5	AUXO4	O	Auxiliary output bit4
6	RXD	I	Serial communication receive signal input
7	PPMS*	I	SYNC-101 recognition input (connected: "L")
8	TXD	OD	Serial communication transmit signal output
9	AUXI0	I	Auxiliary input bit 0
10	AUXI1	I	Auxiliary input bit 1
11	AUXI2	I	Auxiliary input bit 2
12	AUXI3	I	Auxiliary input bit 3
13	AUXI4	I	Auxiliary input bit 4
14	AUXI5	I	Auxiliary input bit 5
15	HSP*	I	High speed polling mode (High: "L")
16	WAIT*	I	When SYNC-101 is connected, connect to 0V
17	AD0	I/O	External bus (Address data) bit 0
18	AD1	I/O	External bus (Address data) bit 1
19	AD2	I/O	External bus (Address data) bit 2
20	AD3	I/O	External bus (Address data) bit 3
21	AD4	I/O	External bus (Address data) bit 4
22	AD5	I/O	External bus (Address data) bit 5
23	AD6	I/O	External bus (Address data) bit 6
24	AD7	I/O	External bus (Address data) bit 7
25	ALE	O	External bus (Address latch enable)
26	GND		Power 0 voltage
27	X1	I	Crystal oscillator terminal 1 (16MHz)
28	X2	I	Crystal oscillator terminal 2 (16MHz)
29	EA	I	Connect to 5V power
30	RUN	I	Output starting permission signal ("H": start)
31	YORG*	I	Y axis origin point setting (synchronous operation)
32	ORG	I	Origin point (base point) input (In synchronous operation, X axis origin point to be used)
33	BHL*	I	CCW direction high speed limit input
	YBL*		Y axis CCW direction limit input (synchronous)
34	FHL*	I	CW direction limit input
	YFL*		Y axis CCW direction limit input (synchronous)
35	BL*	I	CCW direction limit input
	XBL*		X axis CCW direction limit input (synchronous)
36	FL*	I	CW direction limit input
	XFL*		X axis CW direction limit input (synchronous)
37	ALM*	I	Alarm signal input
38	CLK	O	System clock (4MHz) output

Pin number	Signal	I/O	Description
39	RD*	O	External bus read signal (When SYNC-101 is connected)
40	WR*	O	External bus write signal (When SYNC-101 is connected)
41	RESET*	I	Reset input
42	MOD0	I	Serial communication baud rate control, bit 0
43	MOD1	I	Serial communication baud rate control, bit 1
44	MOD2	I	Serial communication mode (binary: "L")
45	NC	I	
46	DIR	O	Rotation direction output, "H": CCW "L": CW
	XDIR		X axis rotation direction signal output (When SYNC-101 is connected.)
47	YDIR	O	Y axis rotation direction signal output "H": CCW, "L": CW
48	HOLD*	O	Motor hold signal output, "L" 2mS after halt
49	INT*	O	Finish interrupt signal
50	SEND	O	Serial communication transmit gate control (While in transmission, "H")
51	AUXRST	O	SYNC-101 control signal
52	POUT	O	Pulse output (True logic)
53	INTLK*	O	Interlock output
54	PIN1	O	Pulse count input terminal 1(Connect to Pout)
55	PIN2	I	Pulse count input terminal 2(Connect to Pout)
56	EXTCLK	I	External clock input for the pulse generation
57	CHGQ	I	Quadrant change input for the circular interpolation operation (Connect to OV when not in use)
58	VCC		5V power
59	NC	I	
60	GND		0V power
61	DVADR0	I	Device address setting: bit 0
62	DVADR1	I	Device address setting: bit 1
63	DVADR2	I	Device address setting: bit 2
64	DVADR3	I	Device address setting: bit 3

* in the table indicates negative logic.

O : Output

OD : Open drain output

I : Input

NC : No connection

The input terminals which is not in use, and NC terminals in input mode, should be pulled up to VCC with 10kohm or pulled down to GND.

2-1. Signal description of system hardware

2-1-1. RESET* (Reset)

Signal used to reset PPMC-112 to initial state. This terminal should be connected to the RESET signal of a user's system. After the rise from a low level, the initialization and operation command from the host processor is put into operation. The RESET signal must be such that the "L" level is retained for at least 10 clock period after the oscillation of the internal oscillator has stabilized with the power supply voltage being within the operation range of PPMC-112.

2-1-2. X_1, X_2 (Crystal oscillator)

The X_1 and X_2 terminals input system clock to PPMC-112. Normally a 16MHz crystal oscillator is connected as shown in the diagram on the left in Fig. 2-3. 2-phase external clock can also be connected as shown in the diagram on the right in Fig. 2-3.

X_1 and X_2 can accept clock input frequencies of 1 to 16MHz, and the operating speed of PPMC-112 is in proportion to the clock. From this point forward, all times in this description are based on this reference clock speed. Unless mentioned otherwise, the times, speeds and data are based on the reference clock speed of 16MHz.

When two or more PPMC-112s are to be operated from a single system clock driver, design the circuit as shown in Fig. 2-4. Also, observe the NOTES on page 2-8.

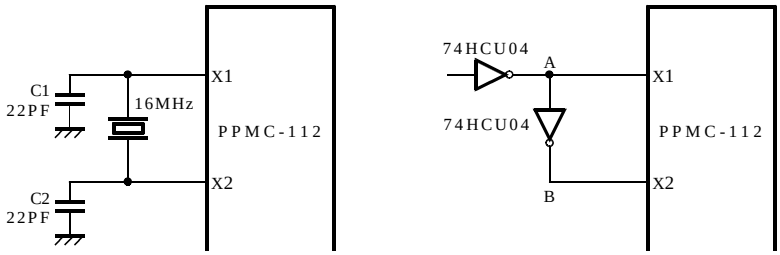


Fig. 2-3

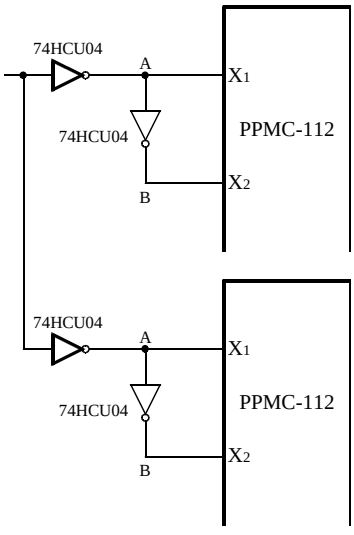


Fig. 2-4

NOTES:

(1). Crystal oscillator

The oscillation frequency of the crystal oscillator is determined by the load capacitance of the crystal oscillator and the external capacitance C1 and C2. However, the equivalent resistance of the crystal and external capacitance must be correct if oscillation is to be started and continued normally.

Table 2-3 below shows the recommended values.

Table 2-3. Oscillation Frequency and Equivalent Series Resistance

Frequency	Equivalent Series Resistance (Max.)	Frequency	Equivalent Series Resistance (Max.)
1MHz	600ohm	12MHz	35ohm
4MHz	100ohm	16MHz	35ohm
10MHz	35ohm		

(2). 2-phase external clock signal input system

When a 2-phase external clock signal driver as shown in Fig. 2-3 (diagram on right) and Fig. 2-4 is used, the following conditions must be satisfied by the circuit at points A and B:

Condition 1 : Duty ratio at A -50% to +50% (@ $V_{CC}/2$)

Condition 2 : CL at A and B 50pF (max.)

2-1-3. MOD0, MOD1 (Operational mode set input)

PPMC-112 will set its operational mode according to these two input signals. When both Mod0 and Mod1 are 0V, the parallel mode will be selected, otherwise serial mode will be selected.

2-1-4. PPMS* (SYNC-101 recognition input signal)

This is the signal to recognize SYNC-101, the interpolation operation assist processor. When SYNC-101 is connected, this input signal must be set to "L".

2-1-5. EXTCLK (External clock input)

For the base clock to generate pulse output, PPMC-112 can choose from internal clock speed of 2MHz, 500kHz, 125kHz. However, if this clock speed is not suitable for the system, the external clock can be fed through this terminal to cater various clock speed needs. The maximum clock speed allowed is 1MHz.

2-1-6. CLK (4MHz clock output)

This is 4MHz clock output available for the external use.

2-2. Host interface signals

The host interface signals are the signals that connect PPMC-112 to the bus of the host processor. They are either signals to access the registers of PPMC-112 or interrupt signals.

2-2-1. CS* (Chip select)

The chip select signal for PPMC-112 connects the signal decoding the upper bits of an address signal. PPMC-112 is accessible when CS* is low. (Refer to 3-1 "Host interface registers.")

2-2-2. A0 (Register select)

This is the signal to switch to a pertinent register when read or write is done with the register of PPMC-112 from the host processor. Normally it connects the LSB of an address signal. (Refer to 3-1 "Host interface registers.")

2-2-3. D7-D0 (Data bus)

These are bidirectional 8-bit buses for data exchange between host processor and PPMC-112.

2-2-4. BUSC (Slave bus interface select)

This signal selects the mode of interface between post processor and PPMC-112. This signal allows easy connection of either of the R/W* type CPU or the RD* and WR* separate type CPU. For the relationship between the BUSC signal and interface mode, refer to 2-2-5, 2-2-6 and Table 2-3.

Table 2-4. Relationship between BUSC Signal and Host Processor Bus I/F

BUSC signal	Host processor bus I/F	Control signal used	
H	R/W type	Data strobe signal (DS signal)	Read/ Write signal (R/W signal)
L	RD, WR separate type	Write strobe signal (WRS signal)	Read strobe signal (RDS signal)

2-2-5. DS, WRS (Data strobe, Write strobe)

This signal is used as the Data Strobe signal for the R/W* type CPU when the BUSC signal is high, and as the Write Strobe signal for the RD*, WR* separate type CPU when the BUSC signal is low. Refer to Table 2-4.

2-2-6. R/W, RDS (Read/Write, Read strobe)

This signal is used as the Read/Write signal for the R/W type CPU when the BUSC signal is high, and as the Read Strobe signal for the RD, WR separate type CPU when the BUSC signal is low. Refer to Table 2-4.

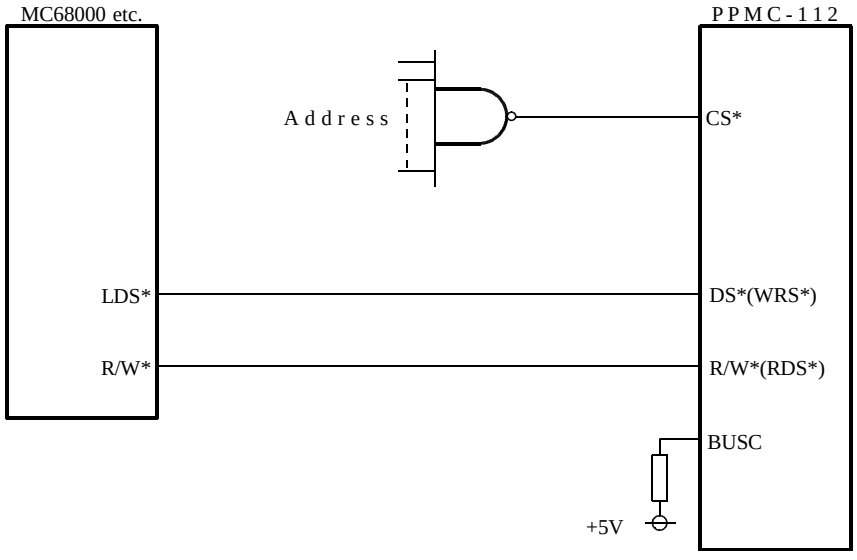


Fig.2-5. Sample Connection of R/W Type Signal

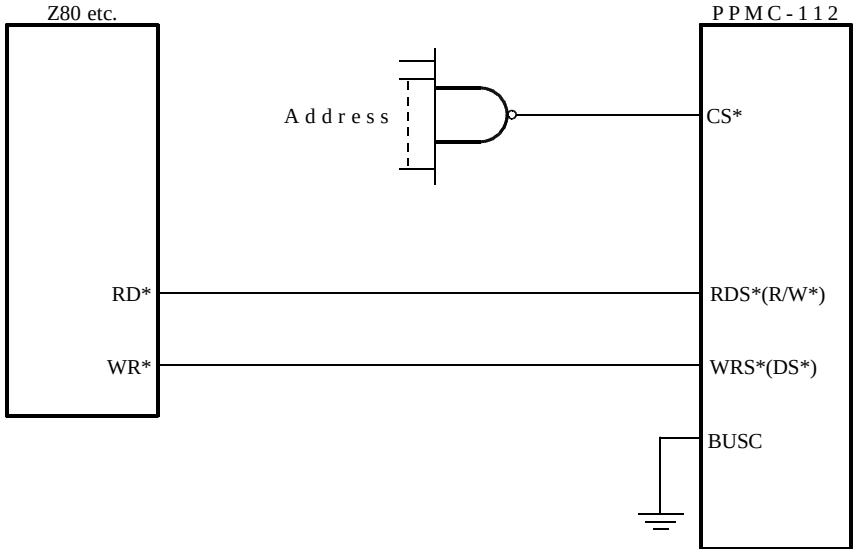


Fig.2-6. Sample Connection of RD, WR Separate Type Signal

2-2-7. INT* (Interrupt signal)

The Interrupt signal for the host processor is delivered in the following cases:

(1) When the command code received by PPMC-112 for the termination interrupt is authorized, and PPMC pulse output has halted.

(2) The finish interrupt control is authorized, and stop/deceleration command or limit input halt the processor.

(3) When the finish interrupt control operation is selected with the interlock command, and it reaches to the interlock releasing position.

(4) In the operation combined with SYNC-101, the pulse output halts.

(5) Alarm signal (ALM*) is detected while executing an operational command.

The INT* signal, which is normally high, goes low when any of above conditions (1) to (5) is met. The INT signal terminal is not an open collector. To connect a multiple interruption, therefore, provide an open collector buffer as shown in Fig. 2-7.

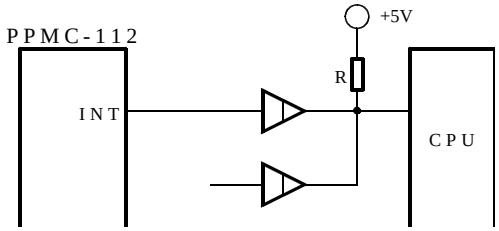


Fig.2-7. Sample Connection of PPMC-112 Interrupt Output Signal

When an error interrupt has occurred in the parallel mode, the INT* signal can be cleared by issuing a "Finish status read command". At this, the signal goes from low to high. Similarly, when an interlock release interrupt occurs, INT* signal can be cleared, but in this case, the finish status to be read will be "00h".

In serial mode, "busy check command" will cancel it. The first "busy check command" after halt will be replied with special frame termination status. Similarly, in case of interlock release, the special frame will be sent back as "00h" in binary mode, and "20h" in ASCII mode.

2-3. Serial communication interface signal(Serial mode)

These are the signals that will be needed to remotely control PPMC-112 via communication line.

2-3-1. TXD, RXD (Transmit, receive signal)

These signals are used in binary or ASCII mode communication: transmit signal output TXD, and receive signal input RXD. TXD is an open drain output, and always has to be pulled-up.

2-3-2. SEND (Send gate control signal output)

This is the signal to control transmission output power for the multi-drop communication. PPMC-112 send TXD while this signal is "H". In the case of MULTI-DROP communication, PPMC-112 opens the send gate via this signal to communicate with the master processor. While the master processor is communicating with other devices, the send gate will be closed to avoid collision of transmitted signals.

2-3-3. MOD0, MOD1, MOD2 (Communication mode / baud rate setting input)

When both MOD0, MOD1 are 0V, parallel mode will be selected, otherwise these will be used to set the baud rate. In serial mode, MOD2 will determine the communication mode. When MOD2 is "H", ASCII communication mode is selected, and when it is "L", binary mode will be selected. In binary mode, the communication at the speed of maximum 125kbpS is available. In ASCII mode, maximum speed is 83.33kbpS. In ASCII mode, any speed except 19.2kbpS is not a standard setting speed, however common PC hardware can handle various speed in ASCII mode communication. Therefore to cater this needs, we can offer driver/software for high speed communication.

In binary communication mode, communication hardware that matches PPMC-112 specifications will be needed. We can offer host interface chip MWSC-101 for this purpose.

Table 2-5. Communication protocol & baud rate setting

MOD2	MOD1	MOD0	Operation mode / Communication mode and baud rate
x	0	0	Parallel mode
0	0	1	Binary mode 31.25kbpS
0	1	0	Binary mode 62.5kbpS
0	1	1	Binary mode 125kbpS
1	0	1	ASCII mode 19.2kbpS
1	1	0	ASCII mode 41.67kbpS
1	1	1	ASCII mode 83.33kbpS

When you plan the system, please note pin 1 to 4 work as input terminal in parallel mode, and output terminal in serial mode.

2-3-4. DVADR0 to DVADR3 (Device address setting input)

These 4 input signals will determine the device address in serial communication. PPMC-112 can have 16 different device addresses on a single communication line, thus up to 16 PPMC-112 can be controlled via the same one communication line.

2-3-5. HSP* (High speed polling mode assignment input signal)

In PPMC-112 system, a host processor always starts communication for the multi-drop communication. It is necessary to do so in order to avoid signal collision on communication line. Therefore, a host processor always

needs to execute polling to check if PPMC-112 finished an operation command. This polling speed will determine the system's overall response time, therefore the operation requires high speed.

In PPMC-112 system, each frame have check sum at the end of communication to prevent communication error. Busy check frame consists of busy check control and check sum. When the high quality line is available, which can be considered as error free, it is possible to remarkable reduce the polling time by skipping check sum verification and replying the status codes directly.

When HSP signal is "L" , only in case of busy check, PPMC-112 does not receive any check sum, but send back the status code.

Polling speed can be reduced to around 3mS in the system with 16 PPMC-112 attached by operating host computer in this way when communicating at 125kbpS speed,.

2-4. Motor control signals

The motor control signals are connected to a motor driver or like device.

2-4-1. DIR (Rotation direction signal)

The DIR signal, which specifies the direction of rotation, goes low when delivering a pulse for CW rotation and goes high when delivering a pulse for CCW rotation. This signal is used together with the POUT signal of 2-4-2.

2-4-2. Pout (Pulse train output signal)

This is the pulse train signal delivered by PPMC-112. The true logic is used and the pulse width is 4 base clock cycle, which is 2 microsecond at 2MHz speed. This signal is used jointly with the DIR signal of section 2-4-1. Also, be sure to connect this signal to the PIN1 and PIN2 signals of section 2-4-3.

2-4-3. PIN1, PIN2 (Internal pulse counter input)

These terminals are input terminals for the pulse counter inside PPMC-112. These signals are important for the operation of PPMC-112. Therefore be sure to connect them to the Pout signal of 2-4-2.

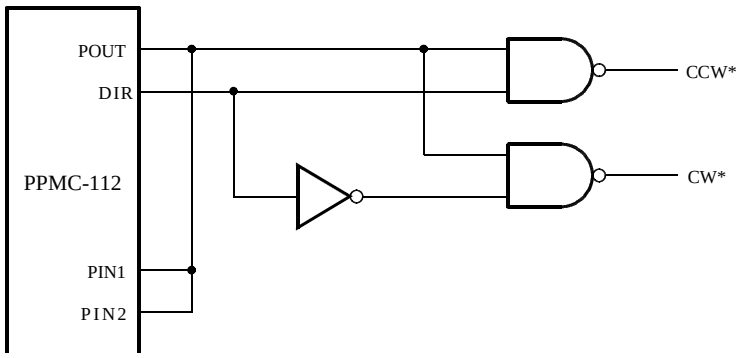


Fig.2-8. Sample Connection of DIR, POUT, PIN1 and PIN2 Signals

2-4-4. HOLD* (Motor hold signal)

This signal indicates that the motor is stopped. The HOLD signal goes low about 2mS after the stop of pulse output. When PPMC-112 receives the next operation command, the HOLD signal goes high. It is used for the lowering of supply voltage at motor stop or external monitoring of it.

2-4-5. RUN (Pulse output start signal)

This signal is checked before a pulse output with an operation command given by the host processor to PPMC-112. If the signal is high, pulse output will start. If it is low, there will be a wait until the signal goes high. During this time, PPMC-112 accepts no other commands, but in parallel mode, the RUN flag will be set at status register.

For instance, combined with interlock signal, this signal is used to adjust the starting timing of multiple PPMC-112s. It can also be used to start operation of two or more PPMC-112s simultaneously by using auxiliary output signal. When you do not use the function of the RUN signal, it must be pull up the voltage to +5V.

2-4-6. INTLK* (Interlock output signal)

When PPMC-112 starts by interlock releasing position setting command, and reaches to the designated position, this signal will turn to be "H". As explained in the former section, this signal can be used to start up, or to control the timing of other devices by connecting to the RUN signal input terminal of other PPMC-112.

2-5. Limit and alarm signals

These are a group of input signals from limits and motor driver. These are all negative logic inputs.

The limit signals and alarm signals as explained below must be kept low for 200 microsecond or longer if they are to be detected by PPMC-112. Also, when a command in Table 2-6 is executed during a pulse output, there is a period during which arrival of the limit signal or alarm signal can not be detected. That is, even if the limit signal or alarm signal is kept low for 200 microsecond or longer, it may not be detected during that time. Therefore, caution must be exercised when executing these commands. When arrival of a limit signal or alarm signal can not be detected during pulse output, the specified pulse output is continued. For details, refer to the section on each command.

Table 2-6. Non detecting Duration of Limit and Alarm Signals

Command	Non-detecting Duration	Maximum time (microsecond)
Instantaneous Speed Change	From receipt of command to end of speed change	300
Acceleration/Deceleration Speed Change	From receipt of command to start of speed change	300
Finish Status Read	From receipt of command to setting of finish status code in output buffer inside PPMC-112	50
Command Error Code Read	From receipt of command to setting of command error code in output buffer inside PPMC-112	50
Control Input Signal Status Read	From receipt of command to setting of control input signal status in output buffer inside PPMC-112	50
Auxiliary Input Signal Status Read	From receipt of command to setting of auxiliary input signal status in output buffer inside PPMC-112	50
Auxiliary Output	From receipt of command to output of auxiliary output signal	50
Decelerating Stop	From receipt of command to start of deceleration	50

2-5-1. ORG*, XORG*, YORG* (Origin input signal)

PPMC-112 checks this signal only at the Constant Speed Origin Search (constant speed movement to origin) command. Upon detection of this signal, PPMC-112 stops pulse output immediately. Normally this signal provides the origin for all positioning controls. When SYNC-101 is connected, ORG* will work as XORG*(origin point of X axis), and YORG* as origin point of Y axis.

2-5-2. FL*, BL*, FHL*, BHL* (Limit input signals)

FL* is the limit to be set at the operation limit point in CW rotation, and BL* is that in CCW rotation. For any operation command, PPMC-112 will stop the operation when it detects this limit in any of the operational directions. If an operation command in the same direction is fed after this, PPMC-112 will not output the pulse but will respond with Error No.3.

FHL* is the high speed limit to be set in CW rotation, and BHL* is that in CCW rotation. PPMC-112 will cause a decelerating stop when it detects this limit during an acceleration or high-speed operation. In this case, if any command which requests alter speed is issued during the deceleration, PPMC-112 will not accept it but will respond with Error No.14.

When connected to SYNC-101, FL* and BL* work as X axis FL and BL*, and FHL* and BHL* will work as Y axis FL* and BL*.

Fig.2-9 shows the physical/positional relationship of the limit signals explained above.

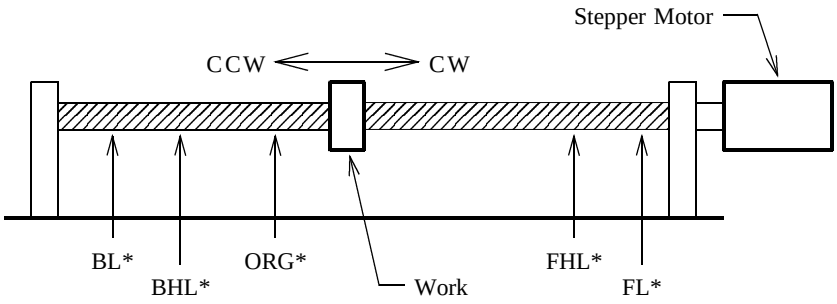


Fig.2-9. Positional Relationship of Limit Switches

* The FL* and BL* limit switches are set at the respective operation limit points of work.
* The FHL* and BHL* limit switches are set to the acceleration/deceleration pulse count or more inside from the FL* and BL* positions, respectively.
* The ORG* limit switch is set at the origin for positioning control.

As the High Speed limit signal, the FHL* signal is effective at CW pulse output, and the BHL* signal at CCW pulse output. And, as shown in Table 2-7, the effectiveness of the High Speed Limit signal varies depending on the following three (3) conditions: the kind of operation command, the setting of high speed limit effective speed pulse rate, and the operational state at detection of the High Speed limit signal.

Table 2-7. Effectiveness of the High speed limit

Operational command	Operational state at the detection of high speed limit			
	Starting up	Accelerating	High speed limit effective speed or over	Decelerating
Constant speed operation	Invalid	x	Valid	x
Acceleration/ Deceleration operation	Valid	Valid	Valid	Invalid
Continuous constant operation	Invalid	x	Valid	x
Constant speed origin search	Invalid	x	Valid	x
Continuous high speed operation	Valid	Valid	Valid	Invalid
After speed alteration command	x	Valid	Valid	Invalid
Single step	Invalid	x	x	x

Valid : Signal decelerates and halts operation. (When detected at start up, the operation does not start, but error code #3 will be replied.)
Invalid : Signal is ignored
x : Not applicable

If a high speed limit effective speed pulse rate is not set with the high speed limit effective speed setting command(default state) after the PPMC-112 is reset, the value of pulse rate at high speed established at the time of initialization shall be used as the high speed limit effective speed pulse rate.

2-5-3. ALM* (Alarm input signal)

This terminal is connected to the alarm output of the motor driver. When PPMC-111 receives this signal during its operation, it will stop the pulse output and send an Interrupt (INT*) signal to the host processor.

2-6. SYNC-101 control I/O signal

PPMC-112 can perform synchronous linear/circular interpolation operation by combining the interpolation processor, SYNC-101. There are two ways to control SYNC-101. In parallel mode, SYNC-101 and PPMC-112 can be connected directly to the same host bus, in which system two processors will be connected by 3 signal lines. These signal lines will be explained in the following section 2-6-1 to 2-6-3.

In serial mode, PPMC-112 will I/O the external bus signals to control SYNC-101's bus lines. These signal lines will be explained in section 2-6-4 and thereafter.

2-6-1. POUT-MRPLS (Master Pulse)

SYNC-101 will receive PPMC-112's POUT signal as MRPLS (Master pulse). SYNC-101 will synchronize to this pulse input and distribute the pulse to X and Y axis.

2-6-2. CHGQ-CHGQ (Quadrant change signal)

In a circular interpolation, the directions of X and Y axis change at each boundary of quadrants, SYNC-101 send CHGQ signal following the detection of the quadrant boundaries. PPMC-112 receive this CHGQ output as the CHGQ input, and control XDIR, YDIR signals.

2-6-3. AUXRST-AUXRST (SYNC-101 auxiliary reset signal)

This is the signal to control the internal logic of SYNC-101. PPMC-112 sends this signal, and SYNC-101 receives it.

2-6-4. AD0 to AD7, ALE, RD*, WR*, WAIT* (SYNC-101 control I/O bus)

This signal will be used in a serial communication mode.

AD0 to AD7 are the 8-bit multiplex I/O bus to control SYNC-101. ALE (Address latch enable) will separate address and data signals and connect data to D0 to D7 of SYNC-101. RD* and WR* are connected between PPMC-112 and SYNC-101, thus controlling read and write operation. A0 of address signals which are separated from the bus will be connected to SYNC-101's A0 input, and WAIT* input will have 0V connection. These chips connection example is shown in fig 2-10.

Through this bus lines, PPMC-112 feeds the SYNC-101 control command to the SYNC-101 from the host processor, thus enables the interpolation operation.

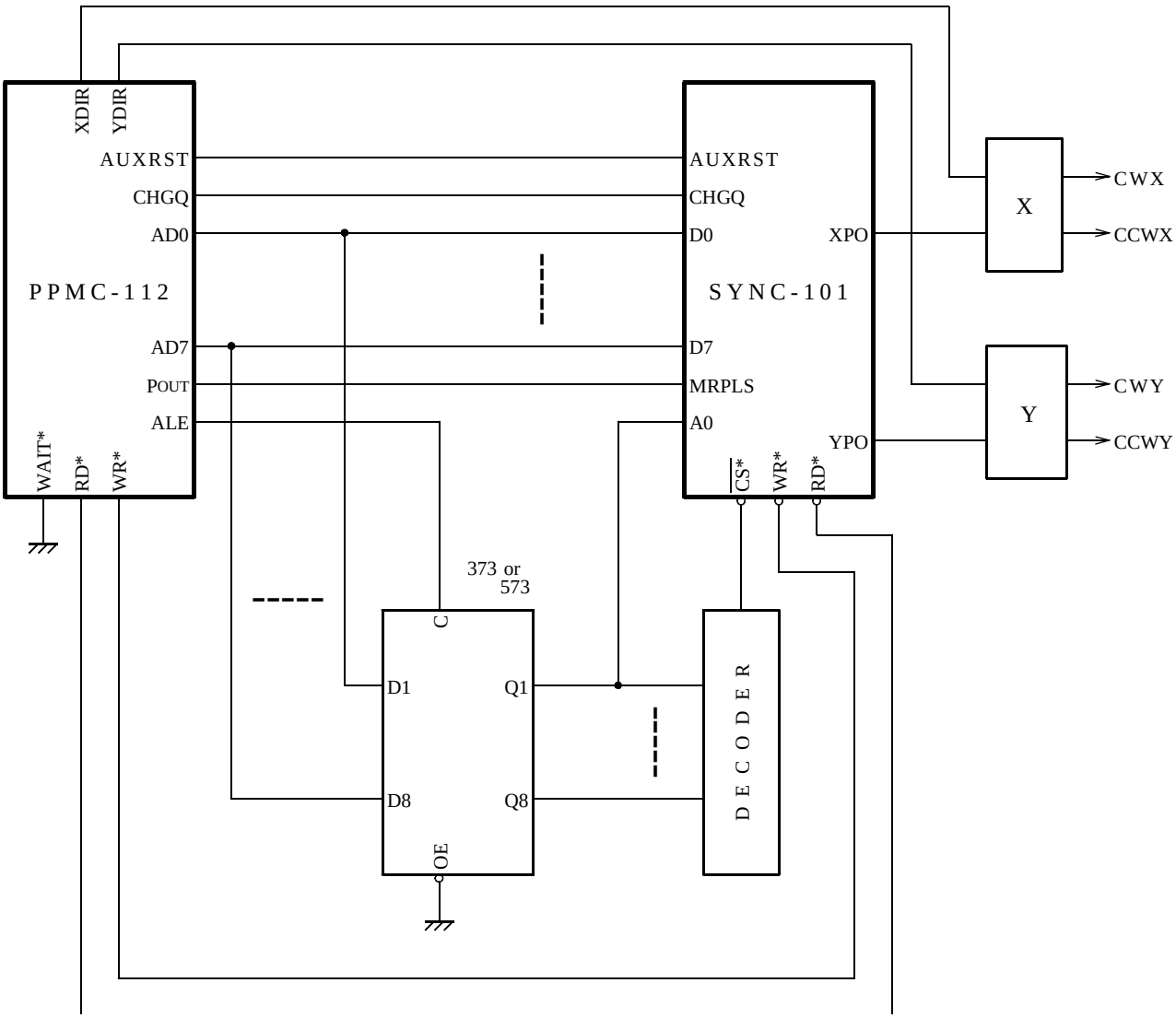


Fig.2-10. Sample combination of PPMC-112 and SYNC-101

2-7. Auxiliary input/output signals

The Auxiliary input/output signals use the general purpose 8-bit I/O ports, which have no direct relation with stepper motor control functions.

2-7-1. AUXI0 - AUXI3 (Parallel) or AUXI0 - AUXI5 (Serial)

AUXI0 to AUXI3 are the 4-bit input ports (6-bit in serial mode) provided by PPMC-112, which serve as auxiliary input ports for the system. Bit with no signal, such as bit 4 to 7 in parallel mode, or bit 6 and 7 in serial mode, data "0" will be assigned. It takes about 20 microsecond to read the state of the input ports.

2-7-2. AUXO0 - AUXO7 (Parallel) or AUXO0 - AUXO4 (Serial)

AUXO0 to AUXO7 are the 8-bit (5-bit in serial mode) output ports provided by PPMC-112, which serve as auxiliary output ports for the system. There will be no meaning for the output to the bit with no port assignment (bit 5 to7 in serial mode). After sending the command, it takes about 20 microsecond for the state of the output ports to change. These output ports immediately turn to "H" after reset, but goes back to "L" following the internal initialization.