

4. RATINGS

PPMC-111C/CFP

4. RATINGS

4 - 1 Absolute maximum ratings

The absolute ratings of PPMC-111 are as specified in Table 4-1.

Table 4-1 (Table of Absolute Maximum Ratings)

I t e m	S y m b o l	R a t i n g	U n i t
Supply voltage	Vcc	-0.5 to +7	V
Input voltage	Vin	-0.5 to +Vcc + 0.5	V
Power consumption (Ta=85 °C)	Pd	500	mW
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-65 to +150	°C
Soldering temperature (10s)	Tsolder	260	°C

Use of PPMC-111 beyond the absolute maximum ratings may result in deterioration and permanent damage.

4 - 2 DC Characteristics

The DC characteristics of PPMC-111 are as shown in Table 4-2.

Table 4-2 (Table of DC Characteristics)

I t e m		S y m b o l	M i n .	M a x .	U n i t	C o n d i t i o n
Low level input voltage	RESET		-0.3	0.25Vcc	V	
	X1		-0.3	0.2Vcc		
	Other		-0.3	0.3Vcc		
High level output voltage	RESET		0.75Vcc	Vcc + 0.3	V	IOL = 1.6mA
	X1		0.8Vcc	Vcc + 0.3		
	Other		0.7Vcc	Vcc + 0.3		
Low level output voltage	All output terminals	VOL		0.45	V	
High level output voltage	AUX00 - AUX07	VCH	2.4		V	IOH = -400microA
	Other		0.75Vcc			IOH = -100microA
Input current		Idr	-1.0	-3.5	mA	Vext = 1.5V Rext = 1.1kohm
Input leakage current		ILI	0.02 (Typ)	±5	microA	0.0 ≤ Vin ≤ Vcc
Output leakage current		ILO	0.05 (Typ)	±10	microA	0.0 ≤ Vin ≤ Vcc -0.2
Current consumption		ICC	35 (Typ)	50	mA	f = 16MHz
Input capacity	All input pins	CIN		10	PF	f = 1MHz

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PPMC-111C/CFP

4 - 3 AC Characteristics

4 - 3 - 1 RD and WR separate bus mode

(1) Register read operation

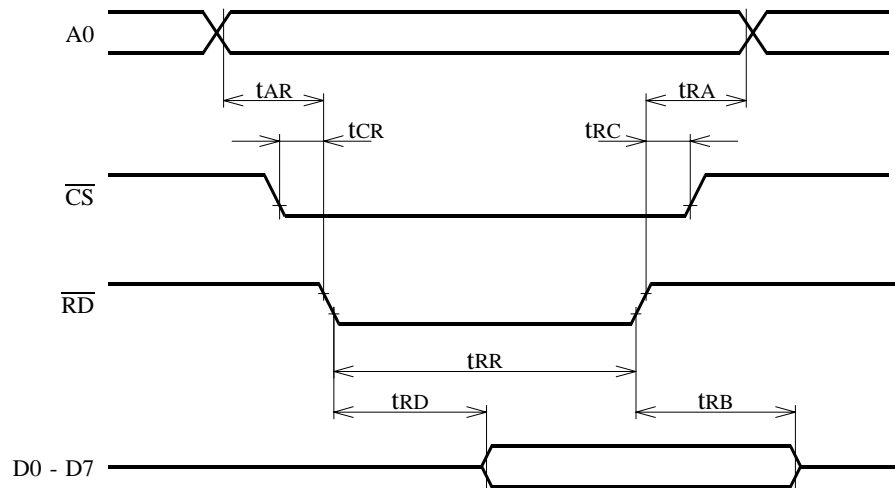


Fig. 4-1 (RD and WR Separate Bus Mode Register Read Timing)

Table 4-3 (RD and WR Separate Bus Mode Register Read Parameters)

I t e m	Symbol	Min	Max	Unit
A0 set time to $\overline{\text{RD}}$	t_{AR}	20		ns
A0 hold time after $\overline{\text{RD}}$	t_{RA}	5		ns
$\overline{\text{CS}}$ set time to $\overline{\text{RD}}$	t_{CR}	0		ns
$\overline{\text{CS}}$ hold time after $\overline{\text{RD}}$	t_{RC}	0		ns
$\overline{\text{RD}}$ pulse width	t_{RR}	120		ns
$\overline{\text{RD}}$ to data output delay	t_{RD}		100	ns
Data hold time after $\overline{\text{RD}}$	t_{RB}	10	90	ns

(VCC = +5V \pm 10%, Ta = -20 to 70°C)

(2) Register write operation

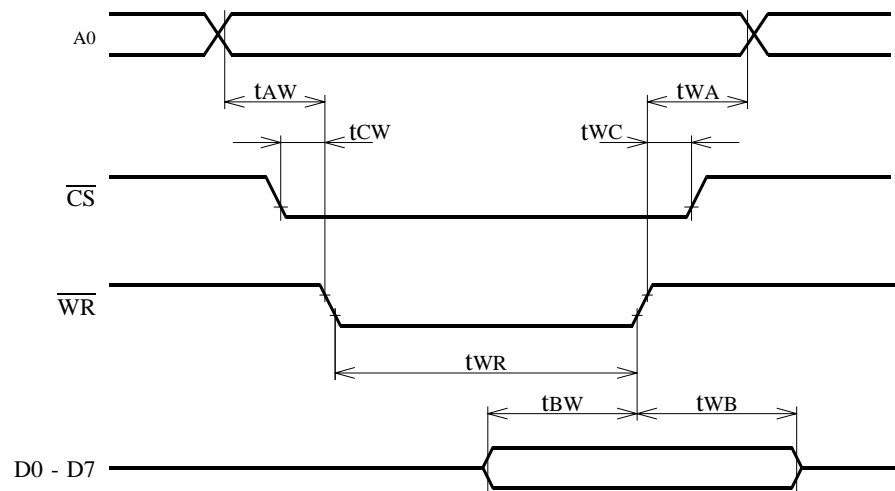


Fig. 4-2 (RD and WR Separate Bus Mode Register Write Timing)

Table 4-4 (RD and WR Separate Bus Mode Register Write Parameters)

I t e m	Symbol	Min	Max	Unit
A0 set time to \overline{WR}	t_{AW}	20		ns
A0 hold time after \overline{WR}	t_{WA}	5		ns
\overline{CS} set time to \overline{WR}	t_{CW}	0		ns
\overline{CS} hold time after \overline{WR}	t_{WC}	0		ns
\overline{WR} pulse width	t_{WR}	120		ns
Data setup to \overline{WR}	t_{BW}	80		ns
Data hold time after \overline{WR}	t_{WB}	10		ns

($V_{CC} = +5V \pm 10\%$, $T_a = -20$ to $70^{\circ}C$)

4. RATINGS

PPMC-111C/CFP

4 - 3 - 2 \overline{DS} and R/ \overline{W} bus mode

(1) Register read operation

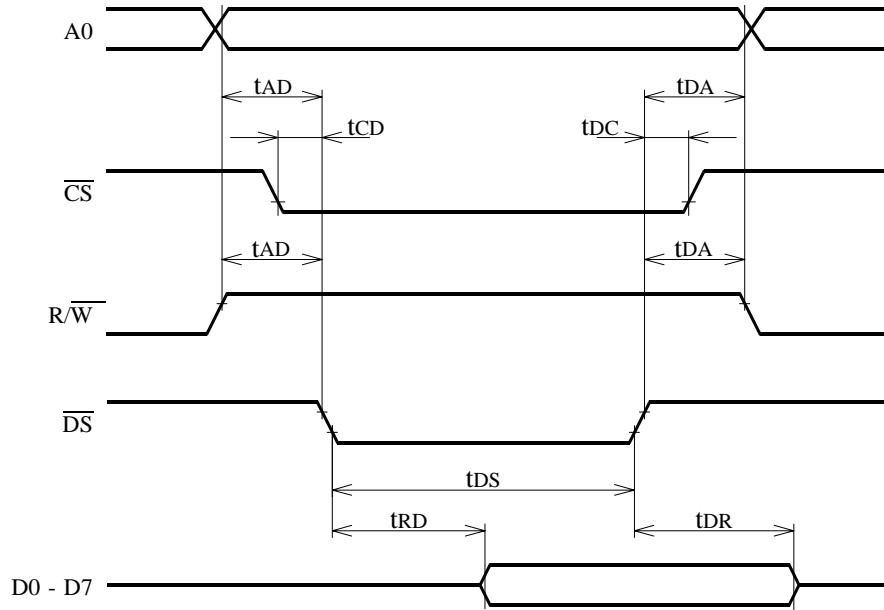


Fig. 4-3 (\overline{DS} and R/ \overline{W} Bus Mode Register Read Timing)

Table 4-5 (\overline{DS} and R/ \overline{W} Bus Mode Register Read Parameters)

I t e m	S y m b o l	M i n	M a x	U n i t
A0, R/ \overline{W} set time to \overline{DS}	t_{AD}	20		ns
A0, R/ \overline{W} hold time after \overline{DS}	t_{DA}	5		ns
\overline{CS} set time to \overline{DS}	t_{CD}	0		ns
\overline{CS} hold time after \overline{DS}	t_{DC}	0		ns
\overline{DS} pulse width	t_{DS}	120		ns
\overline{DS} to data output delay	t_{RD}		100	ns
Data hold time after \overline{DS}	t_{DR}	10	90	ns

($V_{CC} = +5V \pm 10\%$, $T_a = -20$ to $70^\circ C$)

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(2) Register write operation

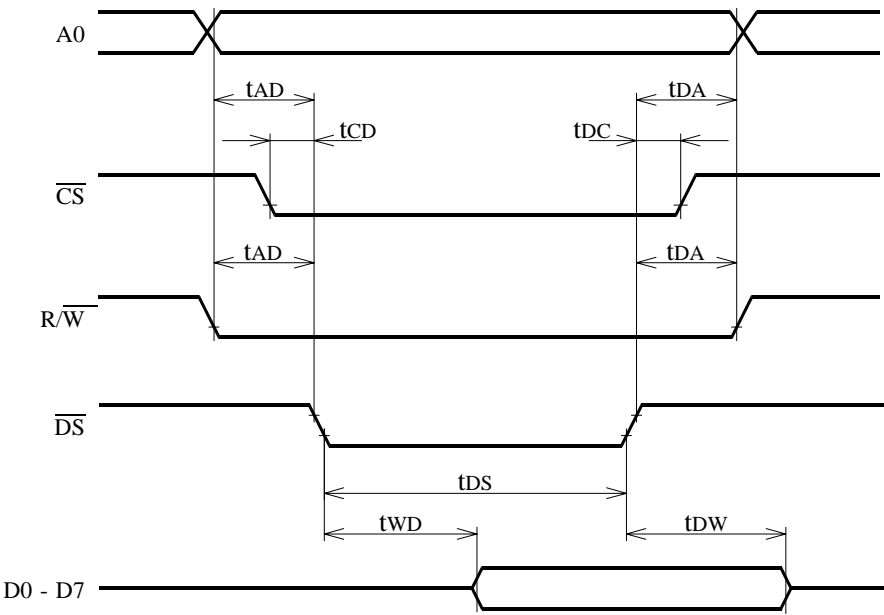


Fig. 4-4 (\overline{DS} , $\overline{R/W}$ Bus Mode Register Write Timing)

Table 4-6 (\overline{DS} , $\overline{R/W}$ Bus Mode Register Write Parameters)

Item	Symbol	Min	Max	Unit
A0, $\overline{R/W}$ set time to \overline{DS}	t_{AD}	20		ns
A0, $\overline{R/W}$ hold time after \overline{DS}	t_{DA}	5		ns
\overline{CS} set time to \overline{DS}	t_{CD}	0		ns
\overline{CS} hold time after \overline{DS}	t_{DC}	0		ns
\overline{DS} pulse width	t_{DS}	120		ns
\overline{DS} to data output delay	t_{WD}	80		ns
Data hold time after \overline{DS}	t_{DW}	10		ns

($V_{CC}=+5V \pm 10\%$, $T_a = -20$ to $70^{\circ}C$)

4. RATINGS

PPMC-111C/CFP

4 - 3 - 3 Alarm and limit signal input timing

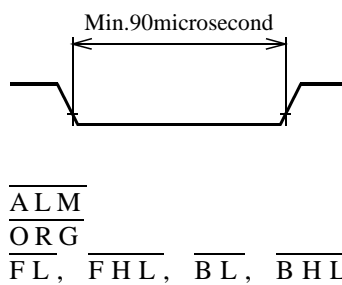


Fig. 4-5 (Alarm and Limit Signal Input Timing)

4. RATINGS

PPMC-111C/CFP

4 - 4 Outline drawings

4 - 4 - 1 Outline drawing of PPMC-111CFP

[Unit : mm]

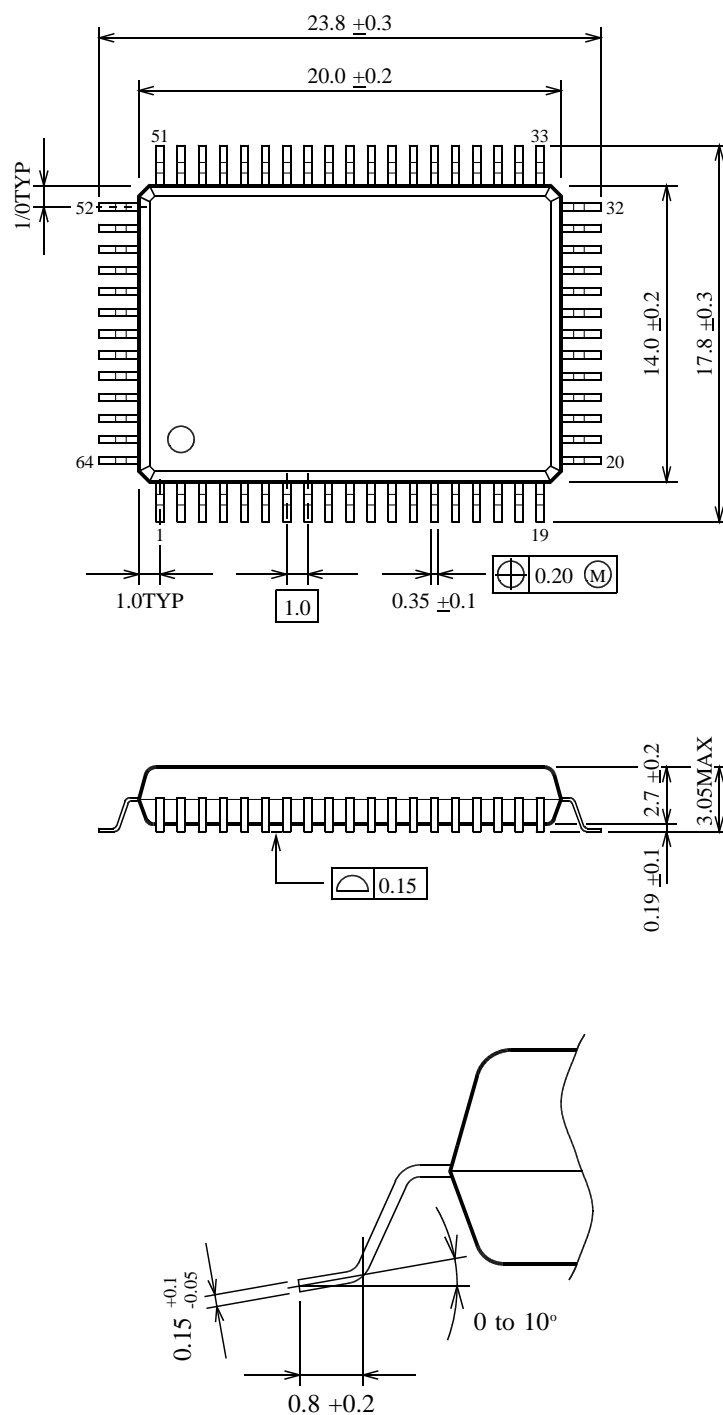


Fig. 4-6 (Outline Drawing of PPMC-111CFP)

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PPMC-111C/CFP

4 - 4 - 2 Outline drawing of PPMC-111C

[Unit : mm]

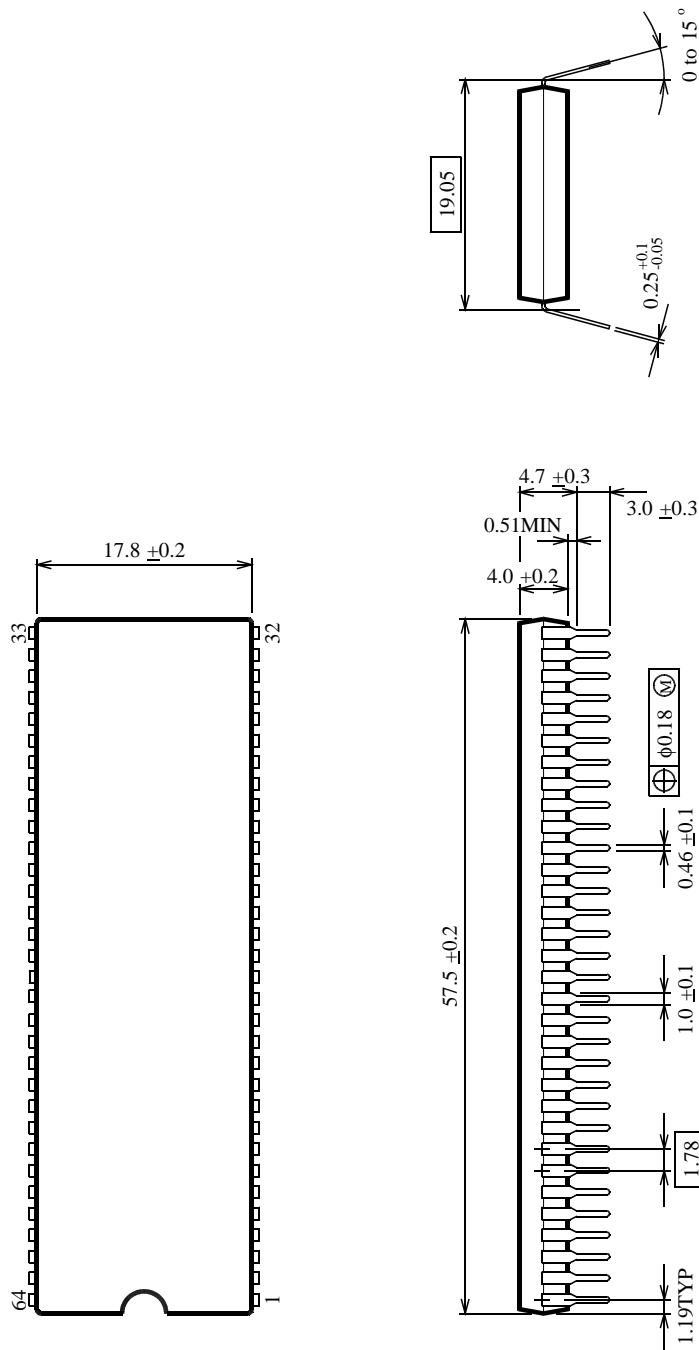


Fig. 4-7 (Outline Drawing of PPMC-111C)