3 . CONTROL COMMANDS OF PPMC-111

The **PPMC-111** operates according to the command codes and data transmitted from the host processor. There are, in general, four (4) groups of commands as listed below:

(1) Initialization commands

This command is used to set the profile of an acceleration/deceleration curve and the range of operation speed. **PPMC-111** must be provided with this command either following the supply of power or resetting prior to any other operations.

(2) Operation commands

These commands are used to operate the stepper motor. There are ten (10) commands, including two (2) stop commands. Some of the commands operate with command codes alone, while other commands require some bytes of data.

(3) Internal register read commands

PPMC-111 has five (5) internal register read commands capable of reading various conditions, including the cause of operation termination, command error code, data on current motor position auxiliary input data and limit switch activation.

(4) Auxiliary commands

There are three (3) auxiliary commands: motor position setting command, auxiliary output command and high-speed limit effective speed setting command.

3 - 1 Host interface registers

PPMC-111 has four (4) registers listed below. These registers are used for the input/output of commands and/or data. **Table 3-1** shows their access conditions.

Table 3-1 (Host interface register)

Name of Register	CS	A_0	RD	WR	Read/Write
Disable	**H**	x	x	x	Disable
Data Register	**L**	**L**	**L**	**H**	Read
Status Register	**L**	**H**	**L**	**H**	Read
Data Register	**L**	**L**	**H**	**L**	Write
Command Register	**L**	**H**	**H**	**L**	Write

3 - 1 - 1 Status register

Status register is a read-only register which indicates the internal conditions of **PPMC-111**. These internal conditions can be read at any time. **Fig. 3-1** shows the bit configuration.

< Status register >

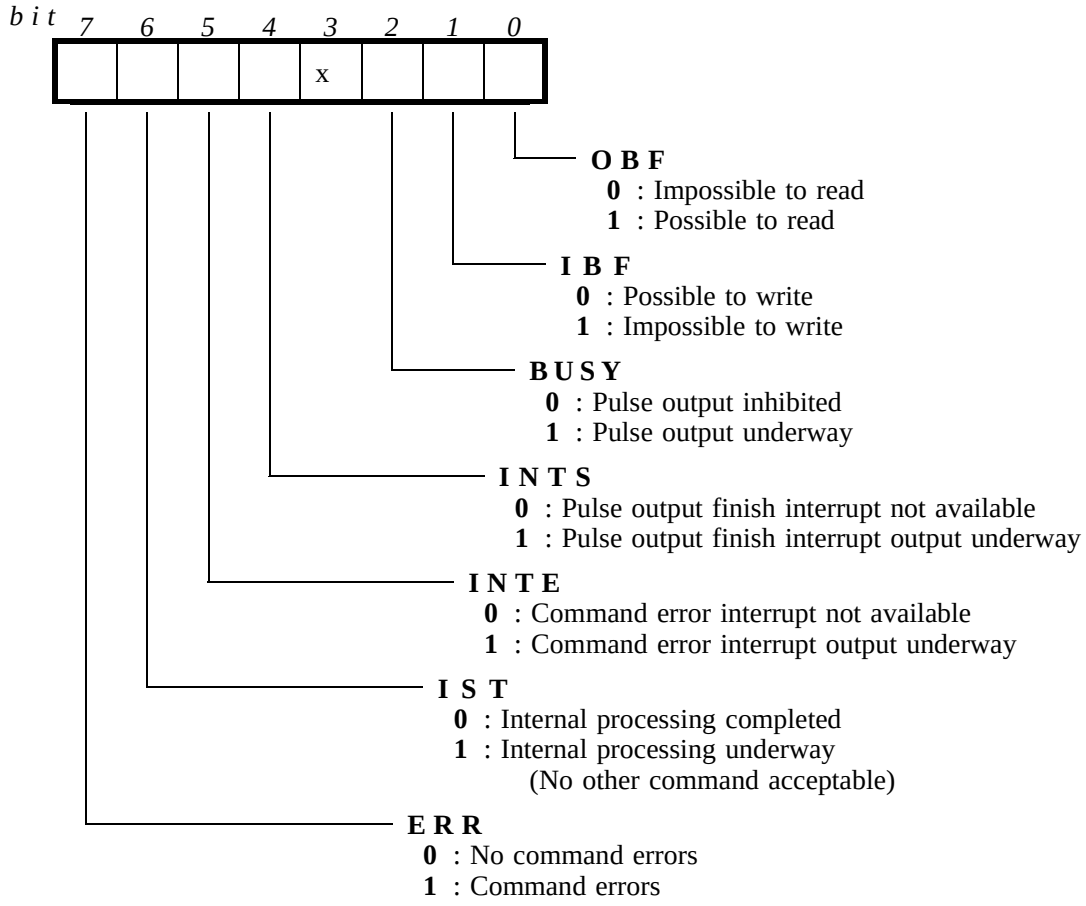


Fig. 3-1 (Status register bit configuration)

(1) OBF : Output Buffer Full Flag

This bit enables checking whether it is ready to read data from **PPMC-111**. Data must be read after making certain that OBF indicates "1." Data read is void if OBF shows "0."

(2) IBF : Input Buffer Full Flag

This bit enables checking whether it is ready to write commands or data to **PPMC-111**. Data cannot be written if the IBF bit is "1." Commands and data must be written after making certain that IBF indicates "0." Entry of commands or data when the IBF bit shows "1" deletes previously written commands and data.

(3) BUSY : Motor Busy

The BUSY bit indicates "1" when **PPMC-111** is engaged in pulse output (i.e., when the motor is rotating). No command other than the stop command, speed change command, status read command and auxiliary output command can be accepted when the BUSY bit indicates "1." This BUSY bit, as well as the IBF bit, must be checked when writing a command.

(4) INTS : INT by Stop

This bit indicates the output of interrupt signal following the termination of pulse output on **PPMC-111**.
If the INTS bit indicates "1," the interrupt ($\overline{\text{INT}}$) signal output is underway following the termination of pulse output. The INTS bit indicates "0" upon issuing the finish status read command (Section **3-4-1**).

(5) INTE : INT by Error

This bit indicates the output of interrupt signal by command error. If the INTE bit reads "1," the interrupt signal is being output by command error. The INTE bit indicates "0" upon issuing the command error code read command (Section **3-4-2**).

(6) IST : Internal Status Flag

This bit indicates the progress of processing of command. The IST bit shows "1" if any command code is written in **PPMC-111**. The bit changes to "0" when data has been written according to the command code and the internal processing has been completed.
It is necessary to make sure that the IST bit indicates "0" before issuing the first command code to **PPMC-111**.
In issuing a command which requires the setting of data, such as the pulse rate and operation pulse number (number of operating pulses), command error (Error No.7) occurs if, following the entry of that command code, another command code is written without writing the necessary data.

(7) ERR : Error Flag

This bit enables checking for any error in the command codes or data furnished by the host processor.
Checking this bit after the internal processing (IST bit of status register = 0) is completed following the issuing of each command enables the detection of an error in the command codes or data issued.
"0"indicates no errors. "1" shows the existence of an error. This bit shows "0" if the command given next is correct. More information on the error can be obtained through the identification of the error number by issuing the command error code read command (Section **3-4-2**).

Table 3-2 (Command error codes)

Error Code		Descriptions of Error
Decimal	Hexadecimal	
0	00	No errors
1	01	Received command not defined.
2	02	No initialization command provided.
3	03	Not operable due to limit signal or alarm signal.
4	04	Not operable as operation pulse number "0" is designated.
5	05	Stop command received while at stop.
6	06	Received data not preceded by command.
7	07	Received command while waiting for data.
8	08	Not operable as origin search command is received while origin signal is already fed.
9	09	Received a command which is unprocessible in BUSY status.
10	0A	Abnormal pulse rate of initialization command (>7FFFh or <000Fh).
11	0B	Excessively small acceleration/deceleration pulse number at the time of initialization.
12	0C	Abnormal pulse rate at the time of initialization (RH<RL).
13	0D	Pulse rate designated at issue of operation command or speed change command is outside the range of pulse rate designated at the time of initialization (RH<RL).
14	0E	Received speed change command while decelerating due to detection of high speed limit or receipt of decelerating stop command.
15	0F	Received decelerating stop command while decelerating due to detection of high speed limit or receipt of decelerating stop command.
16	10	Received speed change command while at stop.
17	11	Abnormal acceleration/deceleration step number at the time of initialization (<2 or >96).
18	12	Abnormal acceleration/deceleration step pulse rate at the time of initialization [R(n) < R(n-1)].
19	13	Abnormal acceleration/deceleration step pulse number at the time of initialization [S(n) < 2].

3 - 1 - 2 Data register (at read)

This register is used to read data which is readable by status read command. Data must be read by referring to the OBF bit of the status register. More information is provided in **Section 3-4** (**Register read command**).

3 - 1 - 3 Command register (write only)

This register is for writing the command code for each command, including the initialization command, operation command, status read command, auxiliary command, etc. Writing can only be done when the IBF bit of the status register indicates "0".

3 - 1 - 4 Data register (at write)

This register is for writing, after writing each command code, the data necessary for each command (e.g., pulse rate, operation pulse, etc.) Writing can only be done when the IBF bit of the status register reads "0". Information on the order of writing is provided in the section discussing each command. Upon completion of the writing of the necessary data, **PPMC-111** performs the necessary internal processing and then, if the RUN terminal indicates "H", operates according to the command/data.

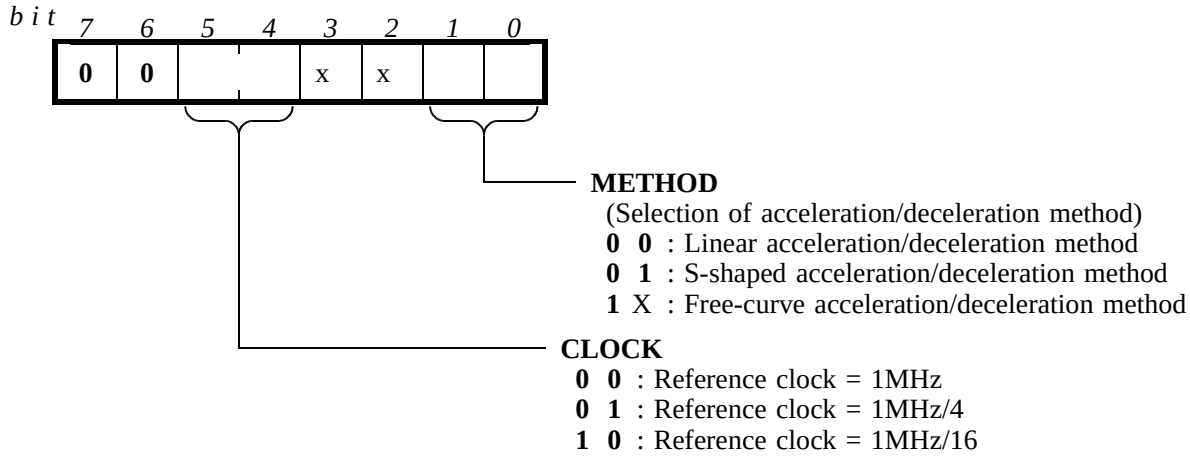
3 - 2 Initialization commands

Upon power resetting, the host processor is required to first issue to **PPMC-111** an initial setting command. The acceleration/deceleration method and speed range are chosen and conveyed in the form of an initialization command code.

If the linear acceleration/deceleration method or S-shaped acceleration/deceleration method is chosen, data necessary for acceleration/deceleration operations (i.e., number of acceleration/deceleration steps, pulse rate and pulse number of each acceleration/deceleration step) are automatically generated inside **PPMC-111** by setting three (3) sets of data, namely, the starting pulse rate, pulse rate at high speed and acceleration/deceleration pulse number (number of acceleration/deceleration pulses).

If the free-curve acceleration/deceleration method is chosen, all the data necessary for acceleration/deceleration operations (i.e., number of acceleration/deceleration steps, as well as the pulse rate and pulse number for each acceleration/deceleration step) must be provided via the host processor.

<**Initialization command code**>



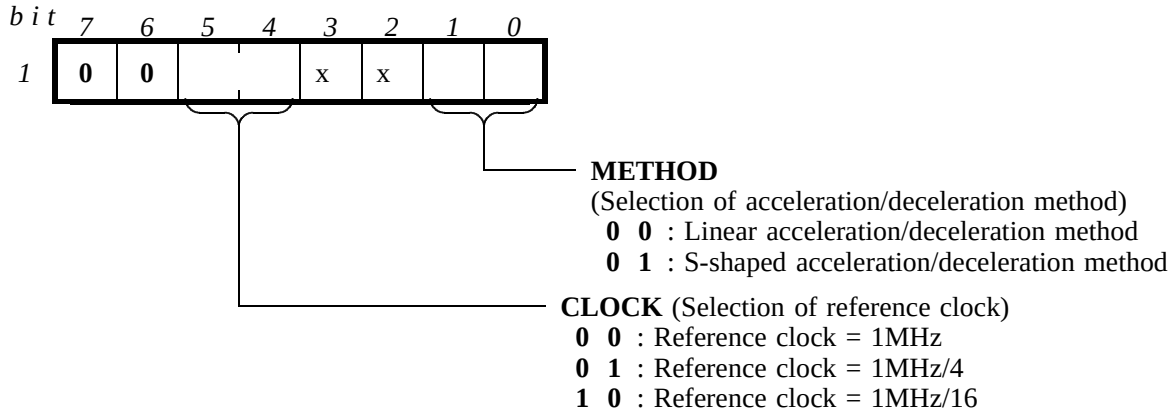
xindicates inefficacy

Fig. 3-2

3 - 2 - 1 Initialization command for linear/ S-shaped acceleration/deceleration method

In performing an initialization command for the linear or S-shaped acceleration/deceleration method, three (3) sets of data, namely, the starting pulse rate, pulse rate at high speed and acceleration/deceleration pulse numbers, shall be fed after the command code.

<Initialization command code for linear/S-shaped acceleration/ deceleration method>



xindicates inefficacy

<Initialization data for linear/S-shaped acceleration/ deceleration method>

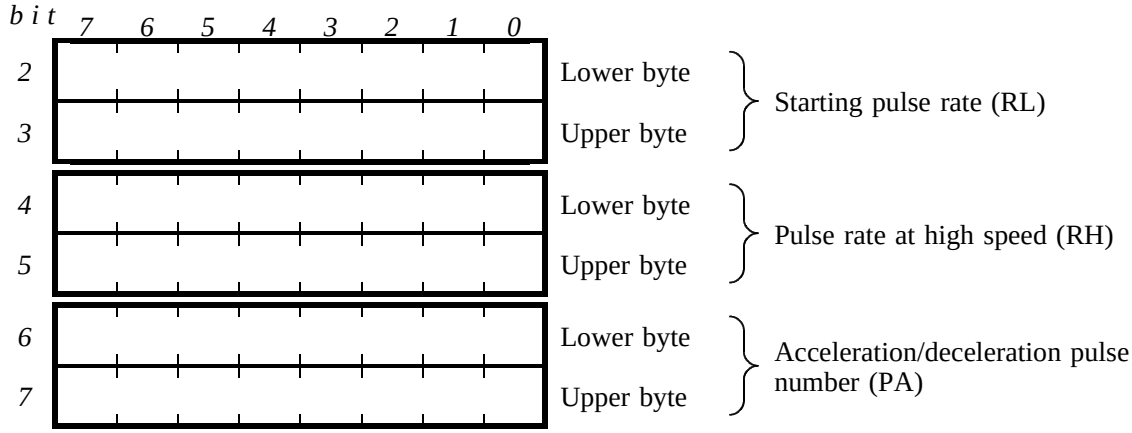


Fig. 3-3

Initialization command for the linear or S-shaped acceleration/deceleration method shall be carried out by writing command codes and data in the order numbered on the left side of **Fig. 3-3**. **Fig. 3-6** shows the same information transformed into a flow chart. The starting pulse rate, pulse rate at high speed and acceleration/deceleration pulse number shall be provided in the form of 16-bit data, while each datum shall be divided into upper and lower bytes and the lower byte data shall be provided first. **Equations 3-1** and **3-2** show the correlation between the starting pulse rate, pulse rate at high speed and pulse output speed. **Figures 3-4** and **3-5** show the correlation between each datum and acceleration/deceleration operation.

$$SH = \frac{Tclock}{RH} \quad \text{----- } \textbf{Equation 3-1}$$

SH : High speed (ppS) RH : Pulse rate at high speed
Tclock : Reference clock

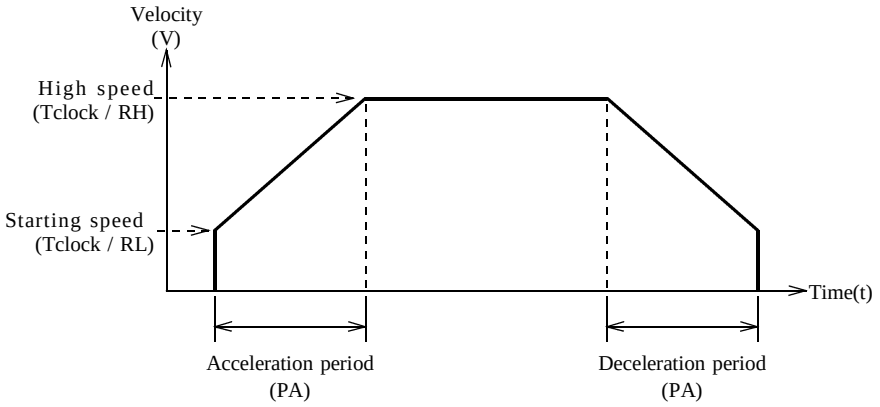
$$SL = \frac{Tclock}{RL} \quad \text{----- Equation 3-2}$$

SL : Starting speed (ppS) RL : Starting pulse rate
Tclock : Reference clock

Table 3-3 shows the correlation between the pulse output speed range and reference clock of **PPMC-111** based on the equations above.

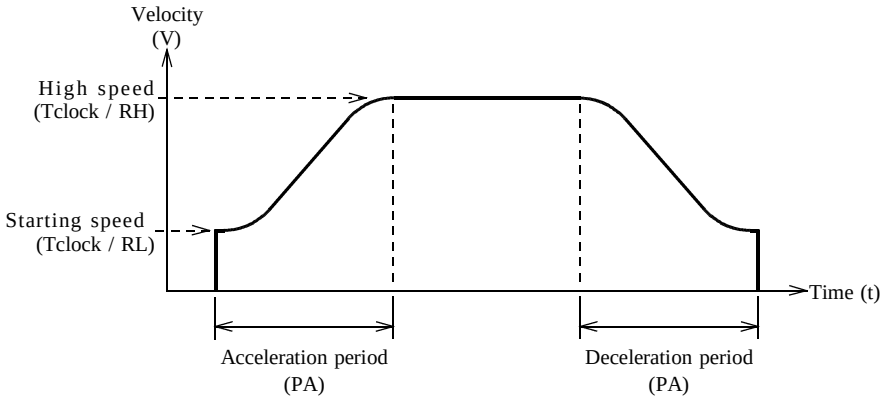
Table 3-3 (Reference clock and pulse output speed range)

Referrence clock (Tclock)	Pulse output speed range
1MHz	30.52ppS to 66.67kppS
1MHz / 4	7.63ppS to 16.67kppS
1MHz / 16	1.91ppS to 4.17kppS



(Acceleration/deceleration operation by linear acceleration/deceleration method)

Fig. 3-4 (Correlation between initialization command data and acceleration/ deceleration operation)



(Acceleration/deceleration operation by S-shaped acceleration/deceleration method)

Fig. 3-5 (Correlation between initialization command data and acceleration/ deceleration operation)

The value of available pulse rate is subject to the restrictions represented in **equations 3-3** and **3-4**. Failure to satisfy these conditions results in a command error, providing error No.**10**. If **equation 3-5** is not satisfied, error No.**12** is provided.

RL = 16 (0010h) to 32767 (7FFFh) ----- **Equation 3-3**

RH = 15 (000Fh) to 32766 (7FFEh) ----- **Equation 3-4**

RH < RL ----- **Equation 3-5**

Acceleration/deceleration pulse number refers to the number of operation pulses delivered during the acceleration or deceleration period. The previously-set acceleration/deceleration pulse number tells how many pulses it requires from booting (start of pulse output) to the high speed or how many pulses it requires from the start of deceleration to the final stop.

The value of available pulse number is subject to the restrictions represented in **equation 3-6**. Failure to satisfy this condition results in a command error, providing error No.**11**.

PA = 8 or over ----- **Equation 3-6**

PA : Acceleration/deceleration pulse number

Fig. 3-6 is a flow chart indicating the flow of issue of initialization command for the liner or S-shaped acceleration/deceleration method.

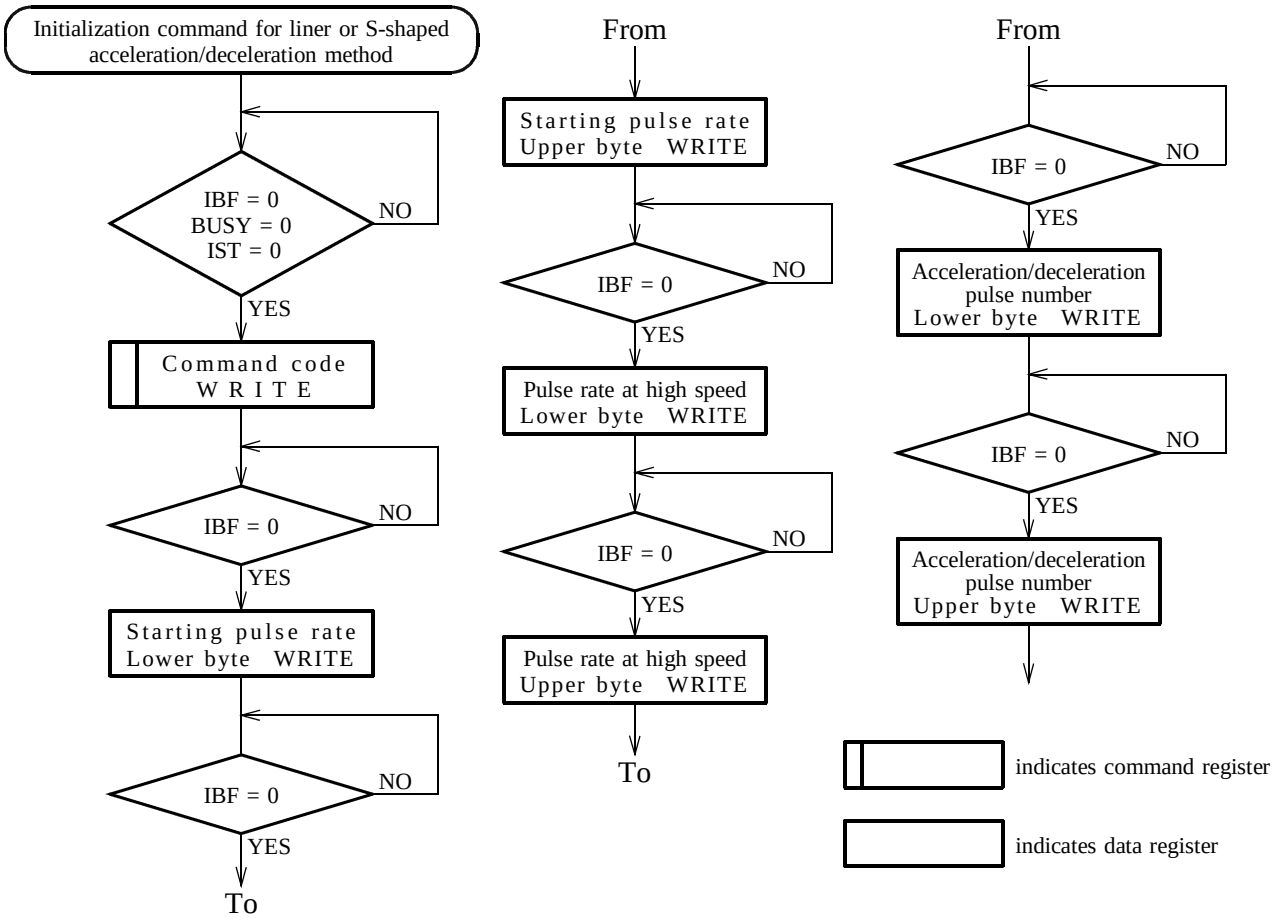
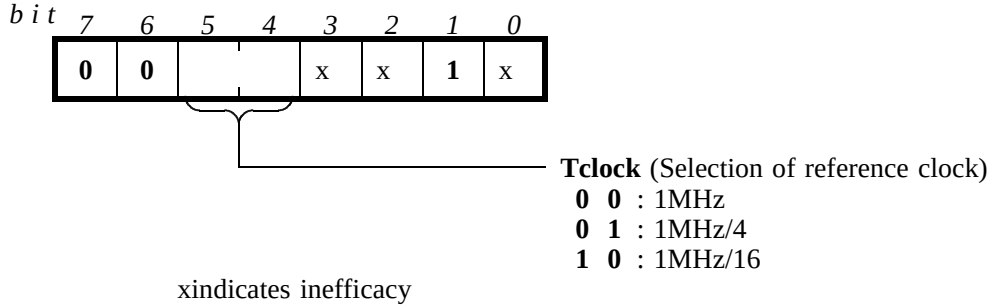


Fig. 3-6 (Flow chart of initialization command for linear or S-shaped acceleration/deceleration method)

3 - 2 - 2 Initialization command for free-curve acceleration/ deceleration method

In performing initialization command for the free-curve acceleration/deceleration method, all data necessary for acceleration/deceleration operations must be fed via host processor after the instruction code. Specifically, the number (N) of acceleration/deceleration steps, pulse rate at high speed, pulse rate [R(n)] for each acceleration/deceleration step, and pulse number [S(n)] for each acceleration/deceleration step shall be defined and fed into **PPMC-111**.

<**Initialization command code for free-curve acceleration/ deceleration method**>



x indicates inefficacy

<**Initialization data for free-curve acceleration/deceleration method**>

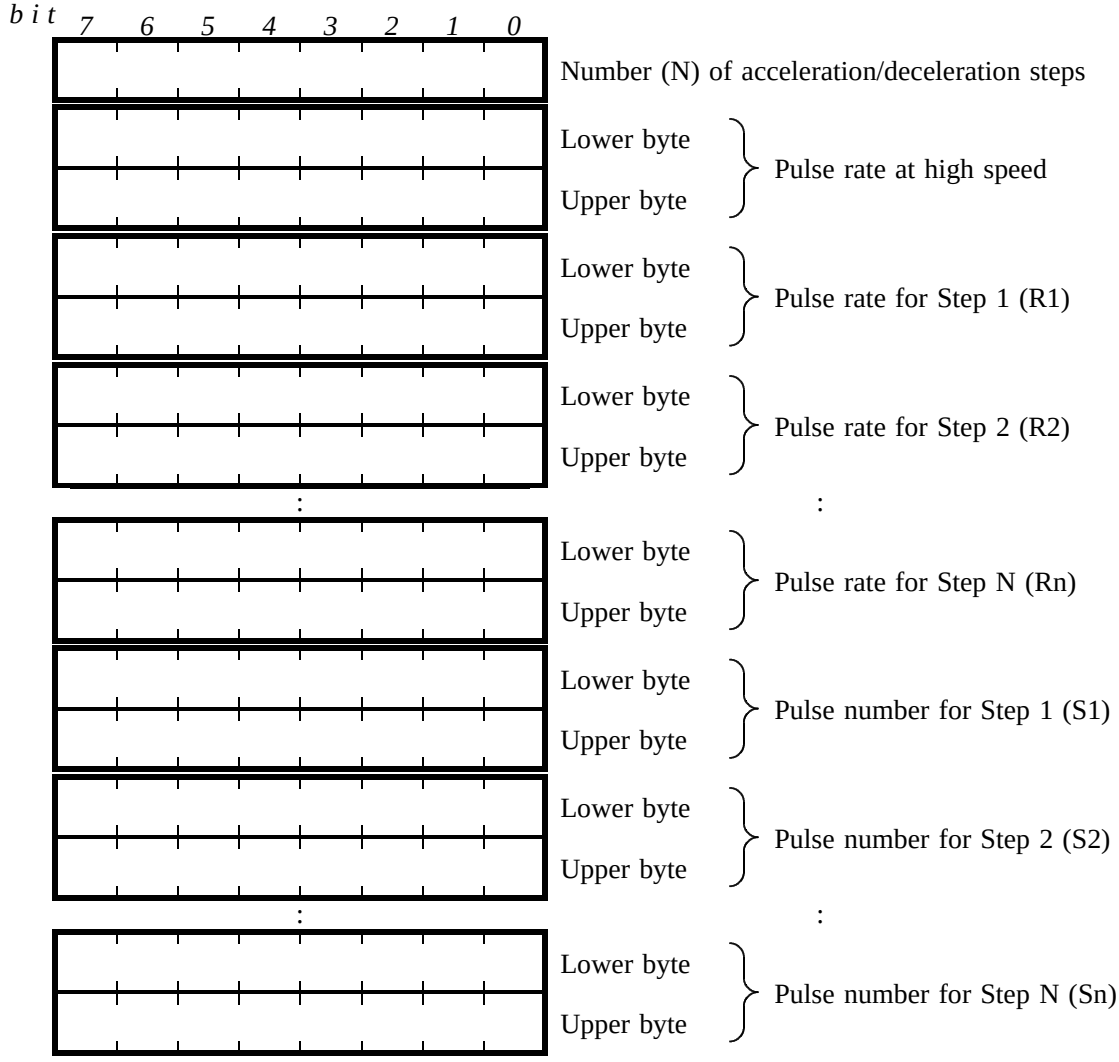


Fig. 3-7

The value of the number(N) of acceleration/deceleration steps, pulse rate [R(n)] for each acceleration /deceleration step, and pulse number [S(n)] for each acceleration/deceleration step are subject to the restrictions represented in **equations 3-7**, **3-8** and **3-9**.

Number (N) of acceleration/deceleration steps

$2 \leqq N \leqq 96$ ----- **Equation 3-7**

Pulse rate [R(n)] for each acceleration/deceleration step

$000Fh \leqq R(n) \leqq R(n-1) \leqq 7FFFh$ ----- **Equation 3-8**

Pulse number [S(n)] for each acceleration/deceleration step

$2 \leqq S(n)$ ----- **Equation 3-9**

In general, relatively smooth acceleration/deceleration operation can be achieved by having small incremental speed change settings for the period immediately after booting and immediately before reaching high speed.

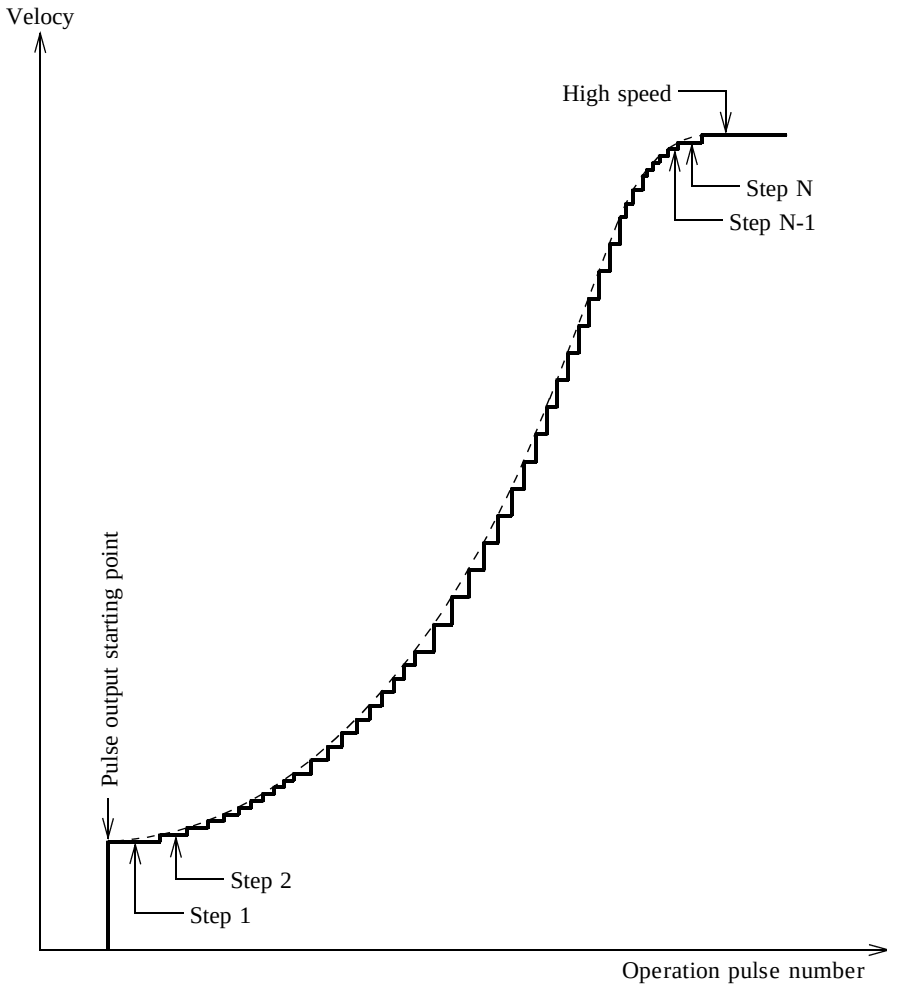


Fig. 3-8 (Sample acceleration curve at the time of initialization by free-curve acceleration/deceleration method)

Fig. 3-9 is a flow chart indicating the flow of issue of initialization command for the free-curve acceleration/deceleration method.

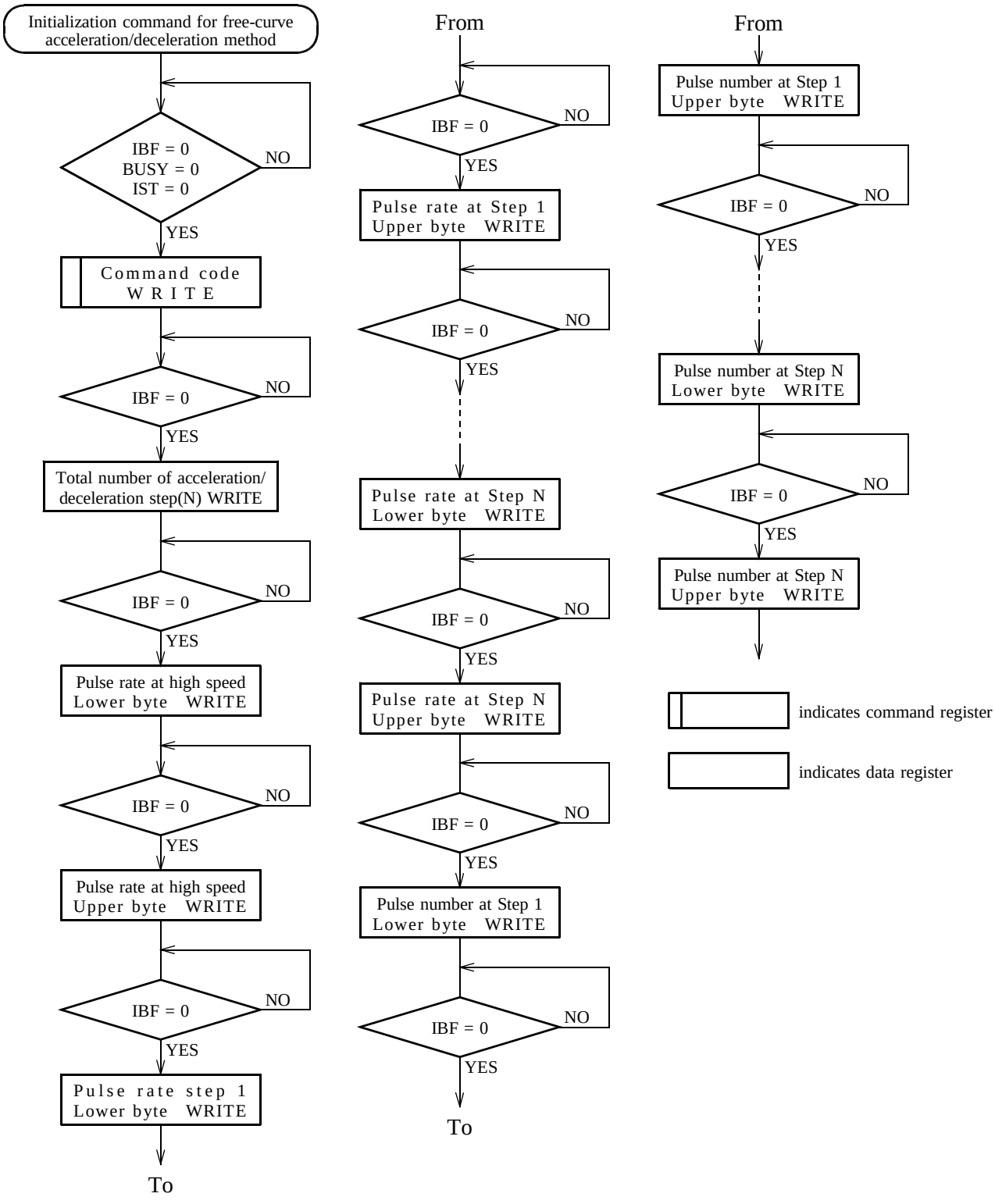


Fig. 3-9 (Flow chart of initialization command for free-curve acceleration/deceleration method)

3 - 3 Operation command

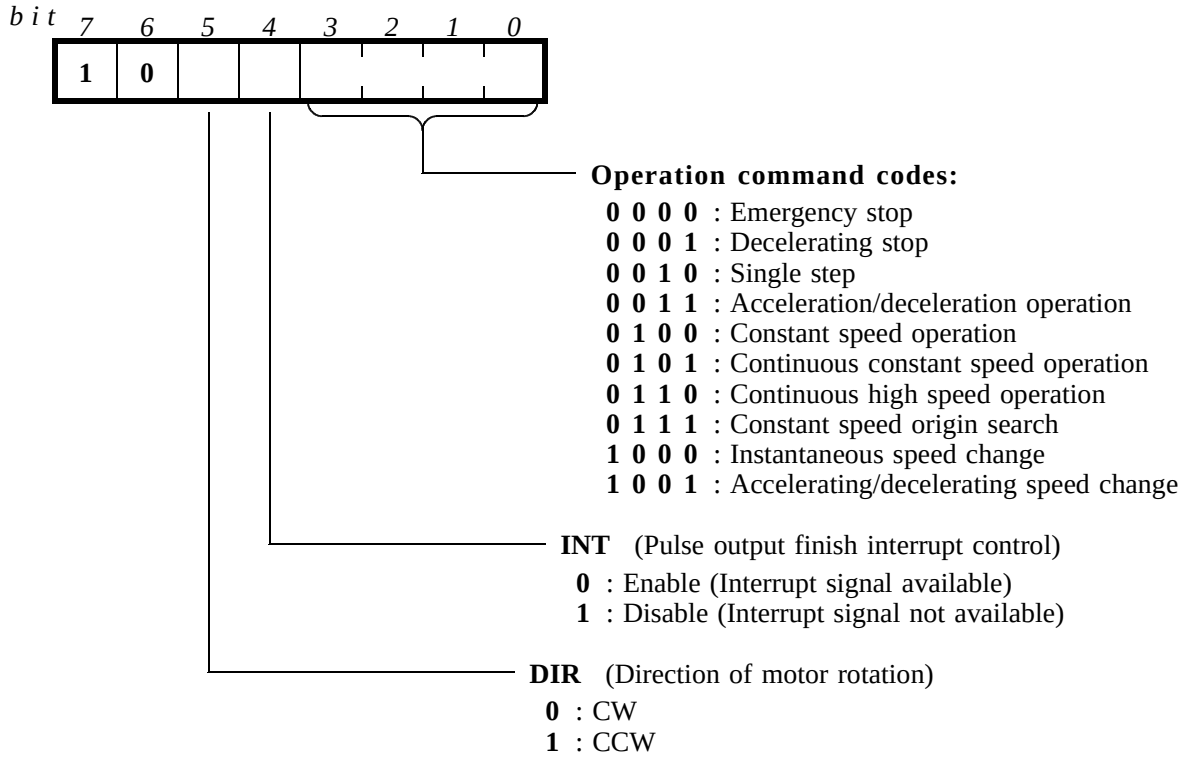


Fig. 3-10 (Bit configuration of operation command code)

3-3-1 Emergency stop

Immediately upon receipt of this command during acceleration/deceleration operation or constant speed operation, **PPMC-111** stops pulse output. Administration of this command when the stepper motor is operating in a speed range higher than its self-boot range may result in being out of step most likely due to inertia from the motor load.

If the INT bit of this command is "0," the interrupt signal ($\overline{INT}$) is output upon termination of pulse output. The DIR bit (direction of motor rotation) has no meaning to this command.

This command only carries a command code and carries no data. This command is significant only during pulse output (Busy = 1); therefore, this command must be written only after the status register's IBF and IST bits, as well as the BUSY bit, are checked.

This command must be used carefully because **PPMC-111** is unable to detect any control input signals, including limit signals, from the start of receiving this command code (IST bit = "1") to the termination of pulse output (IST bit = "0").

<**Emergency stop command**>

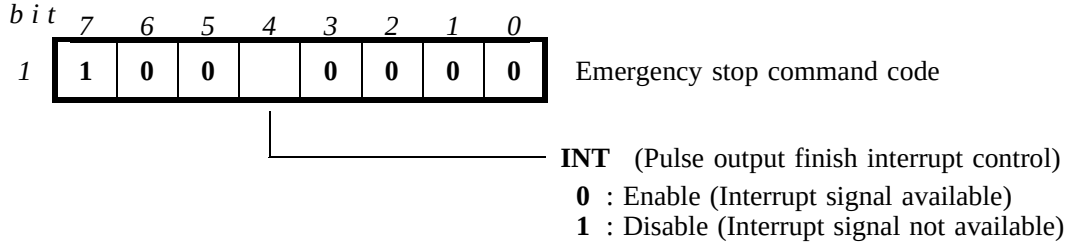


Fig. 3-11

Fig. 3-12 is a flow chart indicating the flow of issue of emergency stop command.

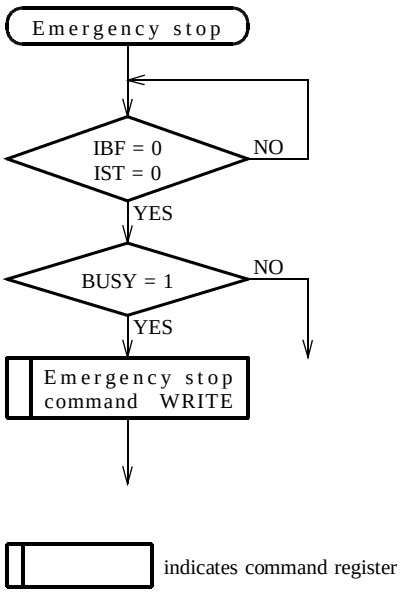


Fig. 3-12 (Flow chart of emergency stop command)

3-3-2 Decelerating stop

Immediately upon receipt of this command, **PPMC-111** starts deceleration and completes pulse output at the starting speed. The interrupt signal ($\overline{INT}$) is output if the INT bit of this command reads "0."

If the operation speed at the receipt of this command is equivalent to the starting speed, which was designated at the time of initialization, it immediately stops without deceleration. The DIR bit (direction of motor rotation)is meaningless with this command. This command only carries a command code and carries no data.

This command is significant only during pulse output (Busy = 1); therefore, this command must be written only after the status register's IBF and IST bits, as well as the BUSY bit, are checked.

This command must be used carefully because **PPMC-111** is unable to detect any control input signals, including limit signals, from the start of receiving this command code (IST bit = "1") to the termination of pulse output (IST bit = "0").

<**Command for decelerating stop**>

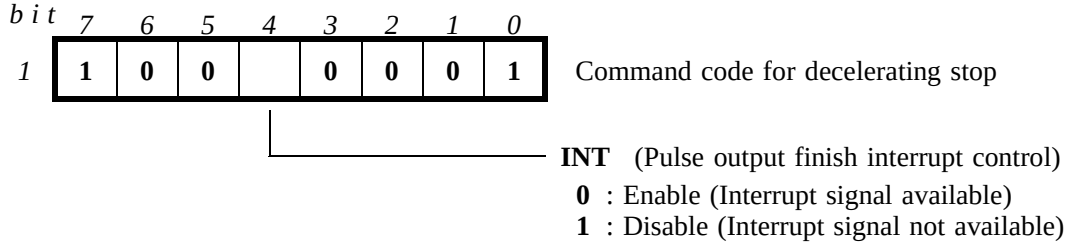


Fig. 3-13

Fig. 3-14 is a flow chart indicating the flow of issue of command for decelerating stop.

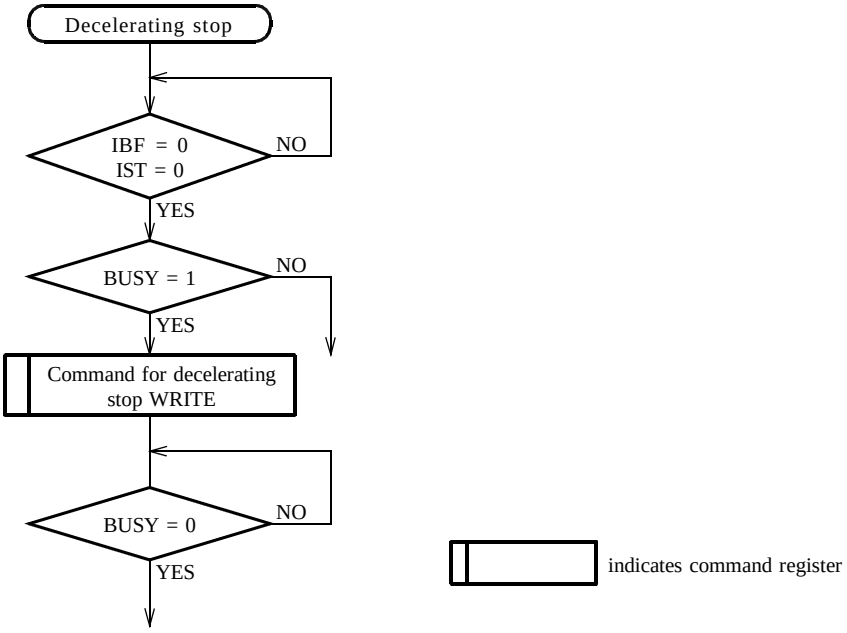


Fig. 3-14 (Flow chart of command for decelerating stop)

3 - 3 - 3 Single step

This command enables movement in an increment/decrement of a single pulse by a command transmitted from the host processor. This command is used when the host processor itself intends to check the position. The timing, etc. of execution of this command must be processed on the host processor if this command must be used continually.

This command only carries a command code and carries no data. This command must be written only after the status register's IBF and IST bits, as well as the BUSY bit, are checked.

<**Single step operation command**>

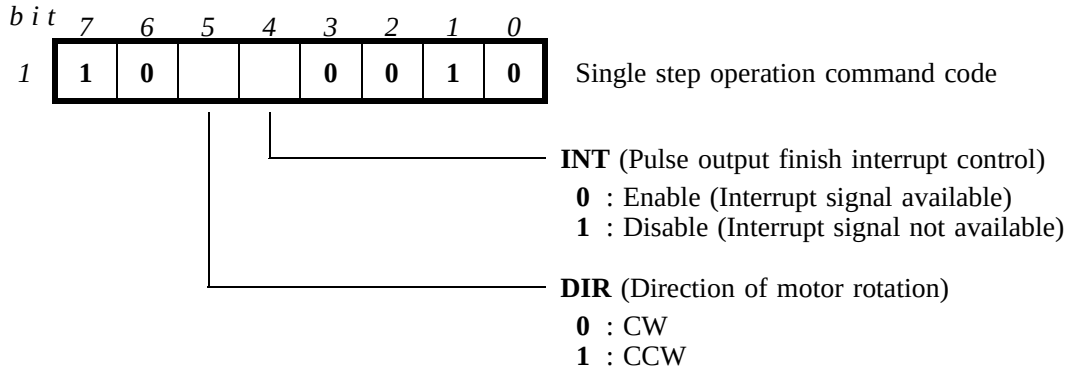


Fig. 3-15

Fig. 3-16 is a flow chart indicating the flow of issue of single step command.

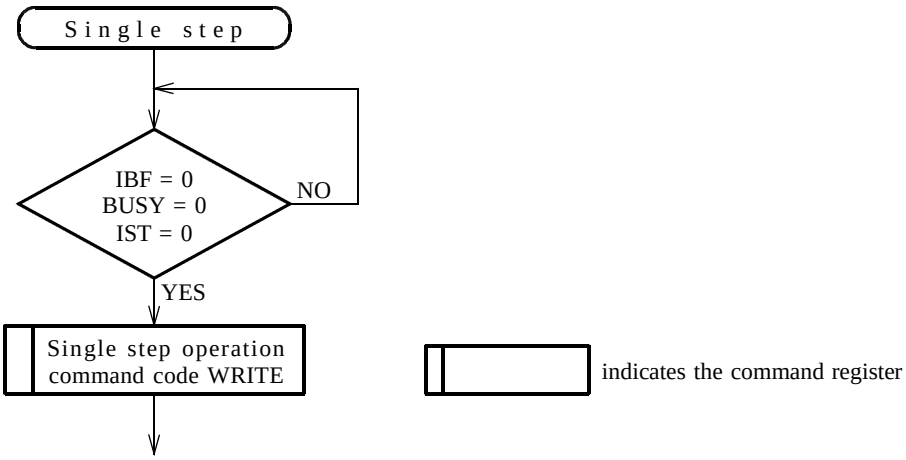


Fig. 3-16 (Flow chart of single step operation command)

3 - 3 - 4 Acceleration/deceleration operation

This command is for acceleration/deceleration operation according to the acceleration/deceleration curve set at the time of initialization together with the command. Designation of a 3-byte operation pulse number is required together with the command. Upon receipt of this command, **PPMC-111** begins pulse output at the starting speed designated at the time of initialization. **PPMC-111** accelerates up to high speed with the designated acceleration/deceleration pulse number. After high speed operation, once it reaches the point where deceleration begins, deceleration occurs with the designated acceleration/deceleration pulse number down to the starting speed where pulse output completes. Setting an operation pulse number smaller than a value twice the designated acceleration/deceleration pulse number leads to the formulation of triangle operation in which deceleration begins in the middle of acceleration. If the INT bit is set at "0," the interrupt signal ($\overline{\text{INT}}$)will be available upon termination of pulse output.
This command must be written only after the status register's IBF, BUSY and IST bits are checked. An operation pulse number must be written while confirming the IBF bit.

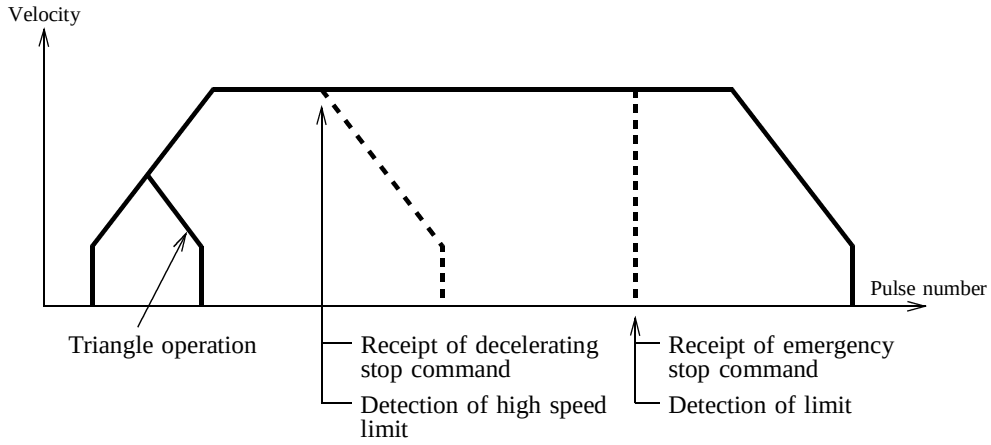


Fig. 3-17 (Sample acceleration/deceleration operation)

<Acceleration/deceleration operation command/data>

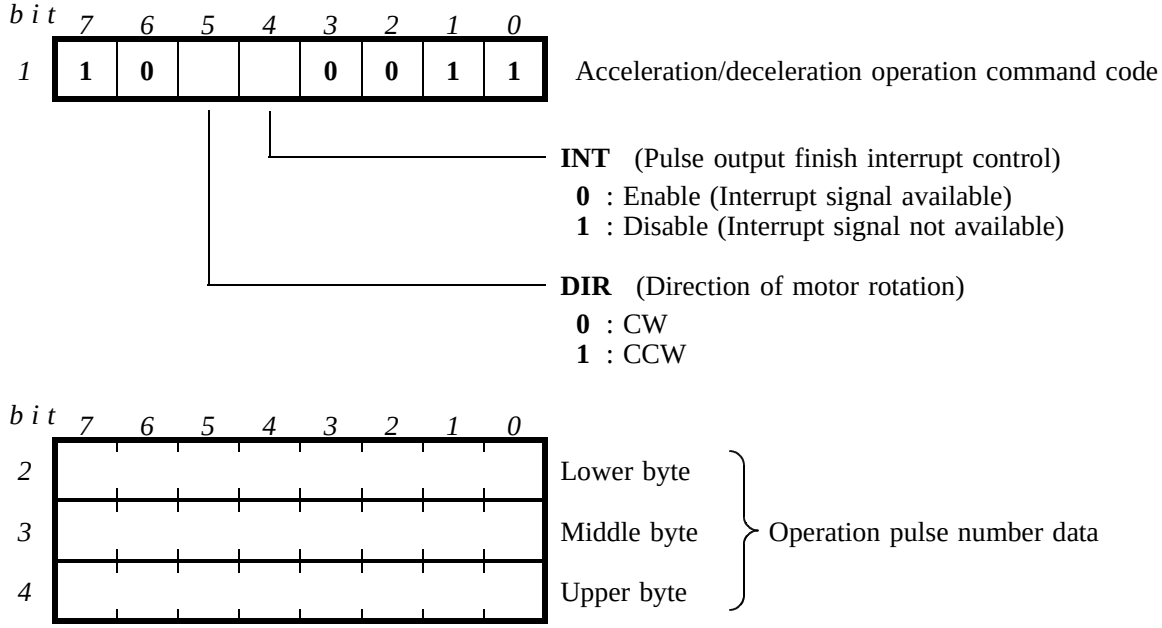


Fig. 3-18

Fig. 3-19 is a flow chart indicating the flow of issue of acceleration/deceleration operation command.

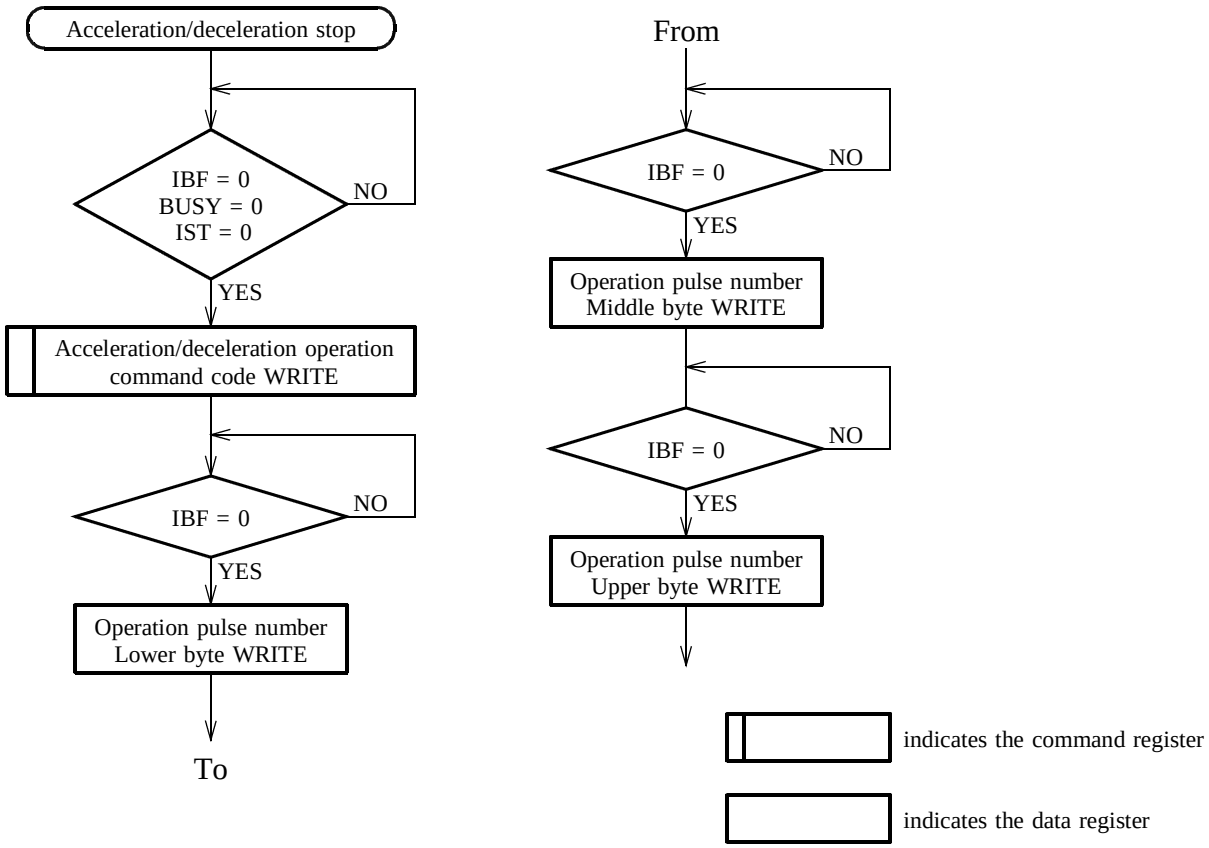


Fig. 3-19 (Flow chart of acceleration/deceleration operation)

3 - 3 - 5 Constant speed operation

This command enables the output of a designated number of pulses at a designated speed. It is necessary to designate after the command code a constant speed pulse rate of two (2) bytes and an operation pulse number of three (3) bytes. The interrupt signal (INT) will be available upon termination of pulse output if the INT bit is set at "0." This command code must be written only after the status register's IBF, BUSY and IST bits are checked. Data must be written in the correct order from the lower byte while confirming the IBF bit.

The value of constant speed pulse rate designated by this command must be within the range of the starting pulse rate set at the time of initialization and the pulse rate at high speed ($\leq$RL, $\geq$RH). Designation of a constant speed pulse rate outside this range leads to a command error (command error code #**13**).

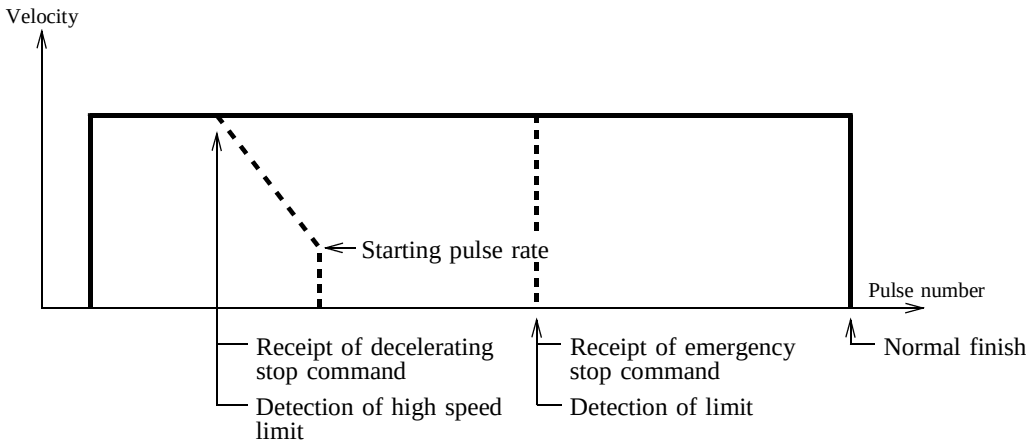


Fig. 3-20 (Sample constant speed operation)

<**Constant speed operation command/data**>

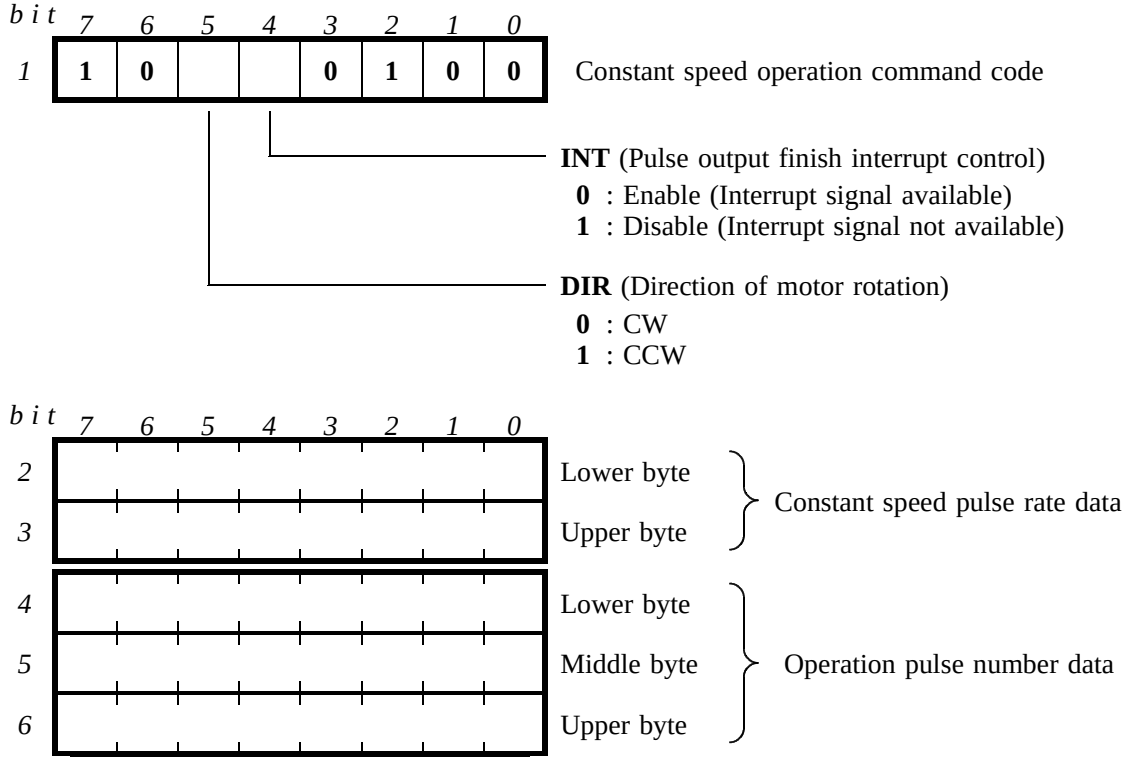


Fig. 3-22 is a flow chart indicating the flow of issue of constant speed operation command.

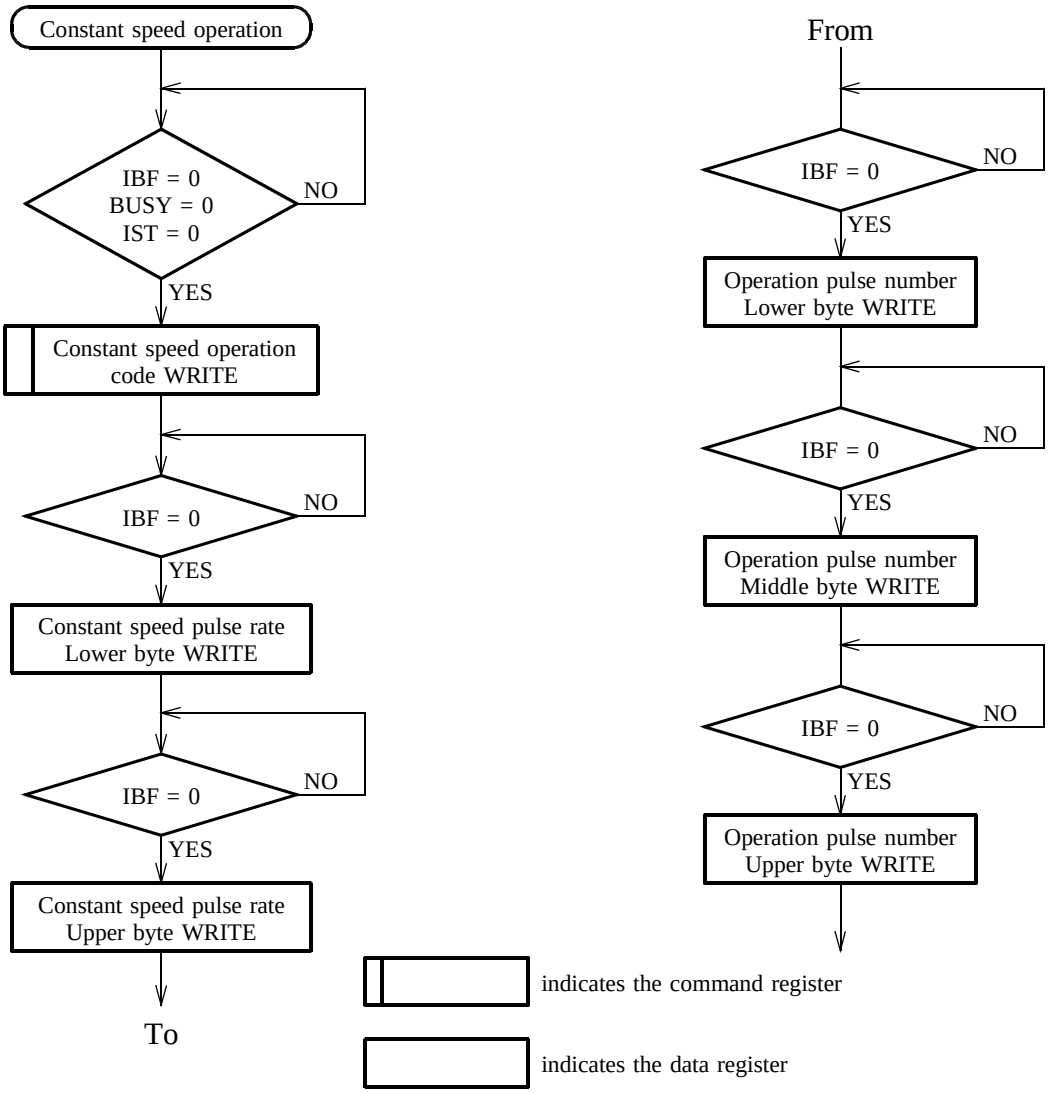


Fig. 3-22 (Flow chart of constant speed operation)

3 - 3 - 6 Continuous constant speed operation

This command enables the continuous output of pulses at a designated speed until the detection of the limit signal. It is necessary to designate a constant speed pulse rate of two (2) bytes after the command code. It makes an emergency stop once a limit signal ($\overline{FL}$ or $\overline{BL}$) corresponding to the rotating direction has been detected. Output of pulses continues endlessly if there is no detection. A limit signal corresponding to the rotating direction refers to the $\overline{FL}$ limit in the case of pulse output in the CW direction, or the $\overline{BL}$ limit in the case of pulse output in the CCW direction. Limit signals in the direction opposite the direction of rotation shall be disregarded. The interrupt signal ($\overline{INT}$) will be available upon termination of pulse output if the INT bit is set at "0".

This command code must be written only after the status register's IBF, BUSY and IST bits are checked. Data must be written in the correct order from the lower byte while confirming the IBF bit.

The value of the constant speed pulse rate designated by this command must be within the range of the starting pulse rate set at the time of initialization and the pulse rate at high speed ($\underline{\leq}$RL, $\underline{\geq}$RH). Designation of a constant speed pulse rate outside this range leads to a command error (command error code #13).

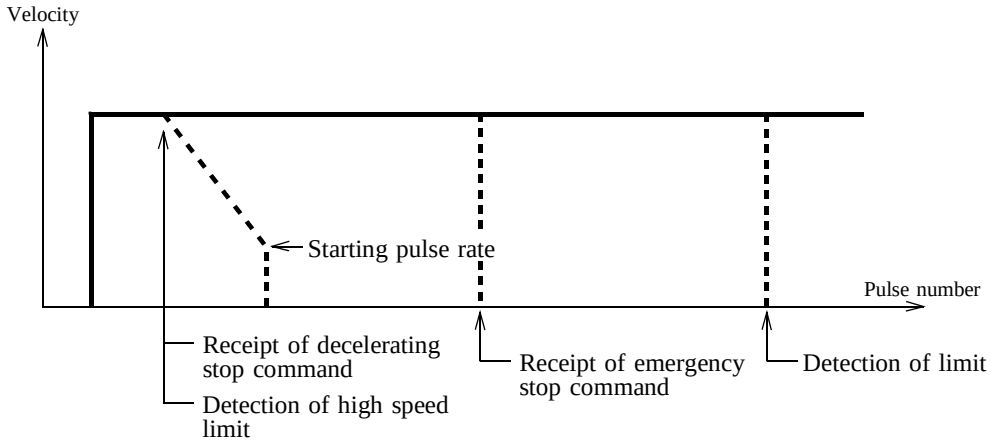


Fig. 3-23 (Sample continuous constant speed operation)

<**Continuous constant speed operation command/data**>

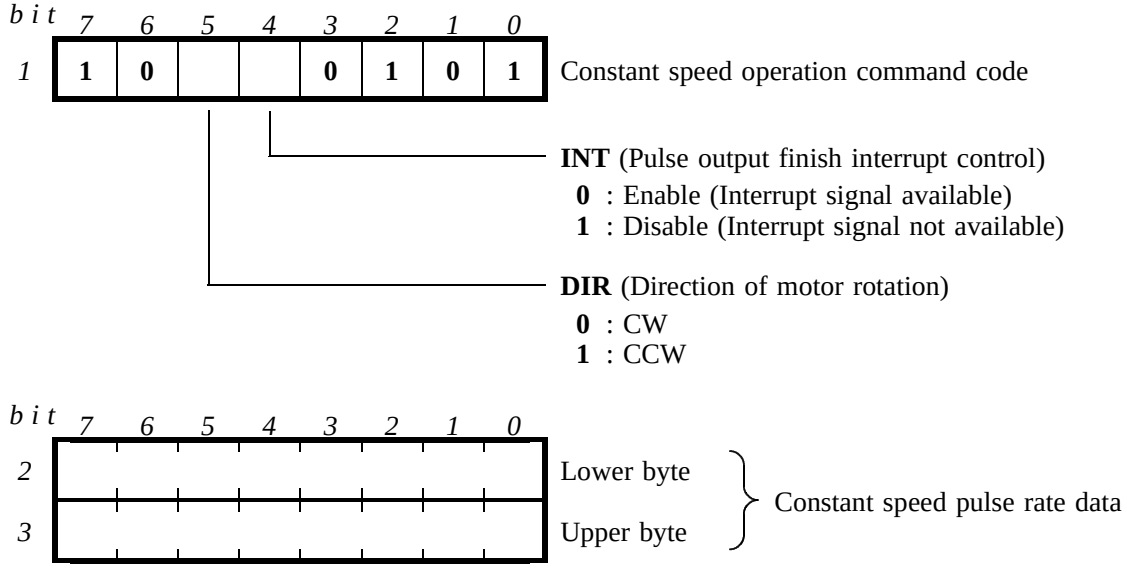


Fig. 3-24

Fig. 3-25 is a flow chart indicating the flow of issue of continuous constant speed operation commands.

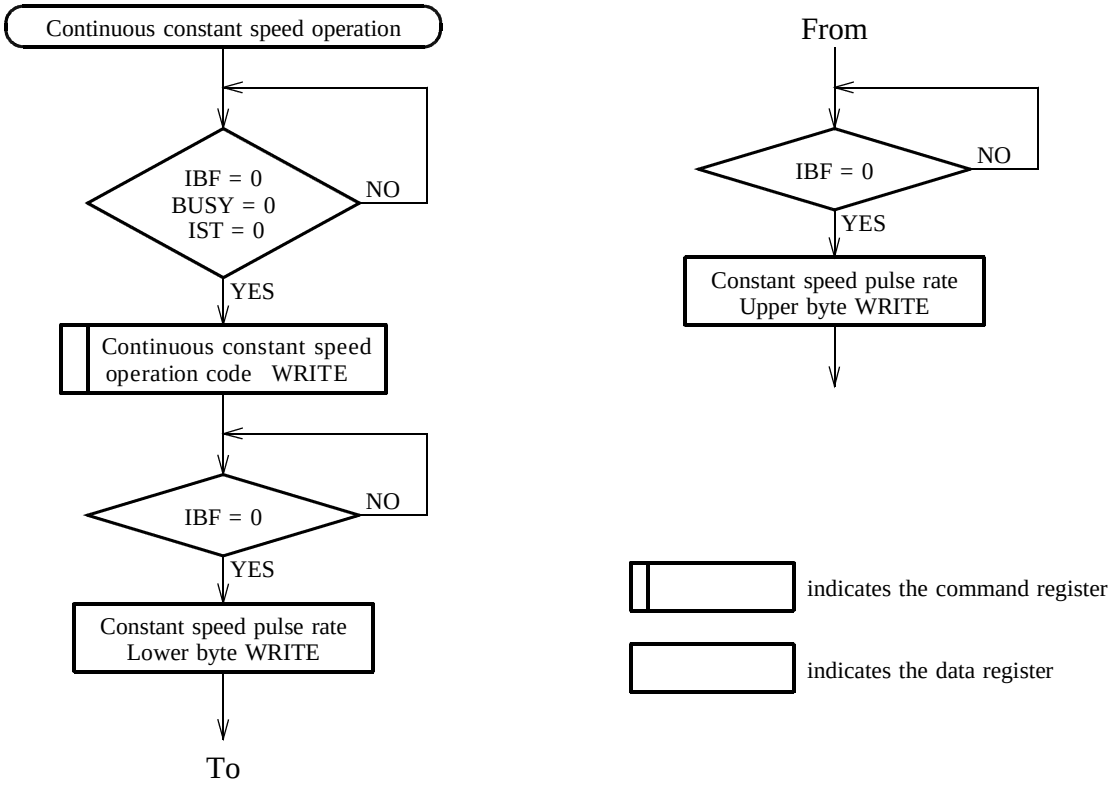


Fig. 3-25 (Flow chart of continuous constant speed operation)

3 - 3 - 7 Continuous high speed operation

This command is for acceleration according to the initialization command and the continuous output of pulses at a high speed until the detection of the high speed limit signal. This command only carries a command code. Data designation is not necessary. It makes a decelerating stop once a high speed limit signal ($\overline{FHL}$ or $\overline{BHL}$) corresponding to the rotating direction has been detected. Output of pulses at a high speed continues endlessly if there is no detection. A high speed limit signal corresponding to the rotating direction refers to the $\overline{FHL}$ limit in the case of pulse output in the CW direction, or the $\overline{BHL}$ limit in the case of pulse output in the CCW direction. High speed limit signals in thedirection opposite the direction of rotation shall be disregarded. The interrupt signal ($\overline{INT}$) will be available upon termination of pulse output if the INT bit is set at "0". The designated detection speed as discussed in **Section 3-5-3** (Decelerating limit detection speed setting command) shall be disregarded in this command.

This command code must be written only after the status register's IBF, BUSY and IST bits are checked.

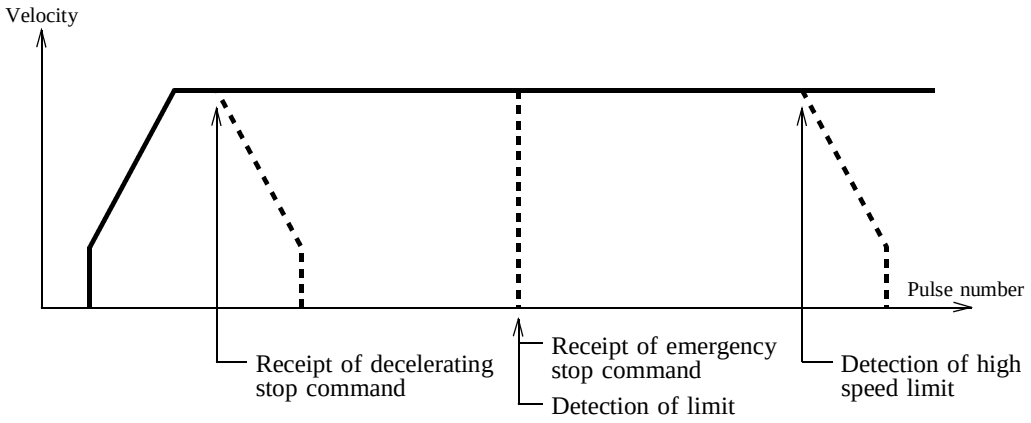


Fig. 3-26 (Sample continuous high speed operation)

<**Continuous constant speed operation command**>

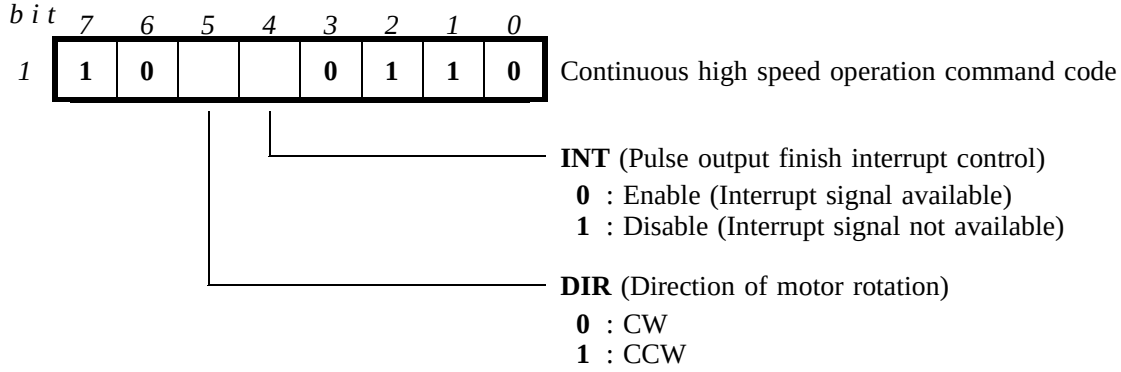


Fig. 3-27

Fig. 3-28 is a flow chart indicating the flow of issue of continuous high speed operation command.

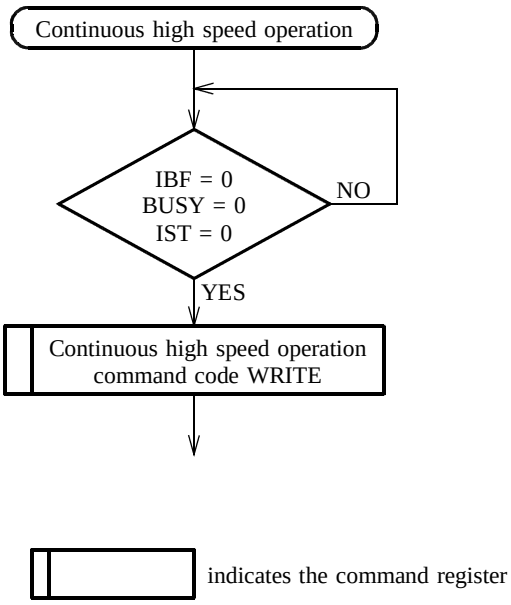


Fig. 3-28 (Flow chart of continuous high speed operation)

3 - 3 - 8 Constant speed origin search operation

This command is for the continuous output of pulses at a designated speed until the detection of the origin signal. It is necessary to designate a constant speed pulse rate of two (2) bytes after the command code. Pulse output is terminated when the origin signal ($\overline{ORG}$) is detected. Output of pulses continues endlessly if there is no detection. The interrupt signal ($\overline{INT}$) will be available upon termination of pulse output if the INT bit is set at "0."

This command code must be written only after the status register's IBF, BUSY and IST bits are checked. Data must be written in the correct order from the lower byte while confirming the IBF bit.

The value of constant speed pulse rate designated by this command must be within the range of the starting pulse rate set at the time of initialization and the pulse rate at high speed ($\underline{\leq}$RL, $\underline{\geq}$RH). Designation of a constant speed pulse rate outside this range leads to a command error (command error code #13).

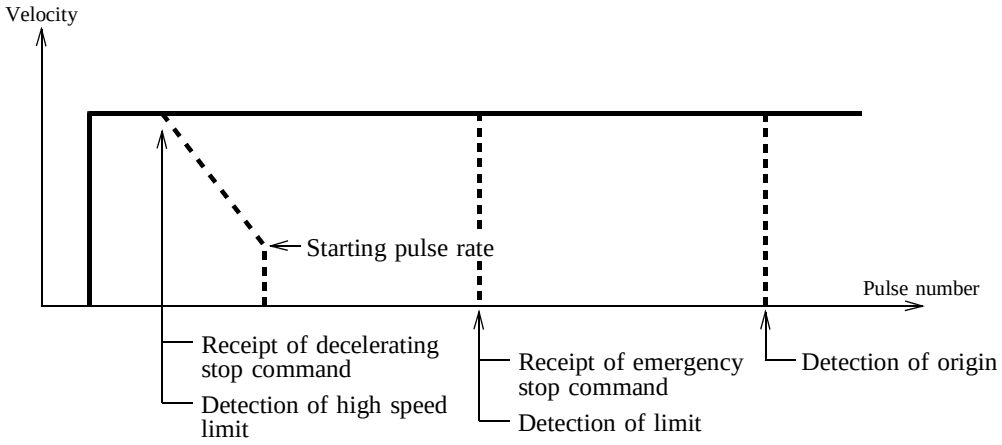


Fig. 3-29 (Sample constant speed origin search operation)

<**Constant speed origin search operation command/data**>

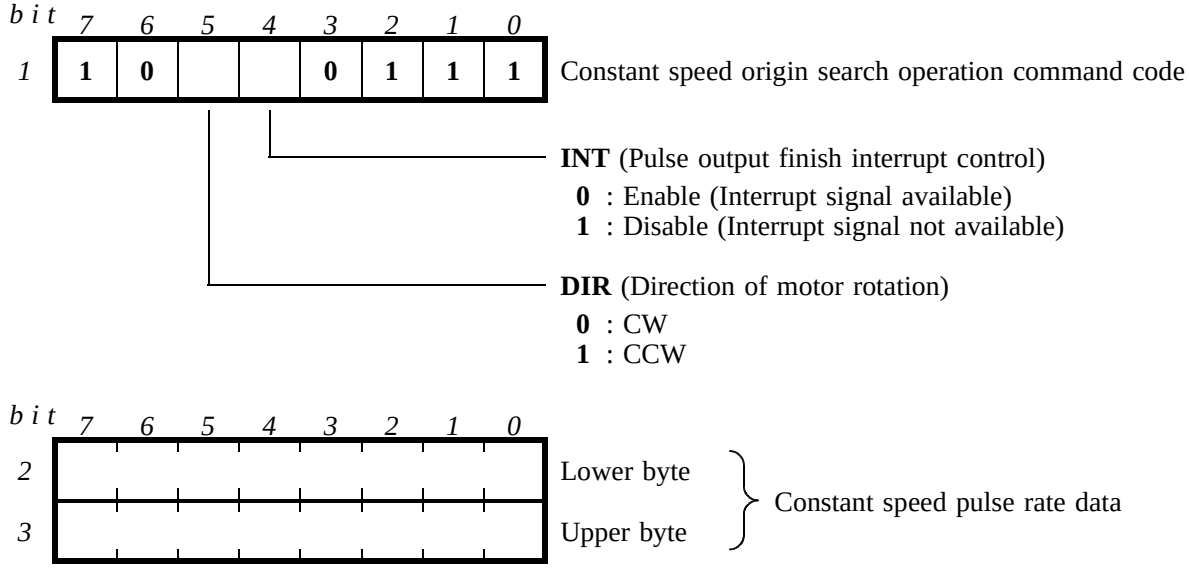


Fig. 3-30

Fig. 3-31 is a flow chart indicating the flow of issue of constant speed origin search operation command.

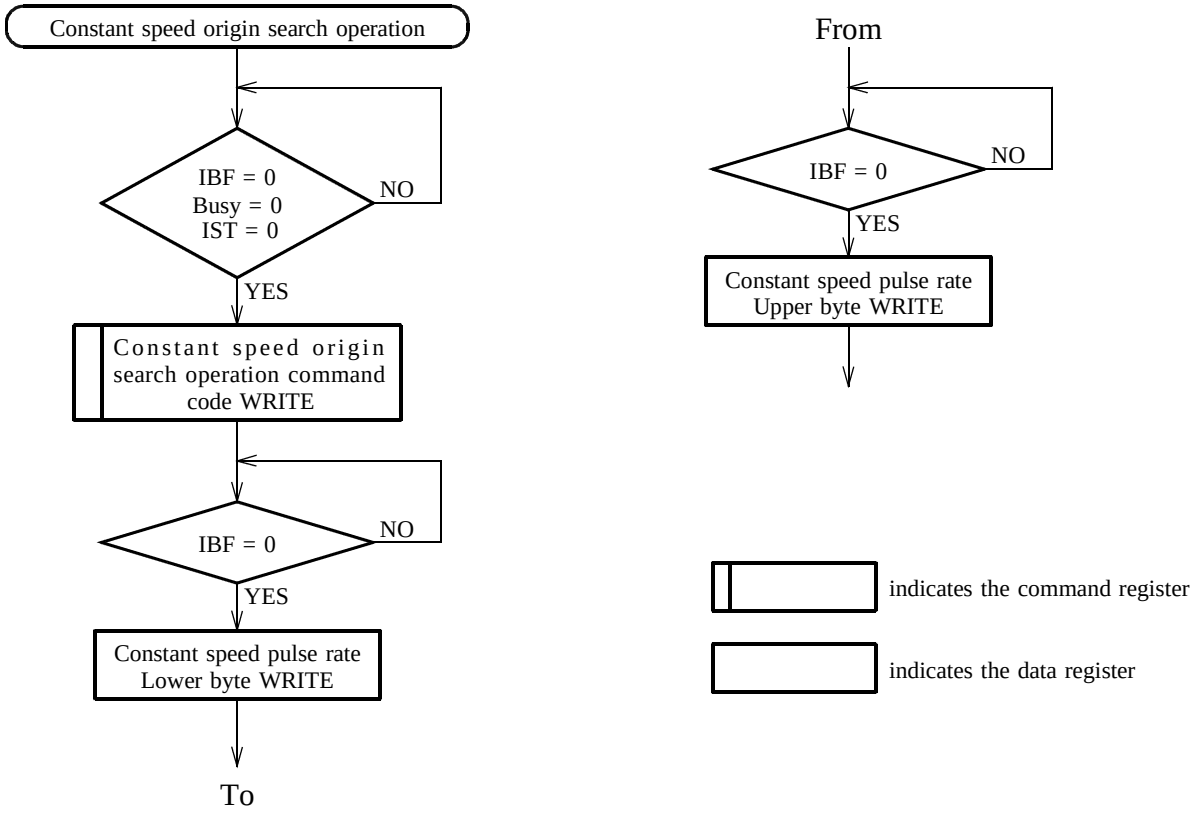


Fig. 3-31 (Flow chart of constant speed origin search operation)

3 - 3 - 9 Instantaneous speed change

This command is used to instantaneously change the operation speed to any designated speed. The command does not affect the number of operation pulses.

This command code must be written only after the status register's IBF, BUSY and IST bits are checked. Data must be written in the correct order from the lower byte while confirming the IBF bit.

The value of constant speed pulse rate designated by this command must be within the range of the starting pulse rate set at the time of initialization and the pulse rate at high speed ($\leq$RL, $\geq$RH). Designation of a constant speed pulse rate outside this range leads to a command error (command error code #13).

If this command is received during pulse output by the acceleration/deceleration operation command, remaining pulses will result because there is no change regarding the deceleration starting point computed within the **PPMC-111** when the acceleration/deceleration operation command is received. The output of these remaining pulses will be carried out at the starting speed as shown in **Fig. 3-32**.

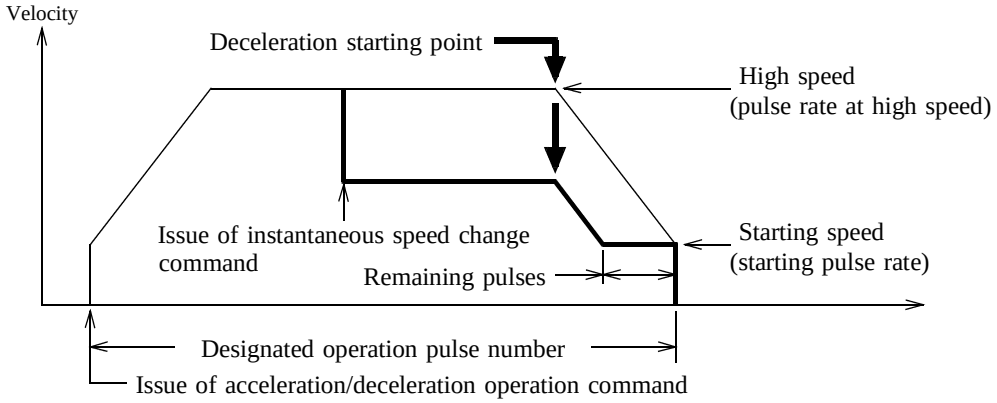


Fig. 3-32

<**Instantaneous speed change command/data**>

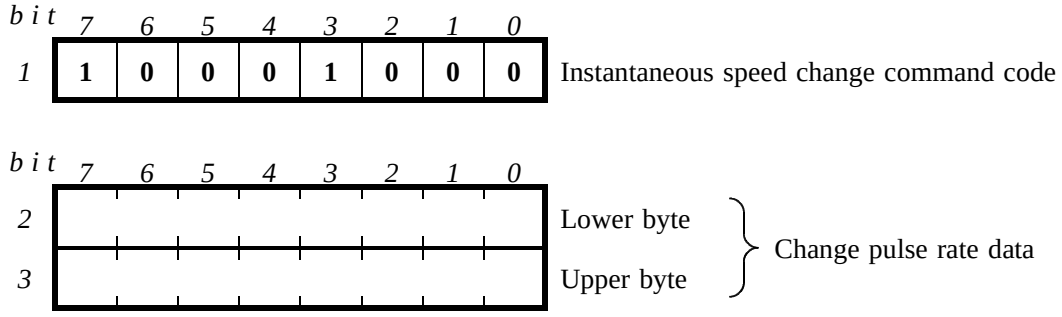


Fig. 3-33

This command must be used carefully because the **PPMC-111** is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to the actual speed change (IST bit = "0").

Fig. 3-34 is a flow chart indicating the flow of issue of instantaneous speed change command.

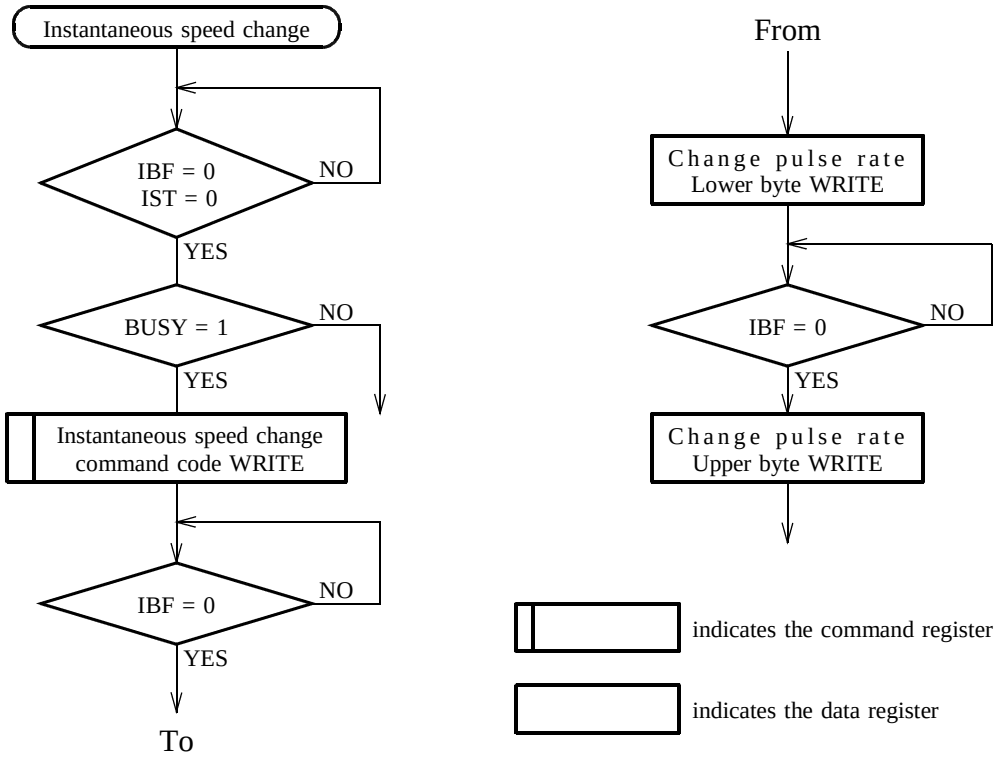


Fig. 3-34 (Flow chart of instantaneous speed change)

3-3-10 Accelerating/decelerating speed change

This command changes a designated operation speed according to the acceleration/deceleration curve set at the time of initialization. The command does not affect the number of operation pulses.

This command code must be written only after the status register's IBF, BUSY and IST bits are checked. Data must be written in the correct order from the lower byte while confirming the IBF bit.

The value of the constant speed pulse rate designated by this command must be within the range of the starting pulse rate set at the time of initialization and the pulse rate at high speed ($\leq$RL, $\geq$RH). Designation of a constant speed pulse rate outside this range leads to a command error (command error code #13).

If this command is received during pulse output by the acceleration/deceleration operation command, remaining pulses will result because there is no change regarding the deceleration starting point computed within the **PPMC-111** when the acceleration/deceleration operation command is received. The output of these remaining pulses will be carried out at the starting speed as shown in **Fig. 3-35**.

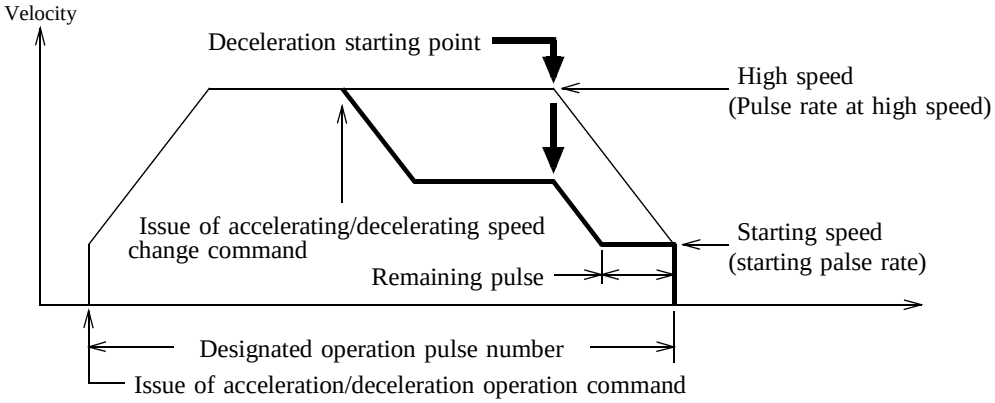


Fig. 3-35

<**Accelerating/decelerating speed change command/data**>

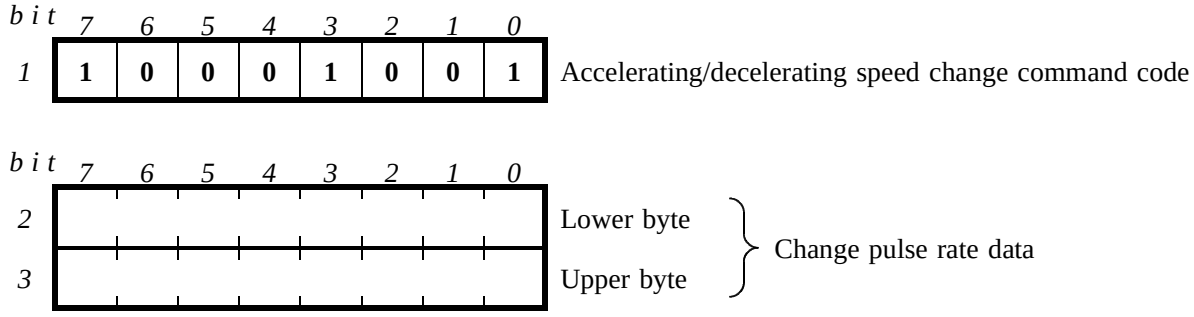


Fig. 3-36

This command must be used carefully because the **PPMC-111** is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to the actual speed change (IST bit = "0").

Fig. 3-37 is a flow chart indicating the flow of issue of accelerating/decelerating speed change command (i.e., command to change speed through acceleration/deceleration).

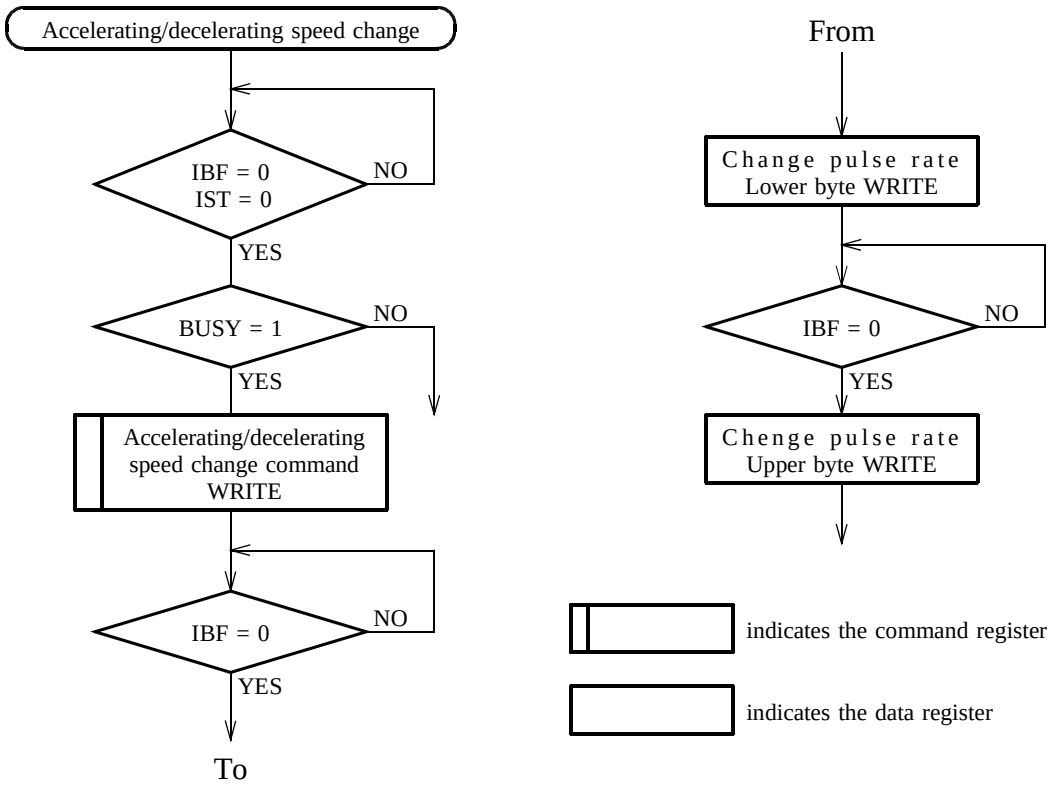


Fig. 3-37 (Flow chart of accelerating/decelerating speed change)

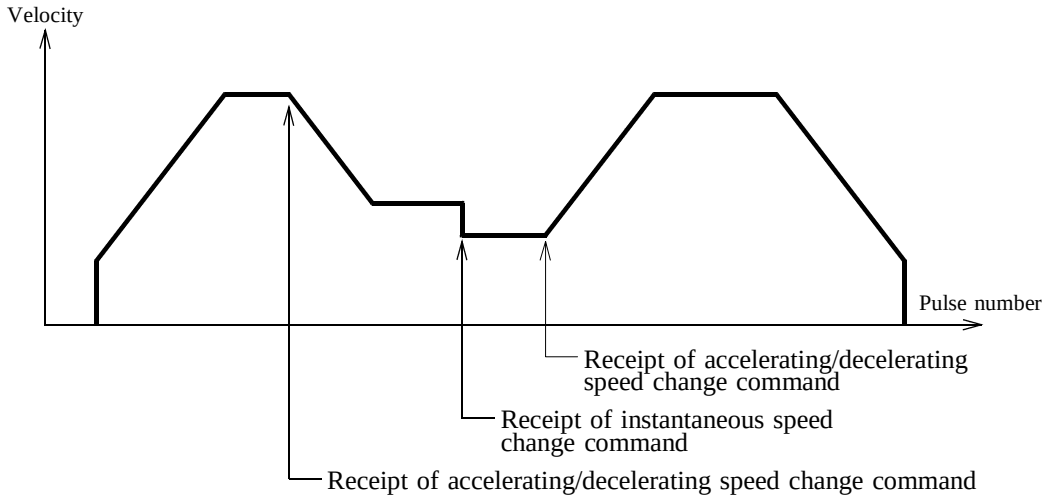


Fig. 3-38 (Sample speed change in accelerating/ decelerating speed change operation)

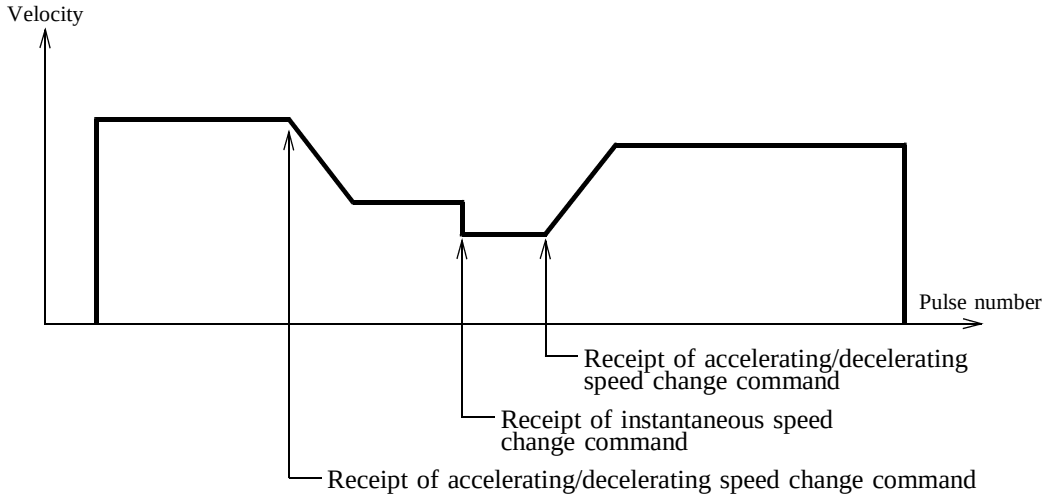


Fig. 3-39 (Sample speed change in constant speed operation)

3 - 4 Internal register read command

This command enables examining of the internal conditions of the **PPMC-111** and the conditions of external input signals. As shown in **Fig. 3-40**, there are five (5) internal register read commands. Reading during pulse output is possible.

<**Internal register read command**>

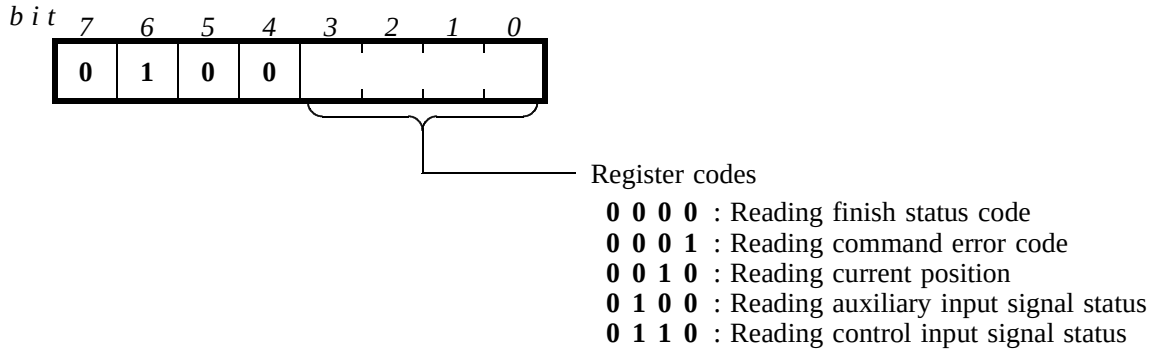


Fig. 3-40 (Internal register read command bit configuration)

3 - 4 - 1 Finish status code read command

This command enables reading of the cause of pulse output. This command, which carries a command code alone, reads out a 1-byte finish status code after the command code is written.

<**Finish status code read command/code**>

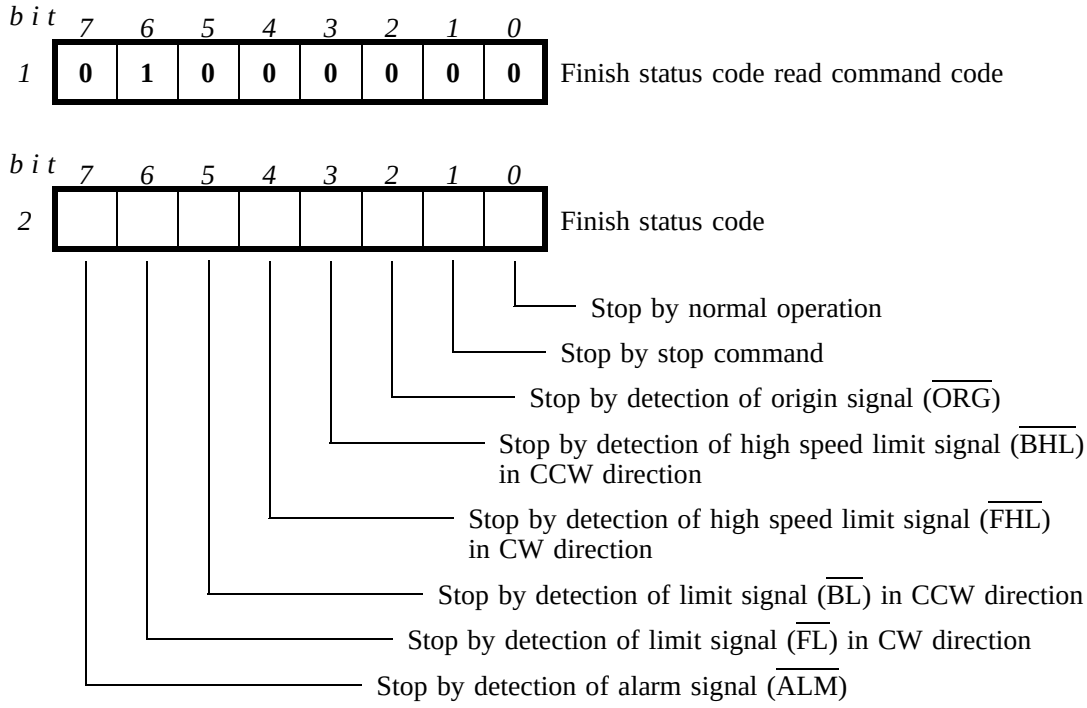


Fig. 3-41

Each finish status code is registered with the internal register of the **PPMC-111** upon termination of pulse output and is maintained during the next pulse output operation. The immediately preceding finish status code can be read for reference during pulse output; however, the preceding finish status code shall be replaced with the most recent finish status code upon termination of the pulse output.
This command must be used carefully during pulse output because the **PPMC-111** is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to when the finish status code is registered with the output buffer inside the **PPMC-111** (OBF bit = "1").
The details of each bit of finish status code are as follows:

(1) Bit 0[**Stop by normal operation**]

Bit 0 indicates "1" upon termination of pulse output when the output of operation pulse number, which was designated at the issue of acceleration/deceleration operation command or constant speed operation command, has been fully completed.

(2) Bit 1[**Stop by stop command**]

Bit 1 indicates "1" upon termination of pulse output with the receipt of instantaneous stop command or decelerating stop command during pulse output.

(3) Bit 2[**Stop by detection of origin signal ($\overline{\text{ORG}}$)**]

Bit 2 indicates "1" upon termination of pulse output with the detection of the origin limit signal ($\overline{\text{ORG}}$) during origin search.

(4) Bit 3[**Stop by detection of high speed limit signal ($\overline{\text{BHL}}$) in CCW direction**]

Bit 3 indicates "1" upon termination of pulse output with the detection of the high speed limit signal ($\overline{\text{BHL}}$) in the CCW direction during pulse output for the CCW direction.

(5) Bit 4[**Stop by detection of high speed limit signal ($\overline{\text{FHL}}$) in CW direction**]

Bit 4 indicates "1" upon termination of pulse output with the detection of the high speed limit signal ($\overline{\text{FHL}}$) in the CW direction during pulse output for the CW direction.

(6) Bit 5[**Stop by detection of limit signal ($\overline{\text{BL}}$) in CCW direction**]

Bit 5 indicates "1" upon termination of pulse output with the detection of the limit signal ($\overline{\text{BL}}$) in the CCW direction during pulse output for the CCW direction.

(7) Bit 6[**Stop by detection of limit signal ($\overline{\text{FL}}$) in CW direction**]

Bit 6 indicates "1" upon termination of pulse output with the detection of the limit signal ($\overline{\text{FL}}$) in the CW direction during pulse output for the CW direction.

(8) Bit 7[**Stop by detection of alarm signal ($\overline{\text{ALM}}$)**]

Bit 7 indicates "1" upon termination of pulse output with the detection of the alarm signal ($\overline{\text{ALM}}$) during pulse output.

The issue of finish status read command clears the interrupt ($\overline{\text{INT}}$) signal output resulting from the termination of pulse output except in the case of concurrent interrupt by command error, in which case the interrupt ($\overline{\text{INT}}$) signal output shall not be eliminated. The "command error code read command" must be issued in order to clear the interrupt ($\overline{\text{INT}}$) signal output due to the occurrence of command error. Issuing the finish status read command changes bit 4 (INTS bit) of the status register to "0"; however, it does not affect bit 5 (INTE bit).
This command code must be written only after the status register's IBF and IST bits are checked. A finish status code must be read after the OBF bit is checked.
Fig. 3-42 is a flow chart indicating the flow of issue of finish status read command.

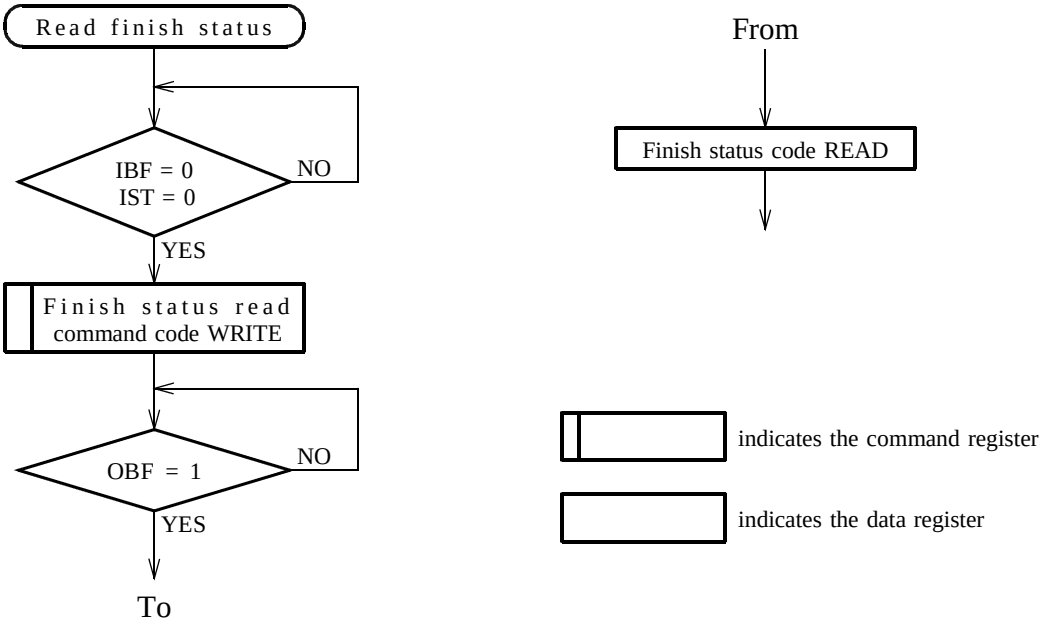


Fig. 3-42 (Flow chart of finish status read)

3 - 4 - 2 Command error code read command

This command enables reading of the cause of command error. This command can be used before, during or after pulse output.

This command, which carries a command code alone, reads out a 1-byte command error code upon writing of the command code.

This command code must be written only after the status register's IBF and IST bits are checked. A command error code must be read after the OBF bit is checked.

If a wrong command code or data is provided from the host processor to the **PPMC-111**, the **PPMC-111** delivers the interrupt signal ($\overline{\text{INT}}$), while bit 5 (INTE bit) and bit 7 (ERR bit) of the status register indicates "1".

Each command error code is overwritten (replaced) every time a command is received from the host processor. The command error code, therefore, reads "00h" once a correct command is provided after the occurrence of a command error. Likewise, bit 7 (ERR bit) of the status register is revised every time a command is received from the host processor. Bit 7, therefore, reads "0" once a correct command is provided after the occurrence of a command error.

The issue of the command error code read command clears the interrupt ($\overline{\text{INT}}$) signal output resulting from the occurrence of a command error except in the case of concurrent interrupt by termination of pulse output, in which case the interrupt ($\overline{\text{INT}}$) signal output shall not be eliminated. The finish status read command needs to be issued in order to clear the interrupt ($\overline{\text{INT}}$) signal output due to the termination of pulse output. Issuing the command error code read command changes bit 5 (INTE bit) of the status register to "0"; however, it does not affect bit 4 (INTS bit).

This command must be used carefully during pulse output because the **PPMC-111** is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to when the finish status code is registered with the output buffer inside the **PPMC-111** (OBF bit = "1").

<Command error code read command/code>

bit	7	6	5	4	3	2	1	0	
1	0	1	0	0	0	0	0	1	Command error code read command code

bit	7	6	5	4	3	2	1	0	
2									Command error code

Fig. 3-43

Fig. 3-44 is a flow chart indicating the flow of issue of command error code read command, and **Table 3-4** is a list of command error codes.

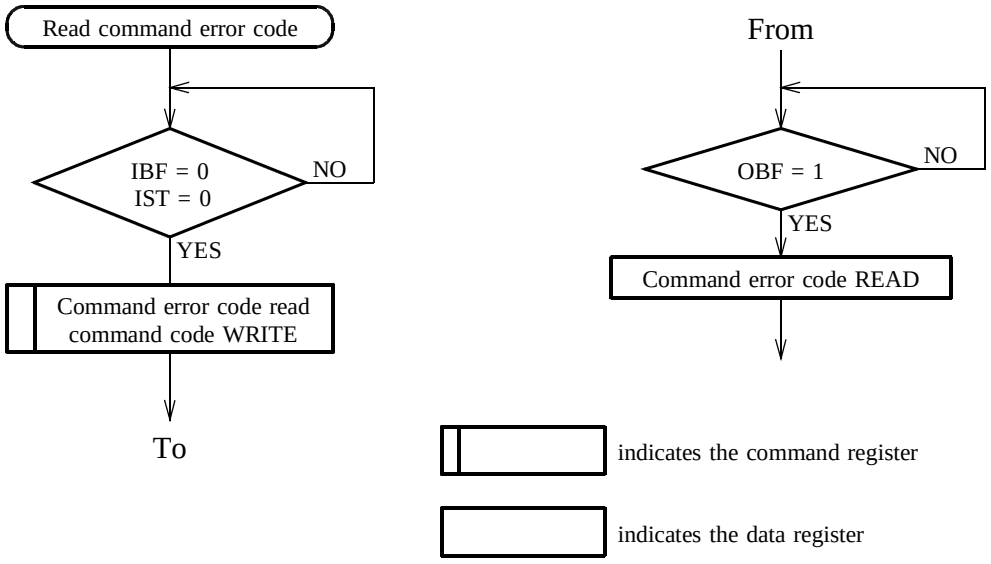


Fig. 3-44 (Flow chart of command error code read)

Table 3-4 (Command error codes)

Error Code		Descriptions of Error
Decimal	Hex. decimal	
0	0 0	No errors
1	0 1	Received command not defined.
2	0 2	No initialization command provided.
3	0 3	Not operable due to limit signal or alarm signal.
4	0 4	Not operable as operation pulse number "0" is designated.
5	0 5	Stop command received while at stop.
6	0 6	Received data not preceded by command.
7	0 7	Received command while waiting for data.
8	0 8	Not operable as origin search command is received while origin signal is already fed.
9	0 9	Received a command which is unprocessible in BUSY status.
10	0 A	Abnormal pulse rate of initialization command (>7FFFh or <000Fh).
11	0 B	Excessively small acceleration/deceleration pulse number at the time of initialization.
12	0 C	Abnormal pulse rate at the time of initialization (RH<RL).
13	0 D	Pulse rate designated at issue of operation command or speed change command is outside the range of pulse rate designated at the time of initialization (RH<RL).
14	0 E	Received speed change command while decelerating due to detection of high speed limit or receipt of decelerating stop command.
15	0 F	Received decelerating stop command while decelerating due to detection of high speed limit or receipt of decelerating stop command.
16	10	Received speed change command while at stop.
17	11	Abnormal acceleration/deceleration step number at the time of initialization (< 2 or > 96).
18	12	Abnormal acceleration/deceleration step pulse rate at the time of initialization [R (n) < R (n - 1)].
19	13	Abnormal acceleration/deceleration step pulse number at the time of initialization [S(n) $\leq$ 1].

3 - 4 - 3 Current position read command

This command is used to obtain the reading (value) of the current position counter inside the **PPMC-111**. This command can be used before, during or after pulse output. This command, which carries a command code alone, reads out a 24-bit datum on the current position upon writing of the command code.

This command code must be written only after the status register's IBF and IST bits are checked. The 24-bit current position data must be read, one byte at a time, in the correct order starting with the lower byte, then the middle byte and finally the upper byte, while checking the OBF bit.

This command must be used carefully during pulse output because the **PPMC-111** is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to when the third byte (i.e., upper byte) of the current position data is registered with the output buffer inside the **PPMC-111** (OBF bit = "1").

<**Current position read command code/data**>

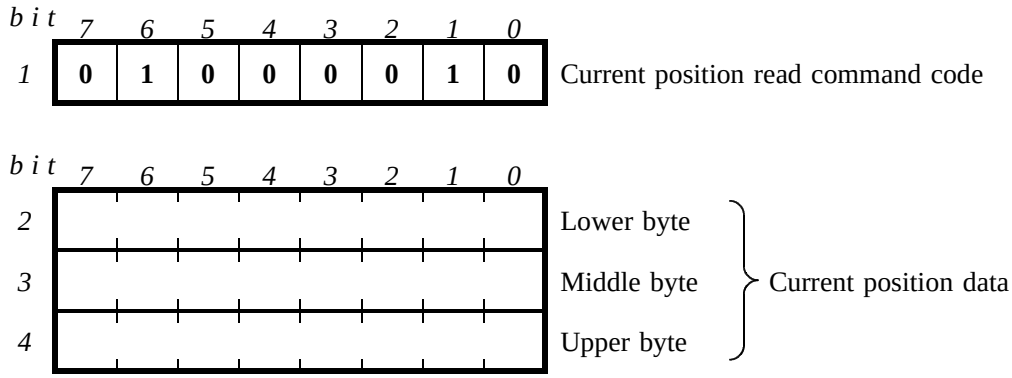


Fig. 3-45

The current position counter of the **PPMC-111** is a 24-bit UP/DOWN counter with the starting value of "000000h." The value of this counter increments when there is an output of pulse in the CW direction and decrements with an output of pulse in the CCW direction. If the reading of the current position counter overflows (i.e., "FFFFFFh"), it first returns to "000000h" then continues to increment. The data on this current position counter, which is revised every time there is an output of operation pulse, enables current position control by means of absolute position. **Table 3-5** shows the correlation between the direction of pulse output and increment/decrement in counter reading.

Table 3-5 (Correlation between the direction of pulse output and increment/decrement in counter reading)

Reading of current position counter	Correlation between the direction of pulse output and increment/decrement in counter reading
F F F F F F h	In case of output of pulse in CCW direction
F F F F F E h	↓
F F F F F D h	
:	
0 0 0 0 0 2 h	
0 0 0 0 0 1 h	
0 0 0 0 0 0 h	Counter reads "000000h" after resetting
F F F F F F h	
F F F F F E h	
:	
0 0 0 0 0 2 h	
0 0 0 0 0 1 h	↑
0 0 0 0 0 0 h	In case of output of pulse in CW direction

When the origin signal ($\overline{ORG}$) is detected during Constant Speed Origin Search Operation, if SEL_TYP terminal is made Open or High, the value of the current position counter inside PPMC-111 will be cleared to "000000h", and if the terminal is made Low the counter won't be cleared.
Fig. 3-46 is a flow chart indicating the flow of issue of the position read command.

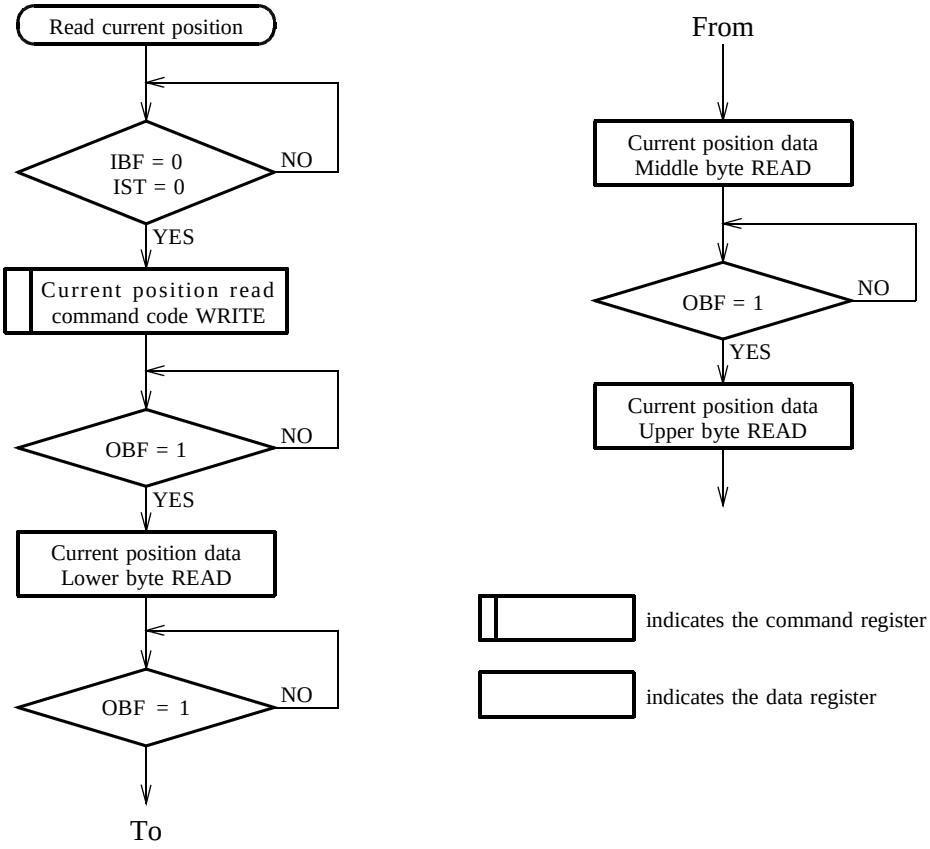


Fig. 3-46 (Flow chart of current position read command)

3 - 4 - 4 Auxiliary input signal status code read command

This command is used to read the conditions of auxiliary input signals AUXI0 through AUXI7. There is a delay of approximately 40microsecond in reading an auxiliary input signal status code. This command, which carries a command code alone, reads out a 1-byte auxiliary input signal status code upon writing of the command code.

This command code must be written only after the status register's IBF and IST bits are checked. The auxiliary input signal status code data must be read while checking the OBF bit. This command can be used before, during or after pulse output

<**Auxiliary input signal status code read command/code**>

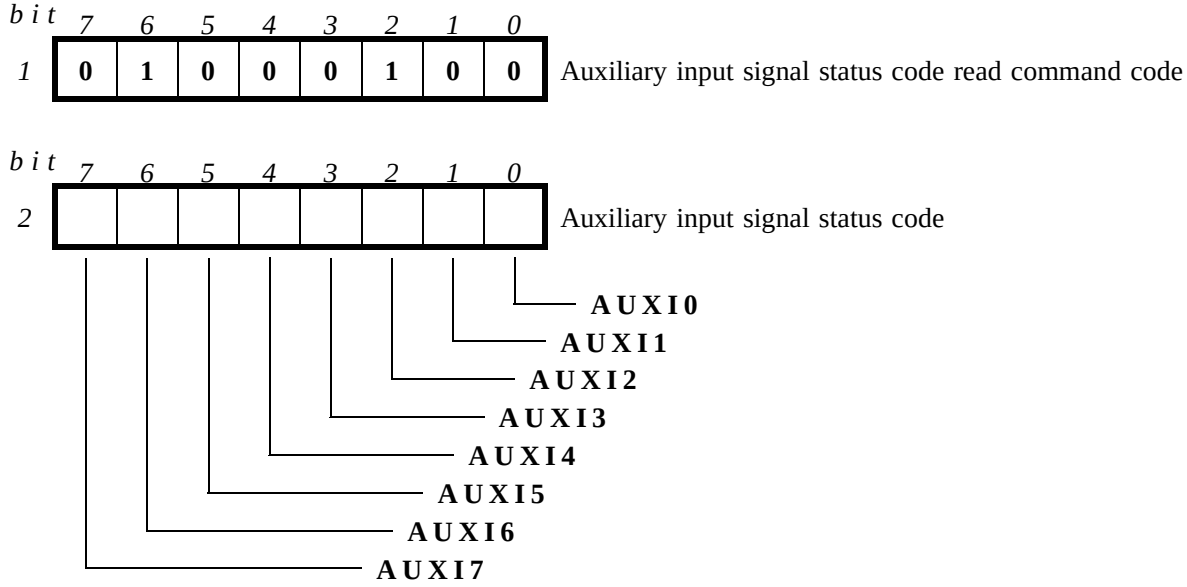


Fig. 3-47

This command must be used carefully during pulse output because the **PPMC-111** is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to when the auxiliary input signal status data is registered with the output buffer inside the **PPMC-111** (OBF bit = "1").

Fig. 3-48 is a flow chart indicating the flow of issue of the auxiliary input signal status code read command.

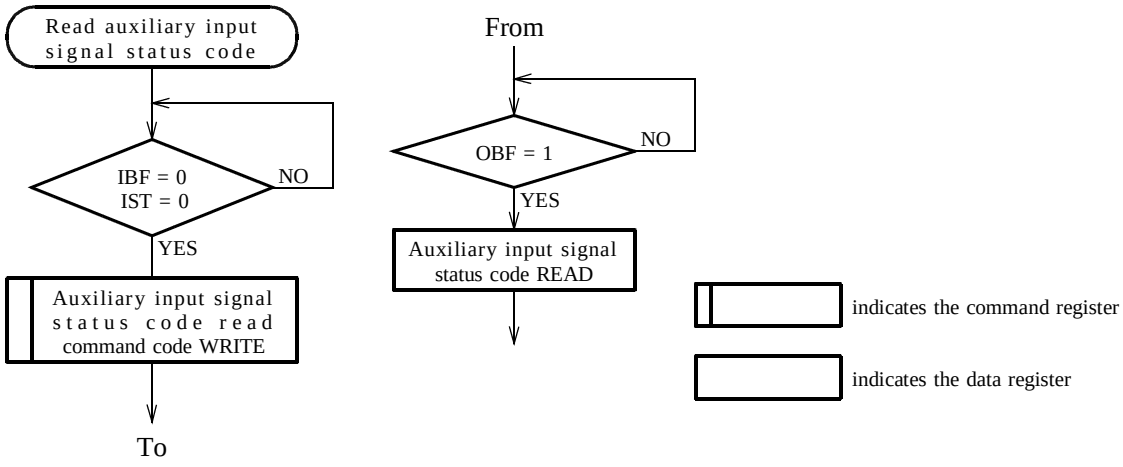


Fig. 3-48 (Flow chart of auxiliary input signal status code read)

3 - 4 - 5 Control input signal status code read command

This command is used to read the conditions of various input signals of the **PPMC-111**, including limit input signals, origin signals, alarm signals and RUN signals. This command reads the condition of each input terminal at the time of this command. Therefore, bits 2 and 0 do not indicate "0" in the case of a decelerating stop at the high speed limit since it has passed the point of detection of high speed limit. In terms of reading of each bit, "0" indicates that there is an input signal, while "1" indicates absence of input signals. This command, which carries a command code alone, reads out a 1-byte control input signal status code upon writing the command code.

This command code must be written only after the status register's IBF and IST bits are checked. The control input signal status code must be read while checking and confirming the OBF bit.

<**Control input signal status code read command/code**>

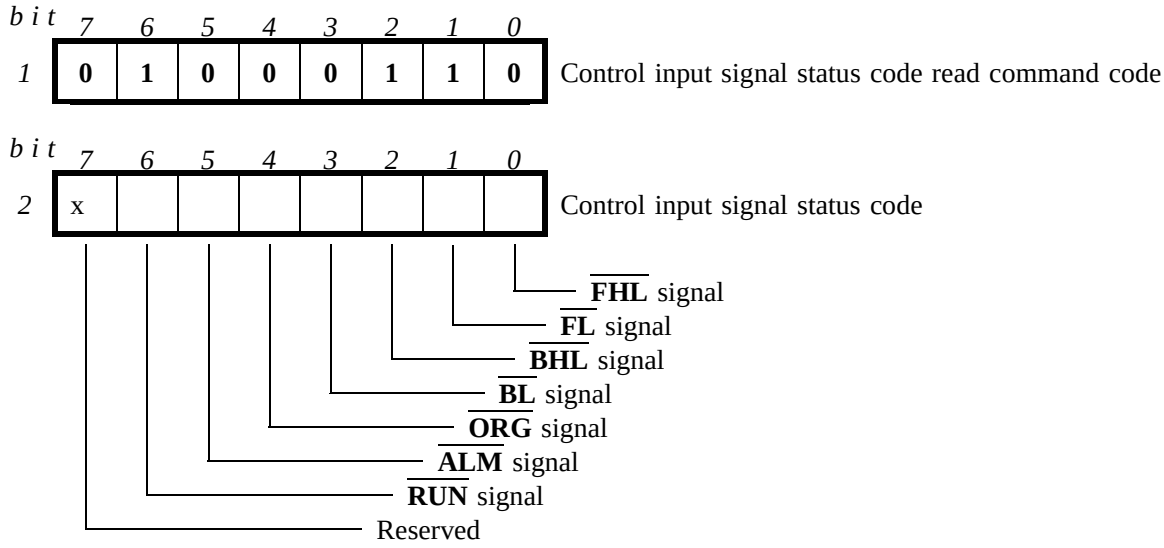


Fig. 3-49

This command must be used carefully during pulse output because the **PPMC-111** is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to when the control input signal status data is registered with the output buffer inside the **PPMC-111** (OBF bit = "1").

Fig. 3-50 is a flow chart indicating the flow of issue of the control input signal status code read command.

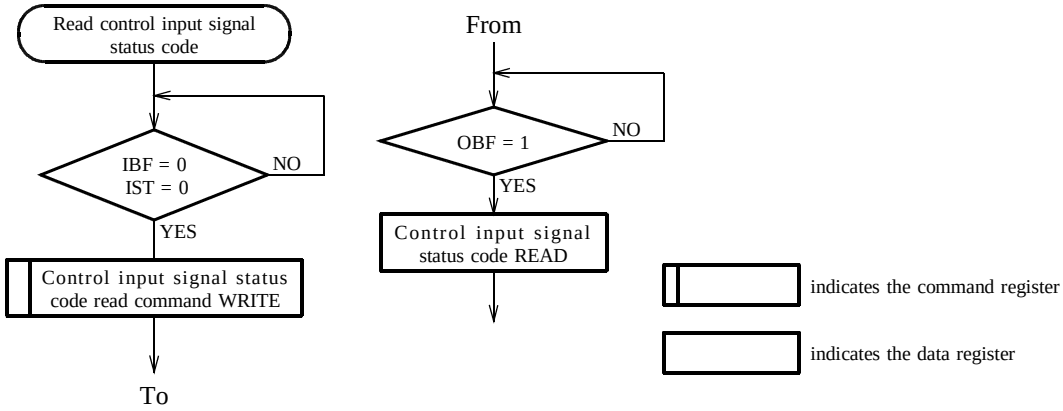


Fig. 3-50 (Flow chart of control input signal status code read)

3 - 5 Auxiliary commands

These commands are used for current position setting, auxiliary output port output and high speed limit effective speed setting (i.e., setting effective speed for high speed limit). There are three (3) commands as shown in **Fig. 3-51**. The auxiliary output command can be used before, during or after pulse output, while the current position setting command and high speed limit effective speed setting command can be used only when there is no pulse output.

<Auxiliary command>

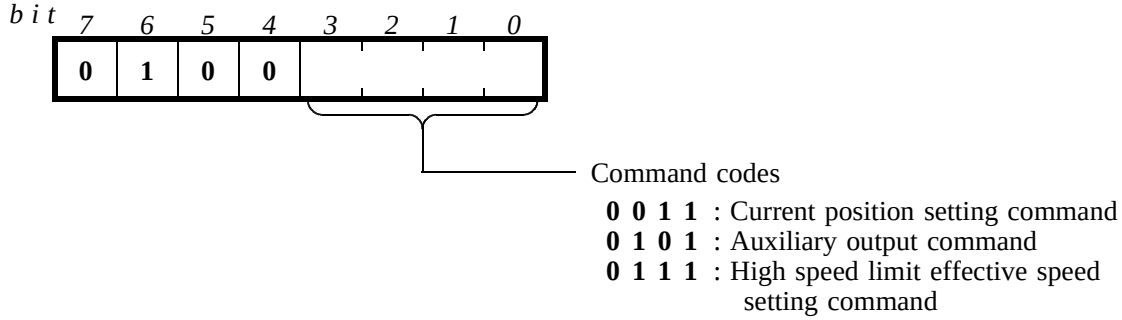


Fig. 3-51 (Auxiliary command bit configuration)

3 - 5 - 1 Current position setting command

This command is used to set the current position of the motor. This command can be used only when there is no pulse output. The reading shows "0" after resetting.

This command code must be written only after the status register's IBF, IST and BUSY bits are checked. 3-byte data on the current position setting must be written in the correct order starting with the lower byte, while checking the IBF bit.

<Current position setting command/data>

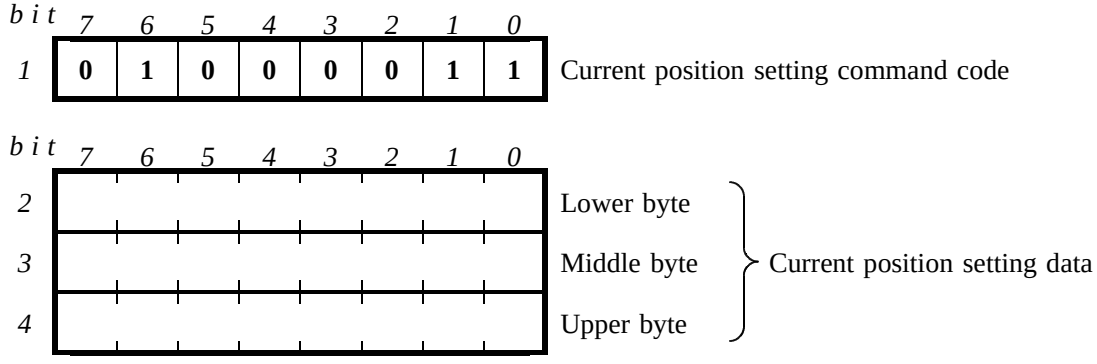


Fig. 3-52

Fig. 3-53 is a flow chart indicating the flow of issue of the current position setting command.

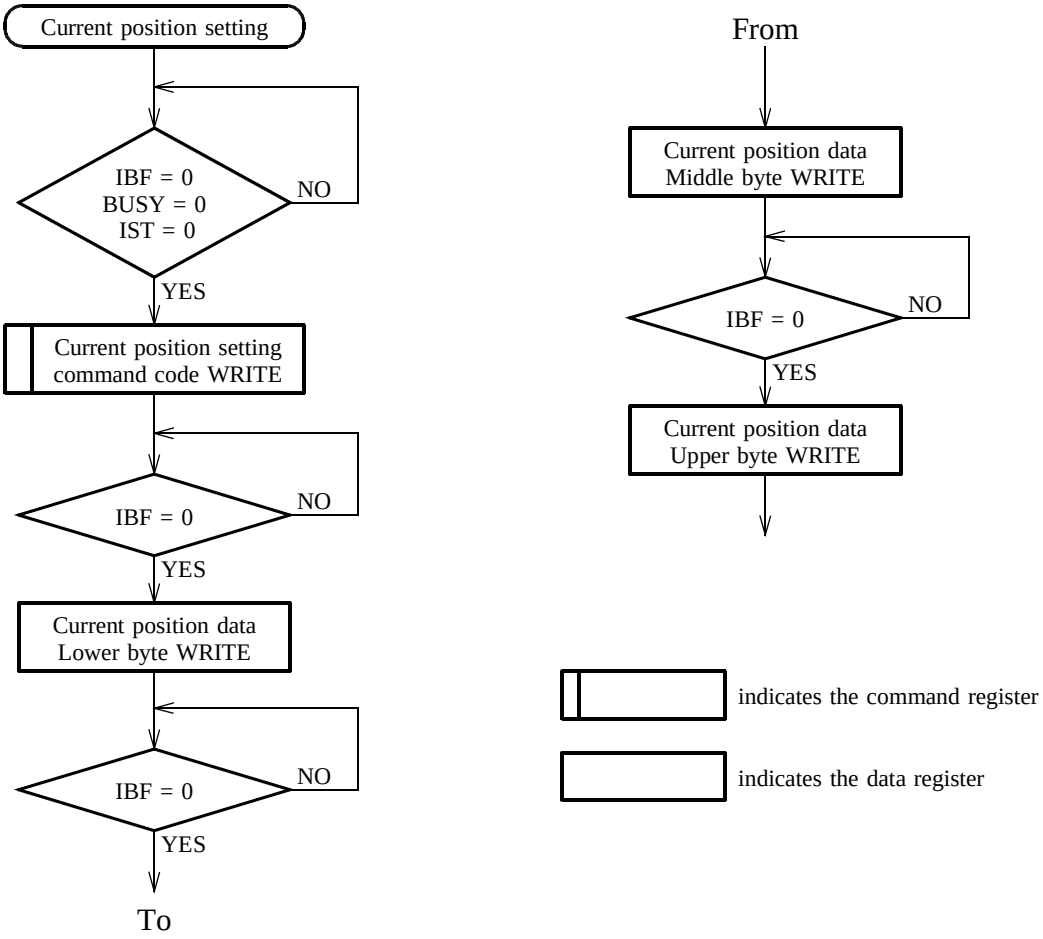


Fig. 3-53 (Flow chart of current position setting command)

3 - 5 - 2 Auxiliary output command

This command is used to set the conditions of signal output via auxiliary output terminals AUXO0 through AUXO7. There is a delay of approximately 40microsecond between the receipt of this command for auxiliary output and the actual change of conditions at the output terminal. The auxiliary output signal shifts to the "H" level after resetting. This command is effective even during pulse output by the **PPMC-111**.

This command code must be written only after the status register's IBF and IST bits are checked. The auxiliary output data must be written while checking the IBF bit.

<**Auxiliary output command/data**>

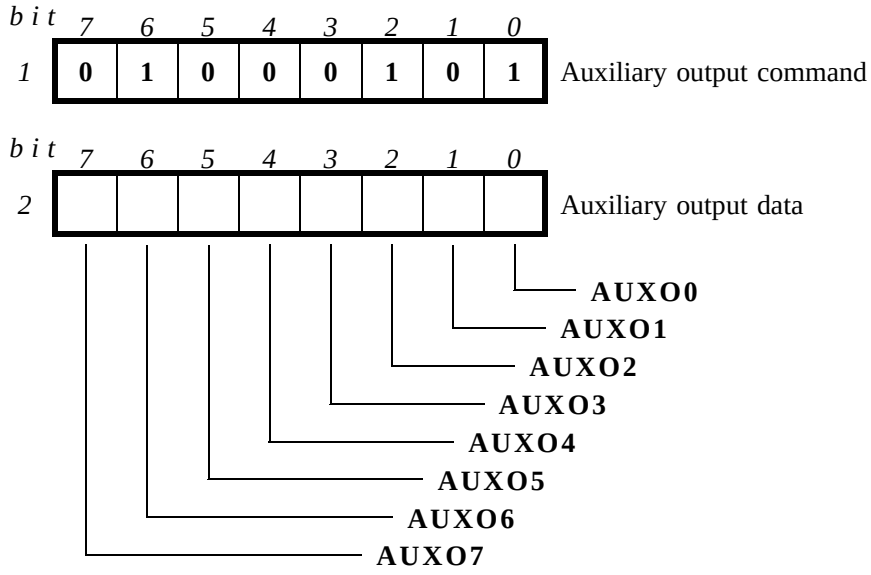


Fig. 3-54

This command must be used carefully during pulse output because the **PPMC-111** is unable to detect any control input signal, including a limit signal, from the start of receipt of this command code (IST bit = "1") to the output of an auxiliary input signal (IST bit = "1").

Fig. 3-55 is a flow chart indicating the flow of issue of the auxiliary output command.

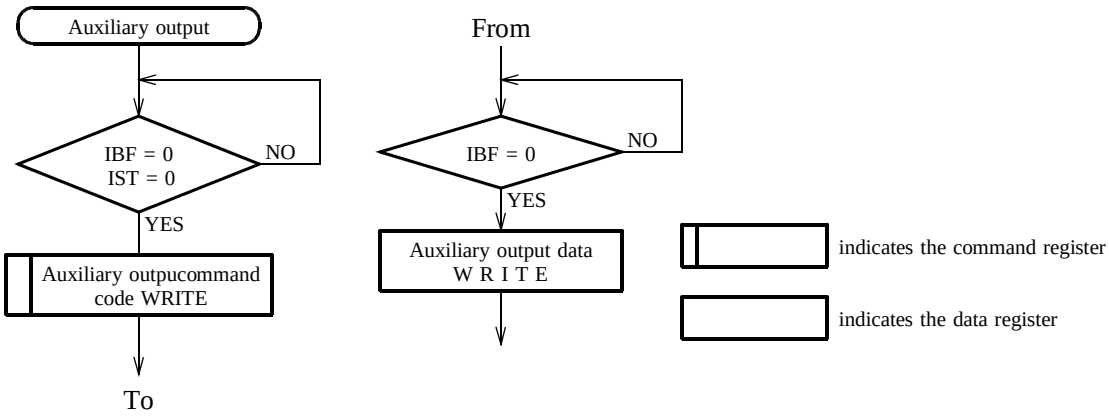


Fig. 3-55 (Flow chart of auxiliary output command)

3 - 5 - 3 High speed limit effective speed setting command

This command is used to set a range of speed which allows high speed limit signals ($\overline{\text{BHL}}$ and $\overline{\text{FHL}}$) of the **PPMC-111** effective. This command can be used only when there is no pulse output. It is necessary to set a 16-bit effective speed pulse rate after the command code.

This command code must be written only after the status register's IBF, IST and BUSY bits are checked. 16-bit data on the pulse rate must be written in the correct order starting with the lower byte and then the upper byte, while checking the IBF bit.

The default value of the high speed limit effective speed is equivalent to the value of pulse rate at high speed established at the time of initialization.

Detection of a high speed limit signal corresponding to the direction of rotation during pulse output at any speed equivalent to or exceeding the speed set by this command leads to decelerating stop even during pulse output by any command. Contrarily, if a high speed limit signal corresponding to the direction of rotation is detected during pulse output at any speed lower than the speed set by this command, the high speed limit signal shall be disregarded and the designated pulse output shall be continued even during pulse output by any command except when pulse output is performed by the continuous high speed operation command (command for high speed operation up to the high speed limit). Detection of a high speed limit signal during pulse output by the continuous high speed operation command leads to an unconditional decelerating stop, regardless of the default value or the setting by the high speed limit effective speed setting command.

If the **PPMC-111** engages in pulse output by either of the three (3) commands for constant speed operation, continuous constant speed operation or constant speed origin search, it continues the designated pulse output without making a decelerating stop even if a high speed limit signal ($\overline{\text{BHL}}$ or $\overline{\text{FHL}}$) is detected. Rotation of the stepper motor by any of these three (3) operation commands implies a rotation speed not exceeding the self-starting frequency of the stepper motor used; therefore, there is only a rare occurrence of dislocation due to becoming out of step when the rotation of the stepper motor comes to a stop. If, however, the instantaneous speed change command or accelerating/decelerating speed change command is received when the stepper motor is rotating by one of the aforementioned constant speed operation commands, the stepper motor may continue to rotate at a speed equivalent to or exceeding its self-starting frequency until it reaches the point where the instantaneous speed change signal ($\overline{\text{BL}}$ or $\overline{\text{FL}}$) is set. Pulse output comes to an immediate stop if the **PPMC-111** detects a limit signal ($\overline{\text{BL}}$ or $\overline{\text{FL}}$), in which case the out-of-step condition of the stepper motor may cause dislocation.

This high speed limit effective speed setting command is provided to prevent such dislocation due to the stepper motor being out of step.

Position setting control is usually started after setting, following the initialization command, the effective speed for the high speed limit at a speed equivalent to or exceeding the self-starting frequency, taking into consideration various physical elements, such as the inertial load.

Figures 3-56 and **3-57** show examples of operations while setting an effective speed for the high speed limit using this command.

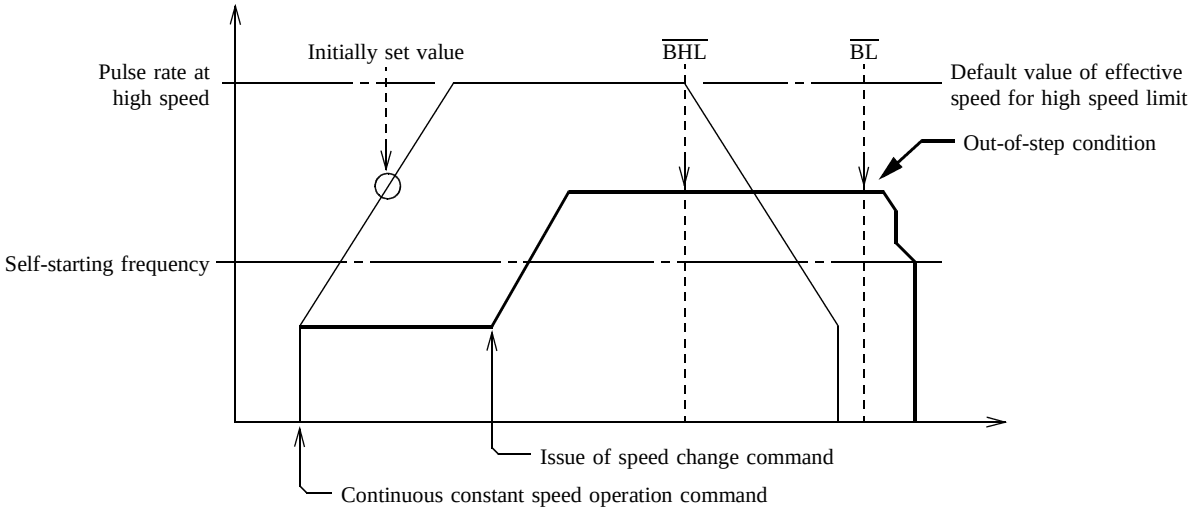


Fig. 3-56 (When effective speed for high speed limit is not set)

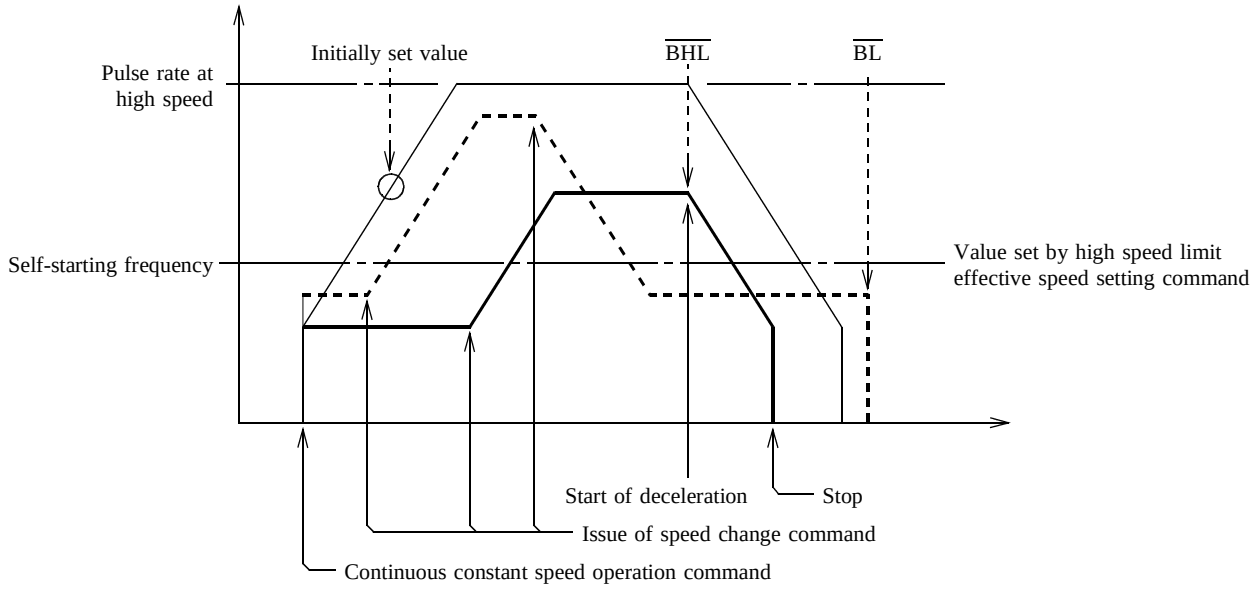


Fig. 3-57 (When parameters for setting effective speed for high speed limit are set without exceeding self-starting frequency)

<High speed limit effective speed setting command/data>

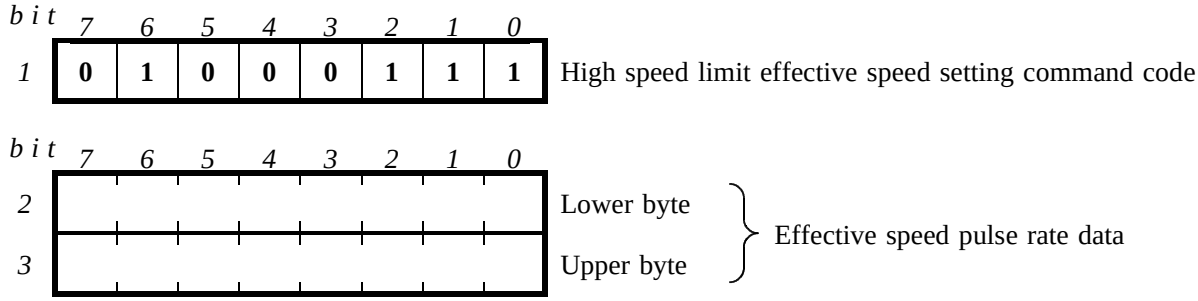


Fig. 3-58

The high speed limit signal $\overline{\text{FHL}}$ is effective during CW pulse output, while the $\overline{\text{BHL}}$ signal is effective during CCW pulse output. The mode of stop upon detection of a high speed limit signal varies as detailed in **Table 3-6**, depending on three (3) conditions: namely, (1) operation command, (2) value of pulse rate set for effective speed for the high speed limit, and (3) pulse output speed at the time of detection of the high speed limit signal.

Table 3-6 (Mode of stop upon detection of high speed limit)

Type of operation command	Pulse output speed at detection of high speed limit				When operation command is received while high speed limit signal is already received
	< High speed limit effective speed		≥ High speed limit effective speed		
	> Starting speed	= Starting speed	> Starting speed	= Starting speed	
Acceleration/deceleration operation command	Continuous designated pulse output operation		Decelerating stop	Emergency stop	No pulse output
Constant speed operation command					
Continuous constant speed operation command					
Constant speed origin search command					
Continuous high speed operation command	Decelerating stop	Emergency stop			
Single step command	Desregards if detected after pulse output				

If a high speed limit effective speed pulse rate is not set using the high speed limit effective speed setting command after the **PPMC-111** (i.e., default status) is reset, the value of pulse rate at high speed established at the time of initialization shall be used as the high speed limit effective speed pulse rate.

Fig. 3-59 is a flow chart indicating the flow of issue of the high speed limit effective speed setting command.

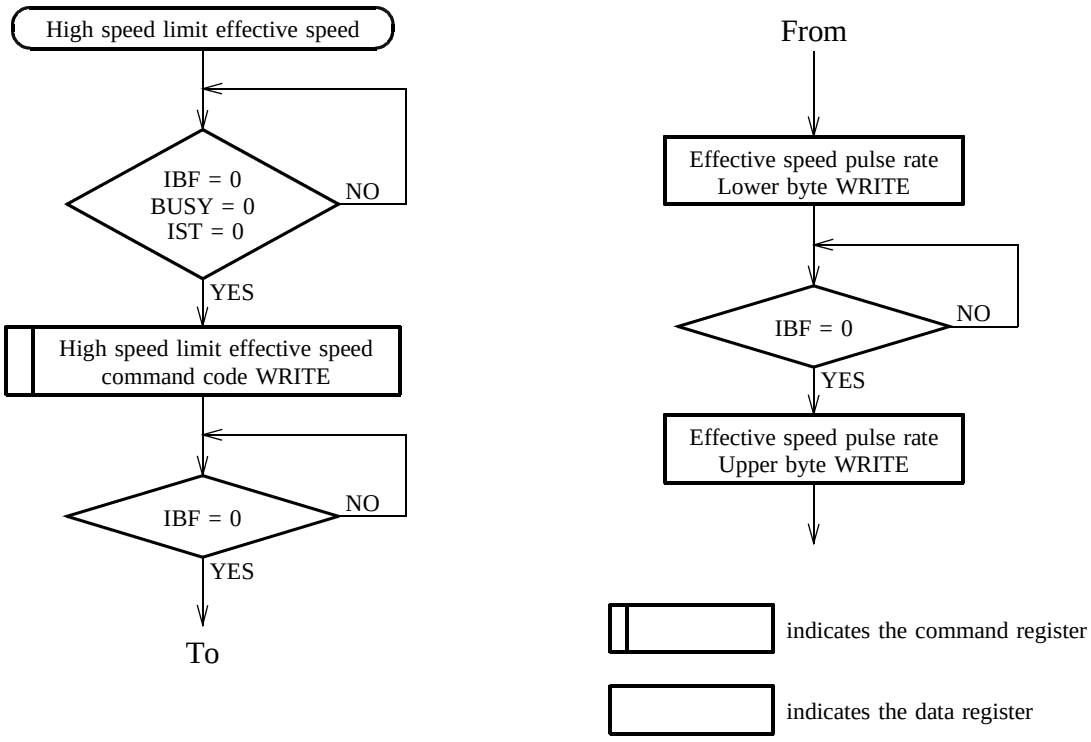


Fig. 3-59 (Flow chart of high speed limit effective speed setting)