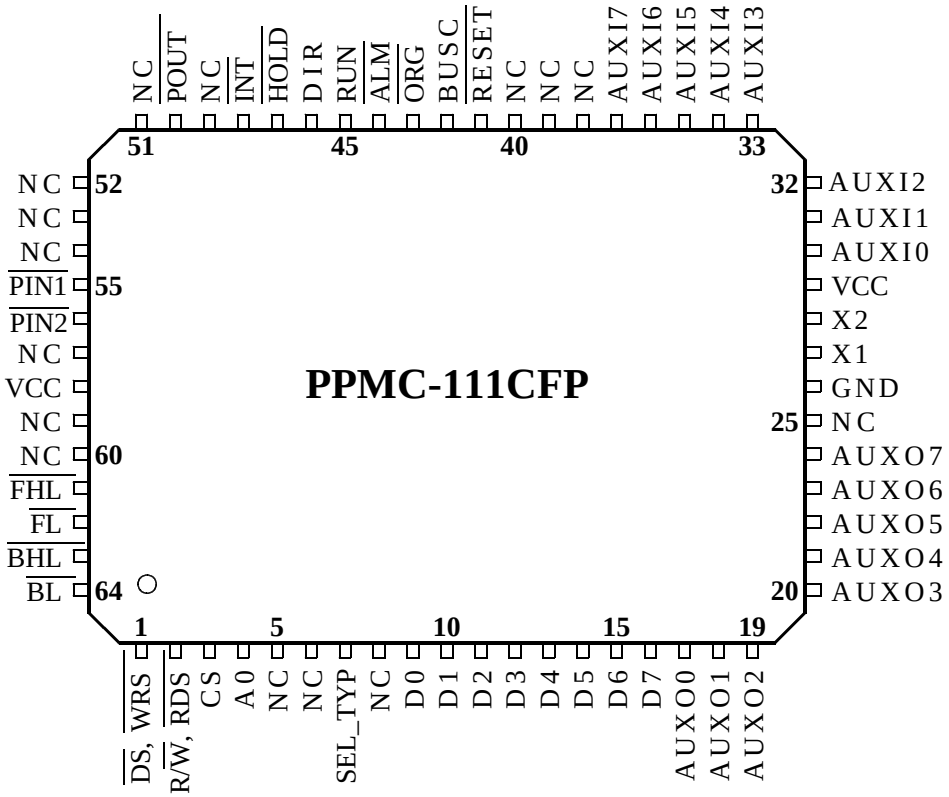
2. TERMINAL ASSIGNMENT

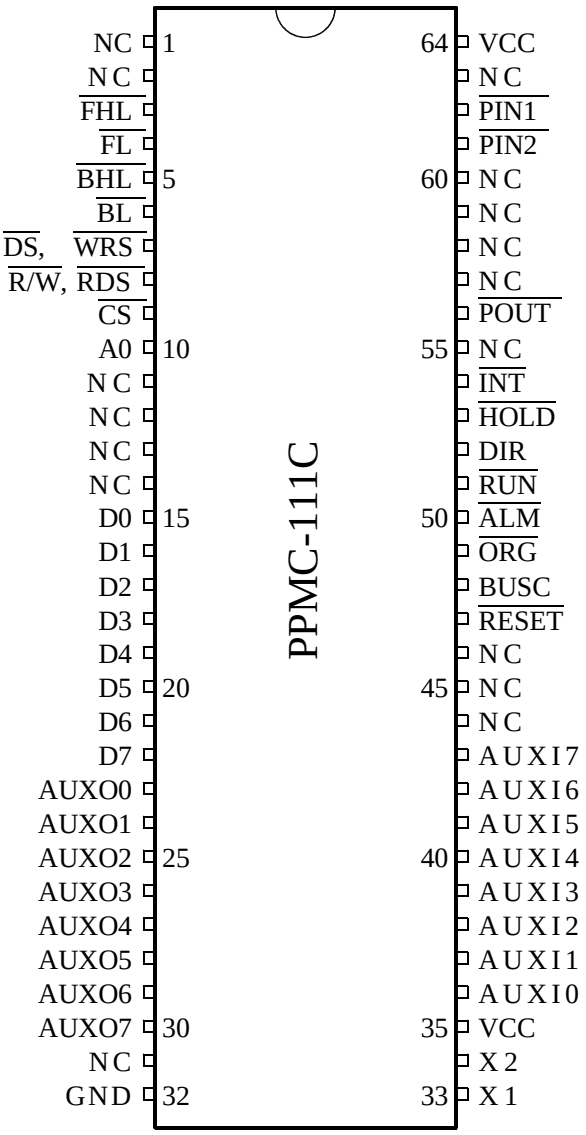
There are two types of **PPMC-111**, each having a different shape. One is "**PPMC-111CFP**" with a 64-pin QFP package and the other is "**PPMC-111C**" with a 64-pin shrink DIP package. **Fig. 2-1** and **Fig. 2-3** show the terminal assignments of I/O signals of the QFP type and the SDIP type, respectively. **Table 2-1** is the terminal - signal table.

This chapter provides a detailed description of these signals.



(Top View)

Fig. 2-1 (Terminal Assignment of PPMC-111CFP)



(Top View)

Fig. 2-2 (Terminal Assignment of PPMC-111C)

2. TERMINAL ASSIGNMENT

Table 2-1 (Terminal - Signal Table)

Terminal Number		Signal	I/O	Description
PPMC 111CFP	PPMC 111C			
1	7	$\overline{DS}$,$\overline{WRS}$	I	Data strobe, Write strobe
2	8	R/$\overline{W}$,$\overline{RDS}$	I	Read/Write, Read strobe
3	9	$\overline{CS}$	I	Chip select input
4	10	$\overline{A_0}$	I	Address 0
5	11	NC	-	
6	12	NC	-	
7	13	SEL_TYP	I	It'll clear the value of the current position counter inside PPMC-111
8	14	NC	-	
9	15	D_0	I / O	Data bus bit 0
10	16	D_1	I / O	Data bus bit 1
11	17	D_2	I / O	Data bus bit 2
12	18	D_3	I / O	Data bus bit 3
13	19	D_4	I / O	Data bus bit 4
14	20	D_5	I / O	Data bus bit 5
15	21	D_6	I / O	Data bus bit 6
16	22	D_7	I / O	Data bus bit 7
17	23	AUXO 0	O	Auxiliary output bit 0
18	24	AUXO 1	O	Auxiliary output bit 1
19	25	AUXO 2	O	Auxiliary output bit 2
20	26	AUXO 3	O	Auxiliary output bit 3
21	27	AUXO 4	O	Auxiliary output bit 4
22	28	AUXO 5	O	Auxiliary output bit 5
23	29	AUXO 6	O	Auxiliary output bit 6
24	30	AUXO 7	O	Auxiliary output bit 7
25	31	NC	-	
26	32	GND	I	Connect to GND
27	33	X_1	I	Crystal oscillator terminal 1
28	34	X_2	I	Crystal oscillator terminal 2
29	35	V_{CC}	I	5V power input
30	36	AUXI 0	I	Auxiliary input bit 0
31	37	AUXI 1	I	Auxiliary input bit 1
32	38	AUXI 2	I	Auxiliary input bit 2
33	39	AUXI 3	I	Auxiliary input bit 3
34	40	AUXI 4	I	Auxiliary input bit 4
35	41	AUXI 5	I	Auxiliary input bit 5
36	42	AUXI 6	I	Auxiliary input bit 6

Terminal Number		Signal	I/O	Description
PPMC 111CFP	PPMC 111C			
37	43	AUXI 7	I	Auxiliary input bit 7
38	44	NC	-	
39	45	NC	-	
40	46	NC	-	
41	47	$\overline{\text{RESET}}$	I	Reset input
42	48	BUSC	I	Slave bus interface select
43	49	$\overline{\text{ORG}}$	I	Origin (base point)
44	50	$\overline{\text{ALM}}$	I	Alarm signal
45	51	$\overline{\text{RUN}}$	I	Pulse output start signal
46	52	DIR	O	Rotation direction output
47	53	$\overline{\text{HOLD}}$	O	Motor hold signal
48	54	$\overline{\text{INT}}$	O	Interrupt signal
49	55	NC	-	
50	56	$\overline{\text{POUT}}$	O	Pulse output
51	57	NC	-	
52	58	NC	-	
53	59	NC	-	
54	60	NC	-	
55	61	$\overline{\text{PIN1}}$	I	Pulse count input terminal 1, Connect to $\overline{\text{POUT}}$.
56	62	$\overline{\text{PIN2}}$	I	Pulse count input terminal 2, Connect to $\overline{\text{POUT}}$.
57	63	NC	-	
58	64	VCC	I	5V power input
59	1	NC	-	
60	2	NC	-	
61	3	$\overline{\text{FHL}}$	I	CW direction high-speed limit input
62	4	$\overline{\text{FL}}$	I	CW direction limit input
63	5	$\overline{\text{BHL}}$	I	CCW direction high-speed limit input
64	6	$\overline{\text{BL}}$	I	CCW direction limit input

$\overline{\quad}$ in the table indicates negative logic.

O = Output

I = Input

NC = Open

The input terminal, which is not in use, pull up to VCC with 10kohm or pull down to GND.

2-1 Signal description of system hardware

2-1-1 $\overline{\text{RESET}}$ (Reset)

Signal used to reset **PPMC-111** to initial state. This terminal should be connected to the RESET signal of a user's system.
After the rise from a low level, the initialization and operation command from the host processor is put into operation. The RESET signal must be such that the "L" level is retained for at least 2microsecond after the oscillation of the internal oscillator has stabilized with the power supply voltage being within the operation range of **PPMC-111**.

2-1-2 X_1, X_2 (Crystal oscillator)

The X_1 and X_2 terminals input system clock to **PPMC-111**. Normally a 16MHz crystal oscillator is connected as shown in the diagram on the left in **Fig. 2-3**. 2-phase external clock can also be connected as shown in the diagram on the right in **Fig. 2-3**.
X_1 and X_2 can accept clock input frequencies of 1 to 16MHz, and the operating speed of **PPMC-111** is in proportion to the clock. From this point forward, all times in this description are based on this reference clock speed. Unless mentioned otherwise, the times, speeds and data are based on the reference clock speed of 16MHz.
When two or more **PPMC-111**s are to be operated from a single system clock driver, design the circuit as shown in **Fig. 2-4**. Also, observe the **NOTES on page 2-6**.

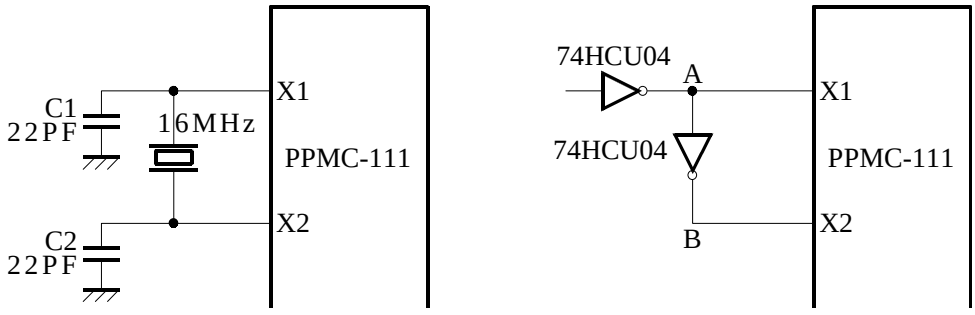


Fig. 2-3

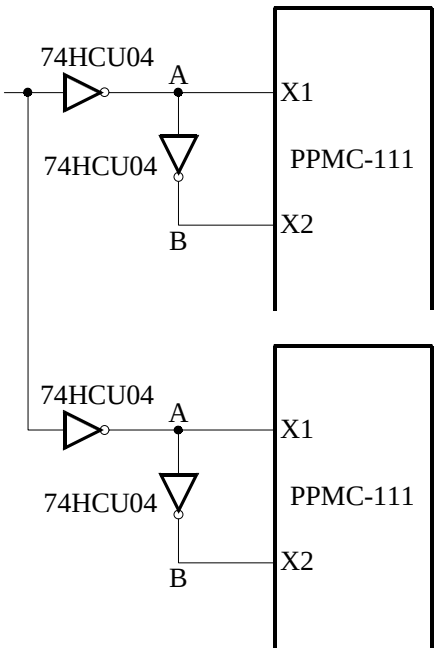


Fig. 2-4

NOTES:

(1) Crystal oscillator

The oscillation frequency of the crystal oscillator is determined by the load capacitance of the crystal oscillator and the external capacitances C1 and C2. However, the equivalent resistance of the crystal and external capacitances must be correct if oscillation is to be started and continued normally.
Table 2-2 below shows the recommended values.

Table 2-2 (Oscillation Frequency and Equivalent Series Resistance)

Frequency	Equivalent Series Resistance (Max.)	Frequency	Equivalent Series Resistance (Max.)
1MHz	600ohm	12MHz	35ohm
4MHz	100ohm	16MHz	35ohm
10MHz	35ohm		

(2) 2-phase external clock signal input system

When a 2-phase external clock signal driver as shown in **Fig. 2-3** (diagram on right) and **Fig. 2-4** is used, the following conditions must be satisfied by the circuit at points **A** and **B**:

Condition 1 : Duty ratio at **A** -50% to +50% (@ Vcc/2)
Condition 2 : CL at **A** and **B** 50pF (max.)

2-2 Host interface signals

The host interface signals are the signals that connect **PPMC-111** to the bus of the host processor. They are either signals to access the registers of **PPMC-111** or interrupt signals.

2-2-1 $\overline{CS}$ (Chip select)

The chip select signal for **PPMC-111** connects the signal decoding the upper bits of an address signal. **PPMC-111** is accessible when $\overline{CS}$ is low. (Refer to **3-1** "**Host interface registers**.")

2-2-2 A_0 (Register select)

This is the signal to switch to a pertinent register when read or write is done with the register of **PPMC-111** from the host processor. Normally it connects the LSB of an address signal. (Refer to **3-1** "**Host interface registers**.")

2-2-3 D_7 - D_0 (Data bus)

These are bidirectional 8-bit buses for data exchange between host processor and **PPMC-111**.

2-2-4 BUSC (Slave bus interface select)

This signal selects the mode of interface between post processor and **PPMC-111**. This signal allows easy connection of either of the R/$\overline{W}$ type CPU or the $\overline{RD}$ and $\overline{WR}$ separate type CPU. For the relationship between the BUSC signal and interface mode, refer to **2-2-5**, **2-2-6** and **Table 2-3**.

Table 2-3 (Relationship between BUSC Signal and Host Processor Bus I/F)

BUSC signal	Host processor bus I/F	Control signal used	
H	R/$\overline{W}$ type	Data strobe signal ($\overline{DS}$ signal)	Read/Write signal (R/$\overline{W}$ signal)
L	$\overline{RD}$, $\overline{WR}$ separate type	Write strobe signal ($\overline{WRS}$ signal)	Read Strobe signal ($\overline{RDS}$ signal)

2-2-5 $\overline{DS}$, $\overline{WRS}$ (Data strobe, Write strobe)

This signal is used as the Data Strobe signal for the R/$\overline{W}$ type CPU when the BUSC signal is high, and as the Write Strobe signal for the $\overline{RD}$, $\overline{WR}$ separate type CPU when the BUSC signal is low. Refer to **Table 2-3**.

2-2-6 R/$\overline{W}$, $\overline{RDS}$ (Read/Write, Read strobe)

This signal is used as the Read/Write signal for the R/$\overline{W}$ type CPU when the BUSC signal is high, and as the Read Strobe signal for the $\overline{RD}$, $\overline{WR}$ separate type CPU when the BUSC signal is low. Refer to **Table 2-3**.

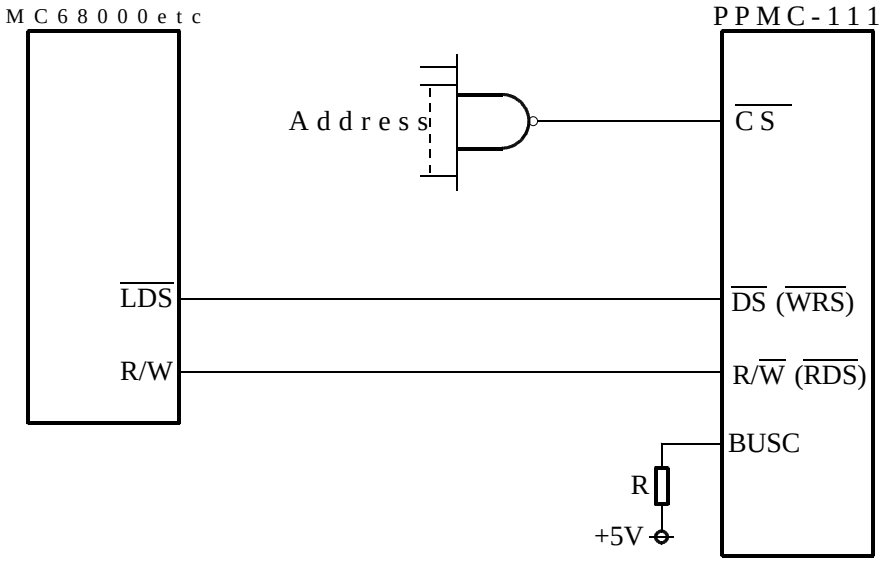


Fig. 2-5 Sample Connection of R/W Type Signal

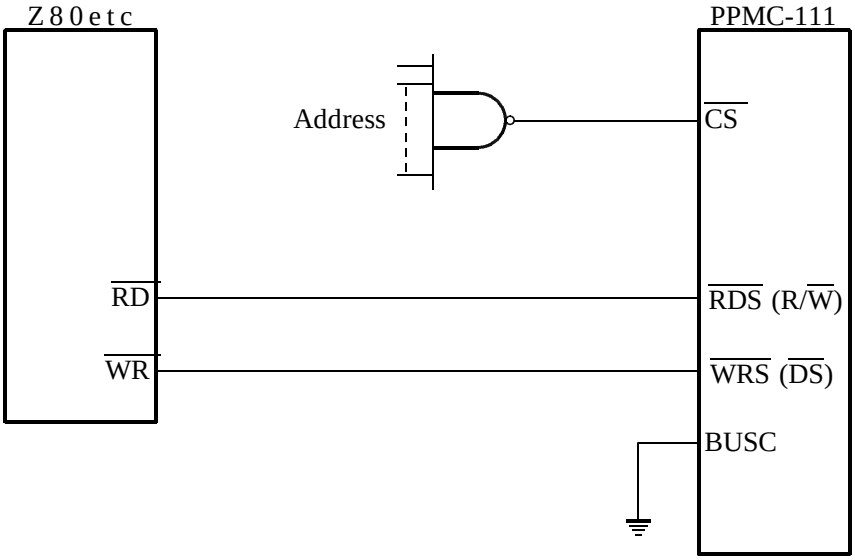


Fig. 2-6 Sample Connection of RD, WR Separate Type Signal

2-2-7 INT (Interrupt signal)

The Interrupt signal for the host processor is delivered in the following cases:

(1) The command code or parameter that **PPMC-111** has received from the host processor is incorrect.
(2) Termination interrupt control of the command code to **PPMC-111** is authorized and the pulse output of **PPMC-111** has finished.

The INT signal, which is normally high, goes low when either above condition (1) or (2) is met. The INT signal terminal is not an open collector. To connect a multiple interruption, therefore, provide an open collector buffer as shown in **Fig. 2-7**.

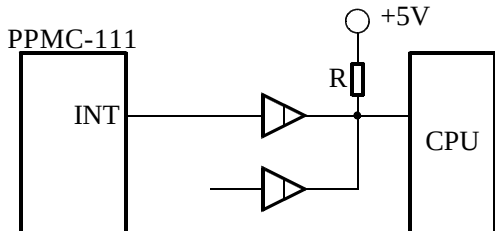


Fig. 2-7 Sample Connection of PPMC-111 Interrupt Output Signal

When a command error interrupt has occurred, the INT signal can be cleared by issuing a Command Error Code Read command. At this, the signal goes from low to high. Also, when a pulse output termination interrupt has occurred, the INT signal can be cleared by issuing a Finish Status Read command, with the signal going from low to high.
Hence, issuing a Finish Status Read command at a command error interrupt or issuing a Command Error Code Read command at a pulse output termination interrupt will not clear the INT signal. To clear the INT signal, therefore, it is necessary to issue a Status Read command corresponding to the cause of an interrupt by checking bit 4 (pulse output termination interrupt status) and bit 5 (command error interrupt status)of the status register.

2 - 2 - 8 $\overline{\text{RUN}}$ (Pulse output start signal)

This signal is checked before a pulse output with an operation command given by the host processor to **PPMC-111**. If the signal is high, pulse output will start. If it is low, there will be a wait until the signal goes high. During this time, **PPMC-111** accepts no other commands.

For instance, this signal is used to start operation of two or more **PPMC-111**s simultaneously. When you do not use the function of the $\overline{\text{RUN}}$ signal, be sure to pull up the voltage to +5V.

2 - 3 Motor control signals

The motor control signals are connected to a motor driver or like device.

2 - 3 - 1 DIR (Rotation direction signal)

The DIR signal, which specifies the direction of rotation, goes low when delivering a pulse for CW rotation and goes high when delivering a pulse for CCW rotation. This signal is used together with the $\overline{\text{POUT}}$ signal of **2-3-2**.

2 - 3 - 2 $\overline{\text{POUT}}$ (Pulse train output signal)

This is the pulse train signal delivered by **PPMC-111**. The waveform is square, and the duty ratio is 50%. This signal is used together with the DIR signal of **2-3-1**. Also, be sure to connect this signal to the $\overline{\text{PIN1}}$ and $\overline{\text{PIN2}}$ signals of **2-3-3**.

2 - 3 - 3 $\overline{\text{PIN1}}$, $\overline{\text{PIN2}}$ (Internal pulse counter input)

These terminals are input terminals for the pulse counter inside **PPMC-111**. These signals are important for the operation of **PPMC-111**. Therefore be sure to connect them to the $\overline{\text{POUT}}$ signal of **2-3-2**.

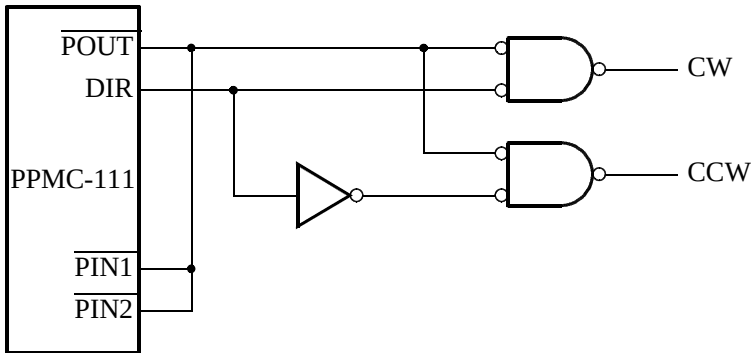


Fig. 2-8 Sample Connection of DIR, $\overline{\text{POUT}}$, $\overline{\text{PIN1}}$ and $\overline{\text{PIN2}}$ Signals

2 - 3 - 4 $\overline{\text{HOLD}}$ (Motor hold signal)

This signal indicates that the motor is stopped. The $\overline{\text{HOLD}}$ signal goes low about 2ms after the stop of pulse output. When **PPMC-111** receives the next operation command, the $\overline{\text{HOLD}}$ signal goes high. It is used for the lowering of supply voltage at motor stop or external monitoring of it.

2-4 Limit and alarm signals

These are a group of input signals from limits and motor driver. These are all negative logic inputs.
The limit signals and alarm signals as explained below must be kept low for 90microsecond or longer if they are to be detected by **PPMC-111**. Also, when a command in **Table 2-4** is executed during a pulse output, there is a period during which arrival of the limit signal or alarm signal can not be detected. That is, even if the limit signal or alarm signal is kept low for 90microsecond or longer, it may not be detected during that time. Therefore, caution must be exercised when executing these commands. When arrival of a limit signal or alarm signal can not be detected during pulse output, the specified pulse output is continued. For details, refer to the section on each command.

Table 2-4 Non-detecting Duration of Limit and Alarm Signals

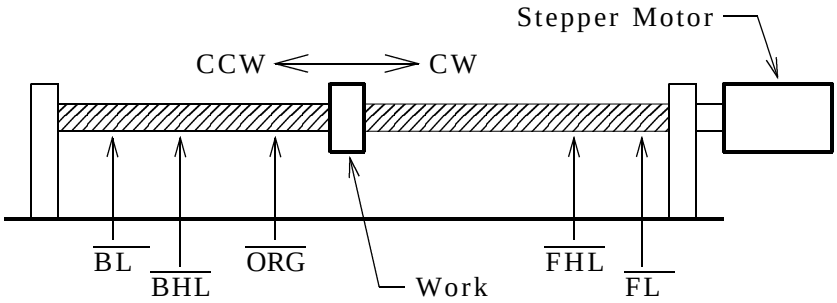
Command	Non-detection Duration
Instantaneous Speed Change	From receipt of command code to end of speed change
Acceleration/Deceleration Speed Change	From receipt of command code to start of speed change
Finish Status Read	From receipt of command code to setting of finish status code in output buffer inside **PPMC-111**
Command Error Code Read	From receipt of command code to setting of command error code in output buffer inside **PPMC-111**
Current Position Read	From receipt of command code to setting of 3rd byte (upper byte) of current position data in output buffer inside **PPMC-111**
Control Input Signal Status Read	From receipt of command code to setting of control input signal status in output buffer inside **PPMC-111**
Auxiliary Input Signal Status Read	From receipt of command code to setting of auxiliary input signal status in output buffer inside **PPMC-111**
Auxiliary Output	From receipt of command code to output of auxiliary output signal
Emergency Stop	From receipt of command code to stop of pulse output
Decelerating Stop	From receipt of command code to start of deceleration

2-4-1 $\overline{\text{ORG}}$ (Origin input signal)

PPMC-111 checks this signal only at the Constant Speed Origin Search (constant speed movement to origin) command. Upon detection of this signal, **PPMC-111** stops pulse output immediately. Normally this signal provides the origin for all positioning controls.

2-4-2 $\overline{\text{FL}}$, $\overline{\text{BL}}$, $\overline{\text{FHL}}$, $\overline{\text{BHL}}$ (Limit input signals)

$\overline{\text{FL}}$ is the limit to be set at the operation limit point in CW rotation, and $\overline{\text{BL}}$ is that in CCW rotation. For any operation command, **PPMC-111** will stop the operation when it detects this limit in any of the operational directions. Also, if an operation command in the same direction is fed after this, PPMC-111 will not output the pulse but will respond with Error No.**3**.
$\overline{\text{FHL}}$ is the high speed limit to be set in CW rotation, and $\overline{\text{BHL}}$ is that in CCW rotation. **PPMC-111** will cause a decelerating stop when it detects this limit during an acceleration or high-speed operation. In this case, if any command including an acceleration request is issued during the deceleration, **PPMC-111** will not accept it but will respond with Error No.**14**.
Fig. 2-9 shows the physical/positional relationship of the limit switches explained above.



The $\overline{FL}$ and $\overline{BL}$ limit switches are set at the respective operation limit points of work.
The $\overline{FHL}$ and $\overline{BHL}$ limit switches are set to the acceleration/deceleration pulse count or more inside from the $\overline{FL}$ and $\overline{BL}$ positions, respectively.
The $\overline{ORG}$ limit switch is set at the origin for positioning control.

Fig. 2-9 Positional Relationship of Limit Switches

As the High Speed limit signal, the $\overline{FHL}$ signal is effective at CW pulse output, and the $\overline{BHL}$ signal at CCW pulse output. And, as shown in **Table 2-5**, the stopping method upon detection of the High Speed Limit signal varies with the kind of operation command, the setting of high-speed limit effective speed pulse rate and the pulse output speed at detection of the High Speed limit signal.

Table 2-5 (Mode of stop upon detection of high speed limit)

<table>
<tr><td rowspan="3">Type of operation command</td><td colspan="4">Pulse output speed at detection of high speed limit</td><td rowspan="3">When operation command is received while high speed limit signal is already received</td></tr>
<tr><td colspan="2">< High speed limit effective speed</td><td colspan="2">> / = High speed limit effective speed</td></tr>
<tr><td>> Starting speed</td><td>= Starting speed</td><td>> Starting speed</td><td>= Starting speed</td></tr>
<tr><td>Acceleration/deceleration operation command</td><td colspan="2" rowspan="5">Continuous designated pulse output operation</td><td rowspan="6">Decelerate stop</td><td rowspan="6">Immediate stop</td><td rowspan="7">No pulse output</td></tr>
<tr><td>Constant speed operation command</td></tr>
<tr><td>Continuous constant speed operation command</td></tr>
<tr><td>Constant speed origin search command</td></tr>
<tr><td>Continuous high speed operation command</td><td>Decelerate stop</td><td>Immediate stop</td></tr>
<tr><td>Single step command</td><td colspan="4">Disregards if detected after pulse output</td></tr>
</table>

If a high speed limit effective speed pulse rate is not set using the high speed limit effective speed setting command after the **PPMC-111** (i.e., default status) is reset, the value of pulse rate at high speed established at the time of initialization shall be used as the high speed limit effective speed pulse rate.

2-4-3 $\overline{ALM}$ (Alarm input signal)

This terminal is connected to the alarm output of the motor driver. When **PPMC-111** receives this signal during its operation, it will stop the pulse output and send an Interrupt ($\overline{INT}$) signal to the host processor.

2 - 5 Auxiliary input/output signals

The Auxiliary Input/Output signals use the general-purpose 8-bit I/O ports, which have no direct relation with stepper motor control functions.

2 - 5 - 1 AUXI0-AUXI7 (Auxiliary input signals: Bit 0 - Bit 7)

AUXI0 to AUXI7 are the 8-bit input ports provided by **PPMC-111**, which serve as auxiliary input ports for the system. It takes about 40microsecond to read the state of the input ports, and no $\overline{\text{INT}}$ signal is delivered by the status change of these input ports.

2 - 5 - 2 AUXO0-AUXO7 (Auxiliary output signals: Bit 0 - Bit 7)

AUXO0 to AUXO7 are the 8-bit output ports provided by **PPMC-111**, which serve as auxiliary output ports for the system. It takes about 40microsecond for the state of the output ports to change. These output ports immediately after reset are high.

2 - 6 SEL_TYP (The value of current position counter)

It will clear the value of the current position counter inside PPMC-111.

When the origin signal ($\overline{\text{ORG}}$) is detected during Constant Speed Origin Search Operation, if this signal is made Open or High, the value of the current position counter inside PPMC-111 will be cleared to "000000h", and if it's made Low the counter won't be cleared.