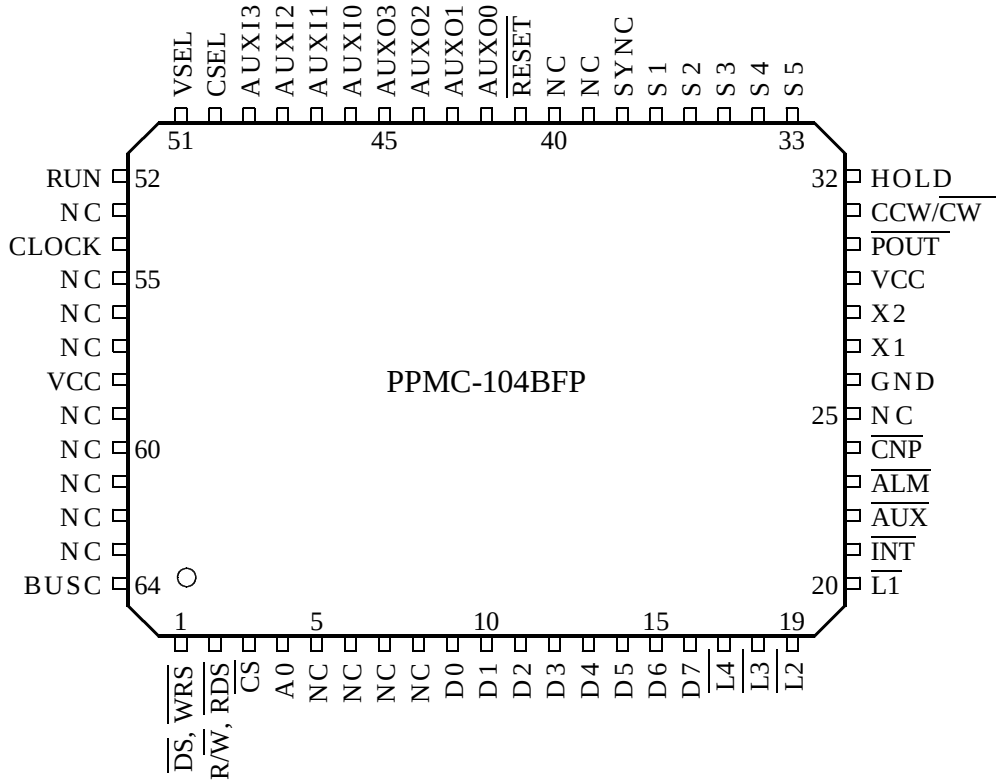
2. Pin Functions

The PPMC-104BFP has a 64 pin QFP package configuration. The layout of the pins for input/output signals is shown in Diagram 2-1, and table 2-1 is the pin assignment table. This chapter explains the details of these signals.



(TOP VIEW)

Diagram 2-1. Pin Assignment of PPMC-104BFP

2. Pin Assignment

Table2-1. Pin assignment

Pin #	Signal	I/O	Functions
1	$\overline{DS}$, $\overline{WRS}$	I	Data Strobe, Write Strobe
2	R/$\overline{W}$, $\overline{RDS}$	I	Read/Write, Read Strobe
3	$\overline{CS}$	I	Chip select input
4	$\overline{A_0}$	I	Address 0
5	NC	O	OPEN
6	NC	I	OPEN (Internal pull up)
7	NC	I	OPEN (Internal pull up)
8	NC	I	OPEN (Internal pull up)
9	D_0	I/O	Data bus bit0
10	D_1	I/O	Data bus bit1
11	D_2	I/O	Data bus bit2
12	D_3	I/O	Data bus bit3
13	D_4	I/O	Data bus bit4
14	D_5	I/O	Data bus bit5
15	D_6	I/O	Data bus bit6
16	D_7	I/O	Data bus bit7
17	$\overline{L4}$	I	CCW High Speed limit
18	$\overline{L3}$	I	CW High Speed limit
19	$\overline{L2}$	I	CCW limit
20	$\overline{L1}$	I	CW limit
21	$\overline{INT}$	O	Interrupt signal
22	$\overline{AUX}$	O	Auxiliary Control output
23	$\overline{ALM}$	I	Alarm input
24	$\overline{CNP}$	I	Origin limit
25	NC	I	OPEN (Internal pull up)
26	GND	I	Connect to GND
27	X_1	I	Crystal oscillator 1
28	X_2	I	Crystal oscillator 2
29	V_{CC}	I	5V power input
30	$\overline{POUT}$	O	pulse output
31	CCW/$\overline{CW}$	O	rotating direction 0 = CW, 1 = CCW
32	HOLD	O	motor hold signal
33	S5	O	Motor 5-phase excitation output
34	S4	O	Motor 4-phase excitation output
35	S3	O	Motor 3-phase excitation output
36	S2	O	Motor 2-phase excitation output

Pin #	Signal	I/O	Functions
37	S1	O	Motor 1-phase excitation output
38	SYNC	O	Synchronizing Signal Output (4MHz)
39	NC	O	OPEN
40	NC	O	OPEN
41	$\overline{\text{RESET}}$	I	Reset input
42	AUXO 0	O	Auxiliary Control output bit0
43	AUXO 1	O	Auxiliary Control output bit1
44	AUXO 2	O	Auxiliary Control output bit2
45	AUXO 3	O	Auxiliary Control output bit3
46	AUXI 0	I	Auxiliary Control input bit0
47	AUXI 1	I	Auxiliary Control input bit1
48	AUXI 2	I	Auxiliary Control input bit2
49	AUXI 3	I	Auxiliary Control input bit3
50	CSEL	I	Internal Clock Select (Internal pull up) 500kHz at "H" or OPEN, 125kHz at "L"
51	VSEL	I	version control (Internal pull up) PPMC-104BFP compatible at "H" or OPEN PPMC-103A/AFP data compatible at "L"
52	RUN	I	Pulse Output Start Control (Internal pull up) Starts pulse output immediately on "H" or OPEN Holds pulse output at "H" until "L"
53	NC	I	OPEN (Internal pull up)
54	CLOCK	I	External Clock signal input
55	NC	I	OPEN (Internal pull up)
56	NC	I	OPEN(Internal pull up)
57	NC	I	OPEN (Internal pull up)
58	V_{CC}	I	5V power input
59	NC	I	OPEN (Internal pull up)
60	NC	I	OPEN (Internal pull up)
61	Pull down	I	Pull down on 10k ohms resistance
62	Pull down	I	Pull down on 10k ohms resistance
63	Pull down	I	Pull down on 10k ohms resistance
64	BUSC	I	Slave Bus Interface Select

$\overline{}$ means the negative logic.

O = Output

I = Input

NC = OPEN

* Pull up or pull down unused input signals with resistance at 10k ohms.

* If the $\overline{\text{L1}}$ to $\overline{\text{L4}}$, $\overline{\text{ALM}}$, and $\overline{\text{CNP}}$ signals are not in use, pull up each unused signal with resistance at 10k ohms.

2-1. System Hardware Related Signals

2-1-1. $\overline{\text{RESET}}$ (Reset)

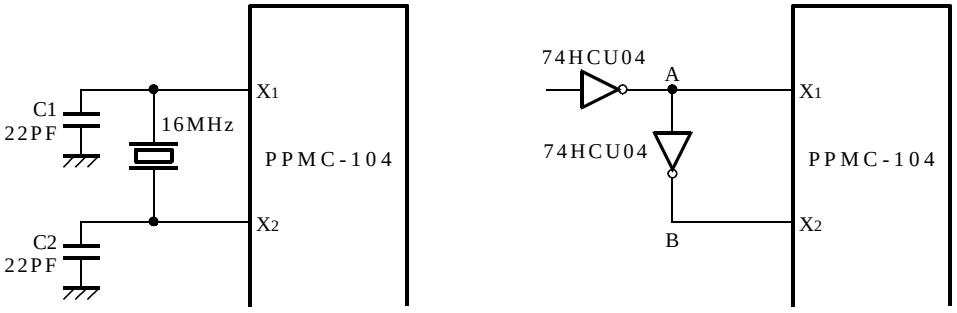
This signal is used to reset the PPMC-104BFP to its initial state. It is usually connected to the system's reset signal. After the PPMC-104BFP starts up from level "L," issue the initialization command and operation commands from the host processor to begin operation. The source voltage must be within the operation range of the PPMC-104BFP and level "L" must be maintained for at least 2 microseconds or longer after vibration of the internal oscillator has stabilized.

2-1-2. X1, X2 (Crystal Oscillator)

The X1 and X2 pins input the PPMC-104BFP's system clock. Normally, a 16MHz crystal oscillator is connected as shown in Diagram 2-2 on the left, however, a 2-phase external clock can also be used as shown in Diagram 2-2 on the right.

The X1 and X2 pins can handle clock input frequencies ranging from 1MHz to 16MHz. The operation speed of the PPMC-104BFP is proportional to the clock input frequency. The time and other parameters defined later in this document are based upon a system clock frequency of 16MHz. Other times, speeds, data, and etc. not particularly defined in the explanation are also based upon the 16 MHz system clock.

When operating multiple PPMC-104BFPs using a single system clock oscillation circuit, design the circuit using Diagram 2-3 as a reference. Make certain to follow the cautions on page 2-5.



Crystal Clock　　2-phase External Clock

Diagram 2-2.

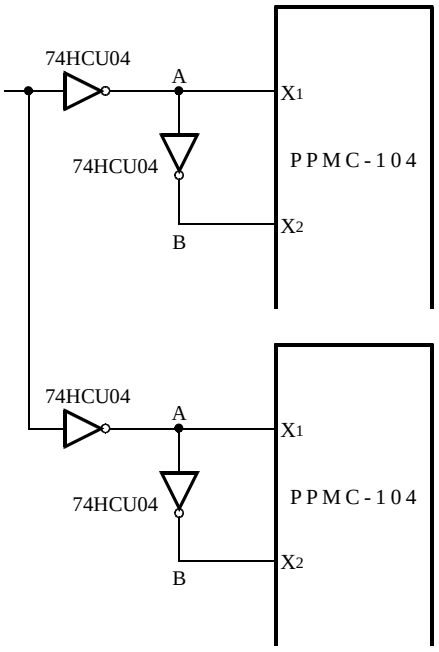


Diagram 2-3.

Cautions

(1). Crystal Oscillator

The oscillating frequency is determined by the crystal oscillator's load capacity and the external capacity C1 and C2. Stable start-up and continuation of oscillation is largely affected by the crystal oscillator's equivalent resistance and external capacity, and recommended values described in Table 2-2 should be used for reference.

Table 2-2. Equivalent series resistance

Frequency	Equivalent series resistance (Maximum)	Frequency	Equivalent series resi stance (Maximum)
1MHz	600 ohms	12MHz	35 ohms
4MHz	100 ohms	16MHz	35 ohms
10MHz	35 ohms		

(2). 2-phase external clock signal input method

When using 2-phase external clock signals as described in Diagram 2-2 (on the right) and Diagram 2-3, make certain that the following conditions are met at points A and B.

Condition 1: The duty ratio at point A should be ±5% (@Vcc/2)
Condition 2: C_L at point A and point B should equal 50pF (maximum)

2-2. Host Interface Signals

These signals connect the PPMC-104BFP to the bus of the host processor. There are signals for accessing the register of the PPMC-104BFP as well as an interrupt signal.

2-2-1. $\overline{CS}$ (Chip Select)

This is a select signal that is sent to the PPMC-104BFP and connects address signals whose upper bits are decoded. The PPMC-104BFP can be accessed when the $\overline{CS}$ is at "L"
(See Section 3-1 "Host Interface Register").

2-2-2. A0 (Register Select)

This is the signal that switches each register when the host processor reads or writes into the register of the PPMC-104BFP. This signal normally connects the least significant bit of an address signal to the appropriate register. (See Section 3-1 "Host Interface Register".)

2-2-3. D7 - D0 (Data Bus)

These are two-way 8-bit buses that exchange data between the host processor and the PPMC-104BFP.

2-2-4. BUSC (Slave Bus Interface Select)

This signal selects the interface format between the host processor and the PPMC-104BFP. This signal allows easy connection to either R/$\overline{W}$ type CPUs or $\overline{RD}$, $\overline{WR}$ separate type CPUs. For the relationship between the BUSC signal and the interface format, refer to Sections 2-2-5 and 2-2-6, as well as Table 2-3.

Table 2-3. Relation between BUSC signal and bus of host processor I/F

BUSC signal	Bus of host processor I/F	Control signal used	
H	R/$\overline{W}$ type	Data Strobe siganl ($\overline{DS}$ signal)	Read/Write signal (R/$\overline{W}$ signal)
L	$\overline{RD}$,$\overline{WR}$ separate type	Write Strobe signal ($\overline{WRS}$ signal)	Read Strobe signal ($\overline{RDS}$ signal)

2-2-5. $\overline{DS}$, $\overline{WRS}$ (Data Strobe, Write Strobe)

This signal is used as the Data Strobe signal for the R/$\overline{W}$ type CPU when the BUSC signal is high, and as the Write strobe signal for the RD, WR separate type CPU when the BUSC signal is low.
Please refer to Table 2-3

2-2-6. R/$\overline{W}$, $\overline{RDS}$ (Read/Write, Read Strobe)

This signal is used as the Read/Write signal for the R/$\overline{W}$ type CPU when the BUSC signal is high, and as the Read strobe signal for the $\overline{RD}$, $\overline{WR}$ separate type CPU when the BUSC signal is low. Please refer to Table 2-3.

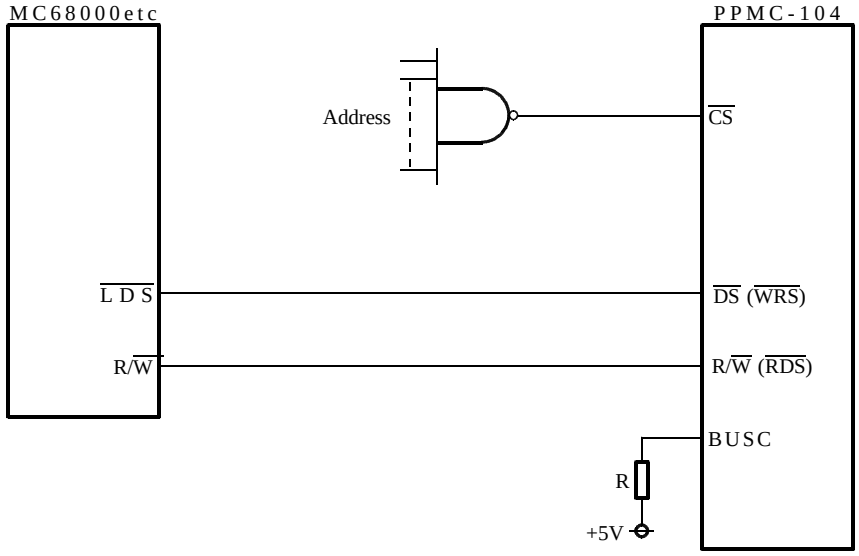


Diagram 2-4. Example connection of R/$\overline{W}$ type signal

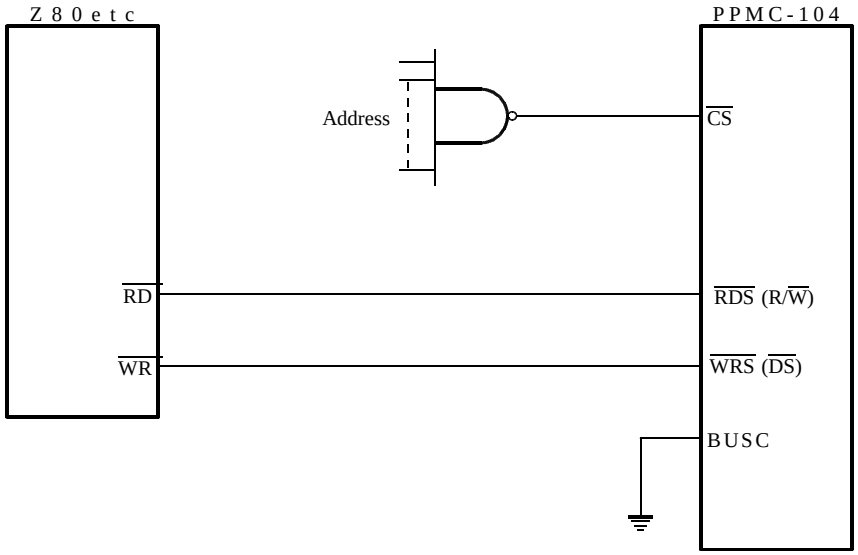


Diagram 2-5. Example connection of $\overline{RD}$, $\overline{WR}$ separate type signal

2-2-7. $\overline{INT}$ (Interrupt Signal)

When the interrupt mask is set to "0" this signal becomes "0" after pulse output is compete, and an interrupt request can be issued to the host processor. Reading the finish status sets this signal to "1", ending the interruption. Since this signal is not an open collector, be sure to provide an open collector buffer when connecting multiple interruptions (see Diagram 2-6).

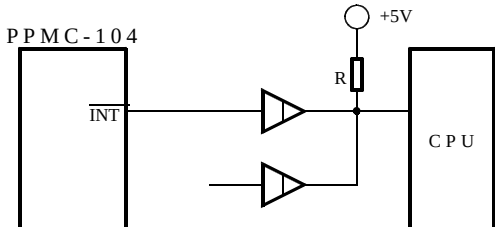


Diagram 2-6. Example connection of Interrupt output signal

If a pulse output termination interrupt occurs, issuing the Finish Status Read command clears the $\overline{INT}$ signal, changing it from "L" to "H".

2-3. Motor Control Signals

These are signals connected to the motor driver.

2-3-1. CCW/$\overline{CW}$ (Operation Direction Signals)

The CCW/$\overline{CW}$ signal is an output signal that indicates the direction of operation. This signal becomes "L" when clockwise direction pulses are outputted, and "H"when counter-clockwise direction pulses are output. This signal is used in conjunction with the $\overline{POUT}$ signal explained in Section 2-3-2.

2-3-2. $\overline{POUT}$ (Pulse Train Output Signal)

This is a pulse train signal sent by the PPMC-104BFP. The waveform of this signal is a square wave and the length of the "L" level signal is 5.0 microseconds in phase excitation mode as well as in POUT mode.This signal is used in conjunction with the CCW/$\overline{CW}$ signal described in Section 2-3-1.

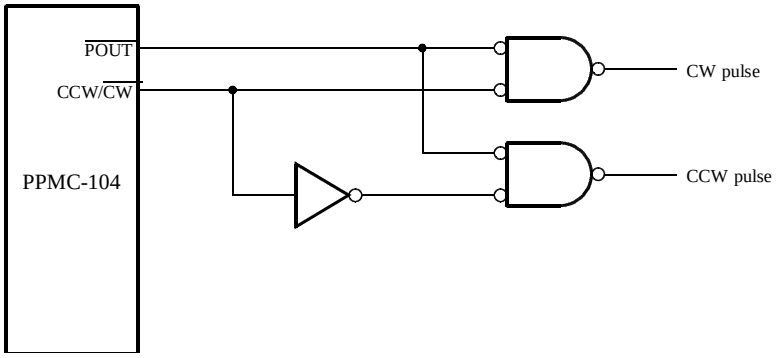


Diagram 2-7. Example connection of CCW/$\overline{CW}$, $\overline{POUT}$ signal

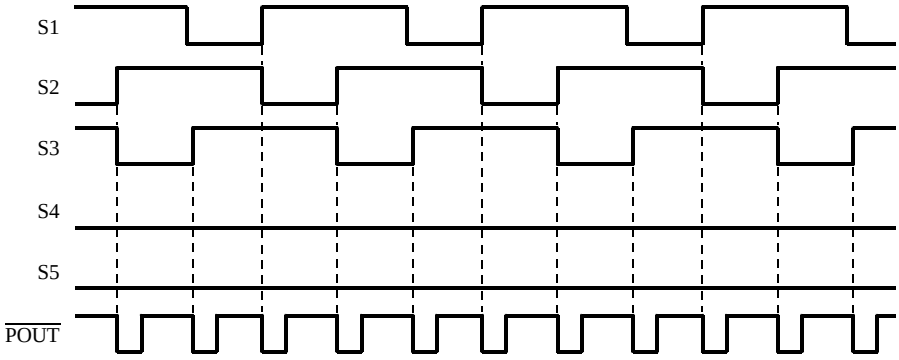
2-3-3. S1 - S5 (Phase Excitation Output)

The S1-S5 signals are phase excitation output signals given to unipolar type motors.The S1-S3 signals are used for 3-phase motors, the S1-S4 signals are used for 4-phase motors, and the S1-S5 signals are used for 5-phase motors. The output pattern of each signal is shown in Diagram 2-8.

The logical level of the output can be set as either positive or negative by the initialization command. Diagram

2-9 shows an example of the driver circuit for this case. Because the PPMC-104BFP maintains S1-S5 output levels at "1" until the initialization command is given, it is necessary to turn off the motor until initialization is complete if a positive logical level phase excitation is used. This control can also be accomplished by using an $\overline{AUX}$ output signal.

Example: With a 3 phase motor, 2-phase excitation and in positive logic



2 phase excitation

3-phase motor

	S1	S2	S3
1	▨	▨	
2		▨	▨
3	▨		▨

4-phase motor

	S1	S2	S3	S4
1	▨	▨		
2		▨	▨	
3			▨	▨
4	▨			▨

5-phase motor

	S1	S2	S3	S4	S5
1	▨	▨			
2		▨	▨		
3			▨	▨	
4				▨	▨
5	▨				▨

1-2 phase excitation

3-phase motor

	S1	S2	S3
1	▨		
2	▨	▨	
3		▨	
4		▨	▨
5			▨
6	▨		▨

4-phase motor

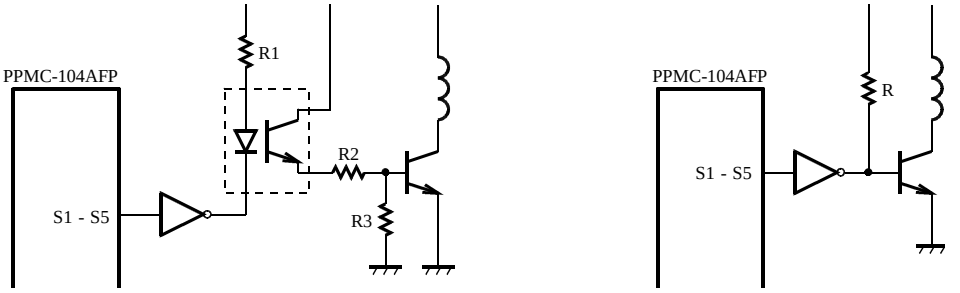
	S1	S2	S3	S4
1	▨			
2	▨	▨		
3		▨		
4		▨	▨	
5			▨	
6			▨	▨
7				▨
8	▨			▨

2-3 phase excitation

5-phase motor

	S1	S2	S3	S4	S5
1	▨	▨			
2	▨	▨	▨		
3		▨	▨		
4		▨	▨	▨	
5			▨	▨	
6			▨	▨	▨
7				▨	▨
8	▨			▨	▨
9	▨				▨
10	▨	▨			▨

Diagram 2-8. Example patters of excitation signals output



positive logical output negative logical output

Diagram 2-9. Examples of positive logical and negative logical drive circuits

2-3-4. HOLD (Motor Hold Signal)

This signal indicates that the motor is stopped. This HOLD signal becomes "H" within approximately 3.4 milliseconds after pulse output has stopped.

When the PPMC-104BFP receives the next operation command, the HOLD signal becomes "L". This signal is used to reduce the voltage of the motor's power source when the motor is stopped, or for external monitoring.

2-4. Limit Input Signals

These are a group of limit signals as well as the motor driver's input signals. These are all negative logical inputs.

In order for the PPMC-104BFP to detect each limit signal explained below, the signal must be maintained at the "L" level for at least the time it takes to output 1 pulse.

2-4-1. $\overline{\text{CNP}}$ (Origin Signal)

The PPMC-104BFP checks this signal only when the Constant Speed Origin Search Operation command is executed. When this signal is detected, the PPMC-104BFP immediately stops pulse output. Normally, this signal becomes the origin for the different positioning controls.

2-4-2. $\overline{\text{L1}}$, $\overline{\text{L2}}$, $\overline{\text{L3}}$, $\overline{\text{L4}}$ (Limit Signals)

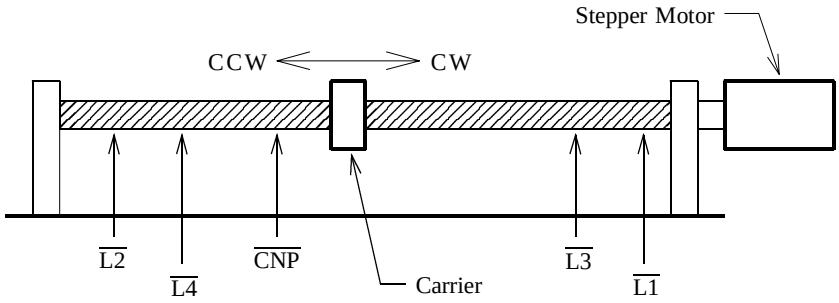
$\overline{\text{L1}}$ and $\overline{\text{L2}}$ are limit signals that are set as operation limit points for the positive (clockwise) and negative (counter-clockwise) directions respectively. The PPMC-104BFP stops all operation when either of these limit signals is detected for the applicable operation direction. Even if an operation command is given again for the same operation direction, pulse output is not executed.

$\overline{\text{L3}}$ and $\overline{\text{L4}}$ are the high speed limits for the positive(clockwise)and negative(counterclockwise) directions respectively. The PPMC-104BFP decelerates and stops operation when these limit signals are detected during acceleration or high-speed operation. Diagram 2-10 shows the physical positions of these limit signals.

2-4-3. $\overline{\text{ALM}}$ (Alarm Input Signal)

When the $\overline{\text{ALM}}$ signal becomes "L," pulse output is immediately stopped and bit 5 of the finish status is set to "1."

When the $\overline{\text{ALM}}$ is not in use, make sure to pull up the signal.



The $\overline{L1}$ and $\overline{L2}$ limit switches are set up at the operation limits of the work.
The $\overline{L3}$ and $\overline{L4}$ limit switches are set up inside of the positions of $\overline{L1}$ and $\overline{L2}$ by the number of accelerating pulses or greater .
The $\overline{CNP}$ limit switch is set up at the origin of the positioning control.

Diagram 2-10. Limit switches relation positioning

2-4-4. RUN (Pulse Output Start Control)

When an operation command is issued from the host processor, this signal is checked before pulse output is executed. If this signal is at the "H" level, pulse output is immediately initiated. When the signal is at the "L" level, the status remains "BUSY", and the PPMC-104BFP holds pulse output and waits for this signal to become "H." Commands other than Immediate Stop and Decelerating Stop, both of which are accepted during pulse output, can be accepted when this signal is at the "L" level. When a stop command is received, Error number "1" will be returned. This signal is used when starting operation of multiple PPMCs simultaneously and so on.

2-5. Auxiliary Input/Output Signals

There are general-purpose 4-bit input/output ports that are not directly related to the pulse motor control function, and 1-bit auxiliary control outputs that are equivalent to those of the PPMC-103.

2-5-1. AUXI0 - AUXI3 (Auxiliary Input Signal Bit0 - Bit3)

AUXI0~AUXI3 are 4-bit input ports provided by the PPMC-104BFP, and can be used as the system's auxiliary input ports. A minimum of approximately 20 microseconds to a maximum of approximately 97 milliseconds are required to read the input port status, and the $\overline{INT}$ signal is not output by a status change in this input port.

2-5-2. AUXO0 - AUXO3 (Auxiliary Output Signal Bit 0-Bit 3)

AUXO0~AUXO3 are 4-bit output ports provided by the PPMC-104BFP and can be used as the system's auxiliary output ports. Approximately 40 microseconds are required for the output port status to change. Because the output pulse train is delayed for this length of time, it is necessary to run a test to determine whether or not problems such as a stepout might occur. This output port is at the "H" level immediately after a reset.

2-5-3. $\overline{\text{AUX}}$ (Auxiliary Control Output)

This output signal can be turned ON or OFF using a command from the host processor. This signal can be controlled even during motor operation, independent of motor control. This signal is negative logical, and after the PPMC-104BFP is reset, it maintains the "H" level until the ON command is received. However, in order for the PPMC-104BFP to process the output ON/OFF command during motor operation, approximately 14 microseconds are required, during which the output pulse train is delayed. Therefore, it is necessary to run a test to determine whether or not problems such as a stepout might occur.

2-6. CLOCK (External Clock)

This is a timing signal that becomes the origin for the speed control of the pulse motor in external clock mode. The external clock signal has the limits described in Diagram 2-11.

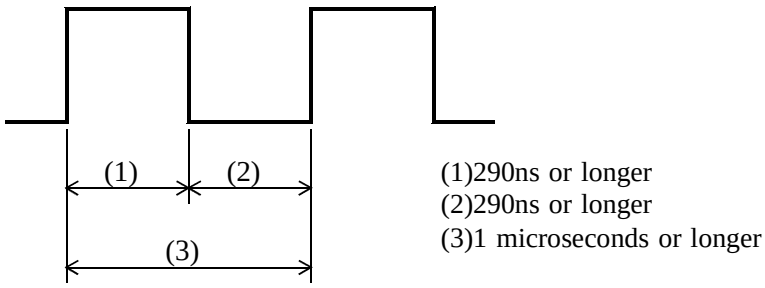


Diagram 2-11 . Limitation of External clock input

2-7. SYNC (Synchronizing Signal Output)

This is a pin that outputs a quarter of the clock inputted at X1 and X2 explained in Section 2-1-2

2-8. CSEL (Internal Clock Select)

This is a pin that selects a base clock frequency for the internal clock mode. 500kHz is selected when this signal is set to "H" or OPEN, and 125kHz is selected when it is set to LOW.

2-9. VSEL(Version Control)

This is a pin that determines compatibility with the speed and switching parameters of the existing version of the PPMC. When VSEL is at "H" or OPEN, it becomes compatible with the PPMC-104AFP. When the VSEL is at "L," it becomes data compatible with the PPMC-103A/AFP.