

# MWSC-101

**Ver 0.6**

**Ampere**

# MWSC-101

## MotionWare System Control LSI

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## Overview

The MWSC-101 is Motionware's main LSI that controls multiple slaves with the PPMC-112 and PIOC-101 from a central location. The MWSC-101 can connect up to 16 slaves together, such as the PPMC and PIOC, and allows high-speed communication at a maximum speed of 125 kbpS. It has an 8 bit bus interface allowing easy connection to the host system.

# 1. *MWSC-101 commands*

## 1-1. *Command structure*

Commands are broadly divided into system commands, which are given to the MWSC-101, and slave commands which are given to individual slaves.

A command code consists of 1 byte. To issue a command, write the command code in the command register, then write the data that is unique to the command into the data register.

Table 2. Command structure

Bit					Command
7	6	5	4	3 - 0	
x	x	1	1	Command code	System commands
x	x	0	0	Slave address	Slave start commands
x	x	0	1		Slave output commands
x	x	1	0		Slave input commands
Other					Reserve

## 1-2. *Command codes for system commands*

System commands are control commands given to the MWSC-101. There are 11 commands in all, including initialization, polling control, and diagnostic.

## 1-3. *Command codes for slave commands*

In a slave command, a 1 byte command containing a device address is written into the command register. The first data of returned in response to the slave command also becomes the address of the controlled device. Because the MWSC-101 simultaneously controls multiple devices, the commands and responses do not necessarily occur in pairs, and the commands and results are recognized by their device addresses.

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## 2. *Process*

The MWSC-101 executes the commands given by the host one after another. The commands are temporarily written into the MWSC's internal buffer and, for commands given to slaves, are executed after the communication channel is opened. Up to two commands are written into the buffer at a time. When the first byte of the third command enters the buffer, the status register's IBF (Input Buffer Full) flag is set to "1", and no more bytes can be written into the buffer.

In most cases, the MWSC reports the results of host command executions to the host. When the MWSC reports to the host, an interrupt signal is issued. Because the MWSC's internal buffer has limited capacity, the host cannot ignore this interrupt signal and continue giving commands one after another. When the internal buffer is full, the MWSC halts operation and waits for the host to read the output before adding the next command to the buffer. The MWSC does not accept host commands during this process.

When the MWSC reports the results of slave command executions to the host, it sends the slave's device number at the beginning of the data. A mode can be set for the normal completion of slave commands so that the interrupt signal is not issued.

## 3. *System commands*

There are nine different types of system commands as listed below. System command codes are written in the command register when the IBF flag shows "0". If the code contains data, the data are written into the data register after the command code every time the IBF flag reads "0".

System command codes

- xx110000 Initialization Polling Command
- xx110001 Polling Start Command
- xx110010 Polling Stop Command
- xx110011 Emergency Stop Command
- xx110100 Busy List Command
- xx110101 Direct Command
- xx110110 Interlock Configuration Command
- xx110111 Error Counter Read Command
- xx111000 Polling Prohibit Command
- xx111001 Polling Resume Command
- xx111111 Status Check Command

## 3-1. Initialization Polling Command

### Overview

The Initialization Polling Command checks all devices connected to the serial line and creates internal tables, sending an interrupt signal to the host and reporting the connection status. When no devices are connected, this command is repeated three times, and it may take some time (approx. 300 milliseconds to 3.5 seconds) before the host receives the interrupt signal.

Make sure to issue this command first before issuing any other commands.

### Code

Command code \$30

Command code only, contains no data.

7	6	5	4	3	2	1	0	
x	x	1	1	0	0	0	0	Command register

### Returned value

The returned value consists of 16 bytes. The PPMC/SYNC version of each device address and whether or not devices are connected are returned from channel 0. The SYS bit is set to "1" in the status register, an interrupt signal is sent, and the returned value is read from the data register.

Table 3.

Returned value	Meaning
	PPMC-112
	SYNC-101
	PIOC-101
\$00	Slave device not connected.
\$FF	Poor communication due to problems such as overlapping addresses (see note) and incorrect baud rate settings.

(Note: When two slaves return the same data at the same time, the MWSC-101 may recognize them as a single slave.

7	6	5	4	3	2	1	0	
Channel 0								Data register
Channel 1								
Channel 2								
Channel 3								
⋮								
⋮								
Channel 12								
Channel 13								
Channel 14								
Channel 15								

## 3-2. Polling Start Command

### Overview

This command initiates polling. The slave (such as a PPMC-112) does not voluntarily report the completion of operation of devices such as motors. The completion is recognized for the first time only when the MWSC-101 goes out and checks the status of the slave (called "polling"). Based on the table created by the Initialization Polling Command, the MWSC-101 continuously conducts polling, checking the status of each operating slave.

When polling is initiated and the devices for which operation commands are completed, or the device that is released from an interlock is detected, an interrupt signal is issued to the host, and the channel number and the completion report data are written into the data register.

### Code

Command code \$31

Command code only, contains no data.

7	6	5	4	3	2	1	0	
x	x	1	1	0	0	0	1	Command register

### Returned value

There is no returned value for this command.

## 3-3. Polling Stop Command

### Overview

This command halts polling.

### Code

Command code \$32

Command code only, contains no data.

7	6	5	4	3	2	1	0
x	x	1	1	0	0	1	0

### Returned value

There is no returned value for this command.



### 3-4. *Polling Prohibit Command*

#### Overview

This command prohibits polling of specified slaves. When an interlock is executed by the hardware to simultaneously run multiple slaves that cannot be controlled by a regular interlock configuration command, this command is used so that polling of the interlocked slaves is not executed.

#### Code

Command code \$38. This command, followed by a 2-byte bit map, specifies the slave device for which polling will be prohibited. Set the channel to "1" for the device for which you would like polling to be prohibited.

7	6	5	4	3	2	1	0	
x	x	1	1	1	0	0	0	Command register
C7	C6	C5	C4	C3	C2	C1	C0	Lower 8 channels
C15	C14	C13	C12	C11	C10	C9	C8	Upper 8 channels

#### Returned value

There is no returned value for this command. If initialization polling is not complete, an error is returned to indicate that initialization polling has not been completed.

Even if initialization polling sets slaves that are not connected, an error will not be returned to indicate that the device is not connected.

### 3-5. *Polling Resume Command*

#### Overview

This command allows polling that has been temporarily prohibited by the above mentioned Polling Prohibit Command to resume.

#### Code

Command code \$39. The command, followed by a 2-byte bit map, sets the slave device for which polling is to resume to "1".

7	6	5	4	3	2	1	0	
x	x	1	1	1	0	0	1	Command register
C7	C6	C5	C4	C3	C2	C1	C0	Lower 8 channels
C15	C14	C13	C12	C11	C10	C9	C8	Upper 8 channels

#### Returned value

There is no returned value for this command. When initialization polling is not complete, an error is returned to indicate that the initialization polling has not been completed. Even if the specified device is not detected by initialization polling, an error is not returned to indicate that the device is not connected.

## 3-6. *Emergency Stop Command*

### Overview

This command checks the slave's operation status, sends the Emergency Stop Command (PPMC-112 's command) to the running device, and reports the results via returned value.

### Code

Command code \$33

Command code only, contains no data.

7	6	5	4	3	2	1	0	
x	x	1	1	0	0	1	1	Command register

### Returned value

The SYS bit of the status register is set to "1" sending an interrupt signal, and the returned value is read from the data register.

"1"        Unable to stop.

"0"        Stopped.

7	6	5	4	3	2	1	0	
C7	C6	C5	C4	C3	C2	C1	C0	Lower 8 channels
C15	C14	C13	C12	C11	C10	C9	C8	Upper 8 channels

## 3-7. *Busy List Command*

### Overview

This command creates a list of devices in operation.

### Code

Command code \$34

Command code only, contains no data

7	6	5	4	3	2	1	0	
x	x	1	1	0	1	0	0	Command register

### Returned value

The returned value is a 2-byte list of slaves in operation. The SYS bit in the status register is set to "1", sending an interrupt signal, and the returned value is read from the data register.

"1"        In operation.

"0"        Stopped or no slave detected.

7	6	5	4	3	2	1	0	
C7	C6	C5	C4	C3	C2	C1	C0	Lower 8 channels
C15	C14	C13	C12	C11	C10	C9	C8	Upper 8 channels

## 3-8. Direct Commands

### Overview

This command is used to initiate direct communication with a specified slave. The input into the MWSC-101 is sent to the slave as is. The received data from the slave is also sent as is, and an interrupt signal is issued every 1 byte. This command can be used only when polling is halted and no other slaves are executing commands. If this command is used during polling, the error code \$86 is returned.

When the slave is a PPMC-112, this command can be used as the "Initialization Command for the free-curve acceleration/deceleration method" and as the "Acceleration/Deceleration Table Read Command".

When continuing to initiate additional communications with the same device, begin by writing a direct command. When other commands are initiated without waiting for reception of the returned data, the remainder of the returned data to be received will be discarded.

### Code

Command code \$35

7	6	5	4	3	2	1	0	
x	x	1	1	0	1	0	1	Command Register
0	0	0	1	Slave address				Data Register
Command and Data of slaves such as PPMC-112								} The calculation range of SUM
SUM								

### Calculation method for SUM

Reciprocal of the sum of all data (including slave address items) written in the data register.

### Returned value

The returned value varies depending upon the command. In the PPMC-112's "Read Acceleration/Deceleration Table Command", close to 400 bytes of data may be sent from the PPMC-112.

An interrupt signal is issued by the MWSC-101 when the SYS, ERR, COMS, INTD, or INTR bits are set to "0" in the status register. Then, the returned value is read from the data register.

Because every time the PPMC-112 returns 1 byte of data (every 88 microseconds), the MWSC-101 issues an interrupt signal, the host must read the data. When the host does not read the data in time, the data will be overwritten. In such cases, the ERR flag is set, an interrupt signal is sent, and the error code \$8A is returned. When using this command, first determine carefully whether or not the host can process an interrupt signal every 88 microseconds.

## 3-9. Interlock Configuration Commands

### Overview

Occasionally, when operation has reached a certain point, the next motor needs to be initiated. This is often accomplished by measuring the approximate amount of time elapsed. Interlock configuration commands allow the next motor to be initiated when operation has reached a specified point. This command enables synchronized movement of the motors based on set positions without any help from the host. This command cannot be issued during polling.

#### a. Hardware Interlock:

The PPMC-112 issues a pulse to the position set by the "Interlock Release Position Setting Command", and sends an INTLK signal. The lower (next) PPMC-112, connected electrically by a cable, receives this signal as a RUN signal and initiates the previously received operation command.

This Interlock, which uses the INTLK-RUN signal and a cable, is called a hardware interlock.

#### b. Software Interlock:

The above mentioned hardware interlock requires an electrical connection using a cable to transmit the INTLK-RUN signal, but this does not necessarily mean that PPMC-112s installed right next to one another are interlocked.

A software interlock solves this problem. When the controlling PPMC-112 reaches the specified point, the PPMC-112 reports its status to the MWSC-101, which is executing polling, instead of issuing INTLK signal.

In accordance with the Interlock configuration command, the MWSC-101 sends the operation command to the controlled PPMC-112. This interlock, however, sends out the operation command via the MWSC-101, and thus takes longer, and may not reach the controlled PPMC-112 in time before the motor of the controlling PPMC-112 has advanced.

### Code

Command code \$36

7	6	5	4	3	2	1	0	
x	x	1	1	0	1	1	0	Command Register
Data length (data length excluding this byte)								Data Register (Data length = 2 to 32)
HL	0	0	0	Controlled slave address				HL = 0 Software interlock
0	0	0	0	Controlled slave address				HL = 1 Hardware interlock
⋮								
⋮								
HL	0	0	0	Controlled slave address				
0	0	0	0	Controlled slave address				

### Returned value

There is no returned value for this command.

## 3-10. *Error Counter Read Command*

### Overview

This command checks the performance of communication with the slaves. This command can only be issued when no polling of slaves is being executed.

### Code

Command code \$37

7	6	5	4	3	2	1	0	
x	x	1	1	0	1	1	1	Command register
0	0	0	0	Slave address				Data register

### Returned value

The returned value consists of the number of frames sent (3 bytes), the number of communication errors that have occurred (2 bytes), and the error counter value within the slave (2 bytes). The SYS bit is set to "1" in the status register and an interrupt signal is issued, after which the returned value is read from the data register.

Every time this command is issued, the counter of the channel that the command is issued to is reset to "0".

7	6	5	4	3	2	1	0
The number of frames sent (lower byte)							
The number of frames sent (middle byte)							
The number of frames sent (upper byte)							
The number of communication errors (lower byte)							
The number of communication errors (upper byte)							
Slave's error counter value(lower byte)							
Slave's error counter value (upper byte)							

## 3-11. Status Check Command

### Overview

This command checks the status of slave devices.

### Code

Command code \$3F

7	6	5	4	3	2	1	0	
x	x	1	1	1	1	1	1	Command register
0	0	0	0	Slave address				Data register

### Returned value

The returned value consists of 1 byte and represents the device address and the device status. The value gives the status of the specified slave address only. The SYS bit is set in the status register, an interrupt signal is issued, and the returned value is read from the data register.

7	6	5	4	3	2	1	0	
0	0	0	0	Slave address				Data register
RUN	SPD	LKD	HLK	POL	x	SYN	AD	

RUN: Motor is in operation.

SPD: Run command is reserved by interlock.

LKD: Controlled slave is locked by interlock (set by the Interlock Release Position Setting Command).

HLK: Hardware interlock (set by the Interlock Configuration Command).

POL: Polling is prohibited (set by the Polling Prohibit Command).

SYN: SYNC-101 is connected.

AD: Normal connection status.

## 3-12. Version Read Command

### Overview

This command reads the version of the MWSC-101.

### Code

Command code \$3E

7	6	5	4	3	2	1	0	
x	x	1	1	1	1	1	0	Command register

### Returned value

A 1- byte value representing the version of the MWSC-101 is returned. The SYS bit is set to "1" in the status register, an interrupt signal is sent, and the returned value is read from the data register.

7	6	5	4	3	2	1	0
Version							

## 4. *Slave commands*

Slave commands control the slave controller. A slave command consists of a command code and data, and the command code controls the command given to the slave device via communication channels. There are three different types of slave commands: start commands, output commands, and input commands. The input/output commands include regular input/output commands as well as the slave direct communication start command. The slave Direct Communication Start Command is indirectly processed by the system commands, and is explained in the system command section.

### 4-1. *Slave start commands*

#### Overview

Slave start commands are used to send commands to begin operation of a PPMC-112. In addition to the start commands, the PPMC-112's operation commands also include stop commands and change speed commands. Because the MWSC-101 cannot distinguish between these commands, they are differentiated and given by the host. Slave start commands are used for the following PPMC-112 operation commands.

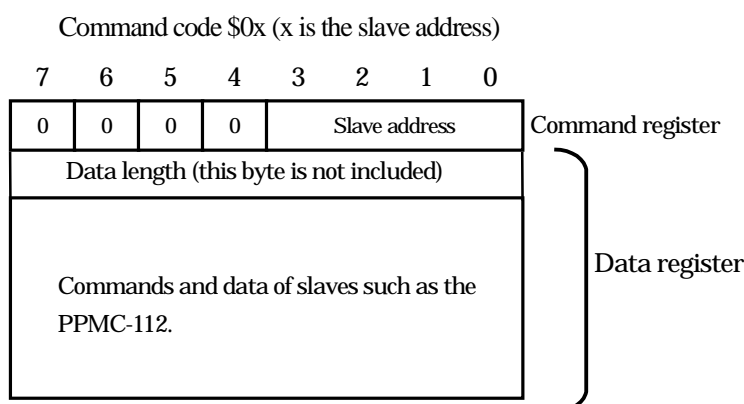
- \* Acceleration/Deceleration Operation Command
- \* Constant Speed Operation Command
- \* Continuous Constant Speed Operation Command
- \* Continuous High Speed Operation Command
- \* Constant Speed Origin Search Operation Command

For slaves that are connected to the SYNC-101, operation commands, except for the Single Step Command, are executed as slave start commands.

When a slave is started by a slave start command, the polling process is initiated automatically by the MWSC-101's Polling Start Command. Operation commands can be executed as slave output commands, but in this case, the polling process will not be initiated and end of run will not be reported. The Single Step Command, Emergency Stop Command, Decelerating Stop Command, as well as the Instantaneous Speed Change Command and Acceleration/Deceleration Speed Change Command should be processed as slave output commands.

Slave start commands assign the total number of bytes occupied by the command and the data as a data length at the beginning of the command, and this command has the same structure as the parallel mode command given to the PPMC-112. The data length and the PPMC-112 command, as well as its data, must all be written into the data register.

#### Code



## Returned value

This value is returned in response to the command. The MWSC-101 does not recognize PPMC-112's commands or any data that are attached to the command. Communication must be executed first to determine whether or not this is a code, status, or range acceptable to the PPMC-112. Please see the PPMC-112 manual for details. The error codes are listed toward the back of the manual. The "no error" code is "\$00".

The returned value for slave start commands consists of 2 bytes. The first byte is the device address, and the second byte represents acknowledgement or an error number. When the returned value is read from the data register, the OBF is set to "1", and an interrupt signal is sent to the host. Once all data is read from the data register, the interrupt signal is canceled.

When the returned value is ready to be read from the data register, the OBF flag is set to "1", and an interrupt signal is issued to the host CPU. This interrupt signal is released when the returned value is read from the data register. Please refer to section 7-3.5.

7	6	5	4	3	2	1	0
0	0	0	0	Slave address			
Returned value							

If the MWSC-101 is in the process of polling, initiated by the Polling Start Command, when the operation initiated by the slave start command is complete, the INTR interrupt is sent in accordance with the COMS bit, and the completion status is read from the data register. A 2 byte value consisting of a slave address and the completion status is returned. Please refer to section 7-3.7.

7	6	5	4	3	2	1	0
0	0	0	0	Slave address			
ALM	FL	BL	FHL	BHL	ORG	CMD	NML

- ALM: Stop by detection of alarm signal
- FL: Stop by detection of CW direction Limit signal
- BL: Stop by detection of CCW direction Limit signal
- FHL: Decelerating stop by detection of CW direction High Speed Limit signal
- BHL: Decelerating stop by detection of CCW direction High Speed Limit signal
- ORG: Stop by detection of ORG signal
- CMD: Stop by detection of Stop Command
- NML: Stop by detection of normal operation



## 4-2. Slave output commands

### Overview

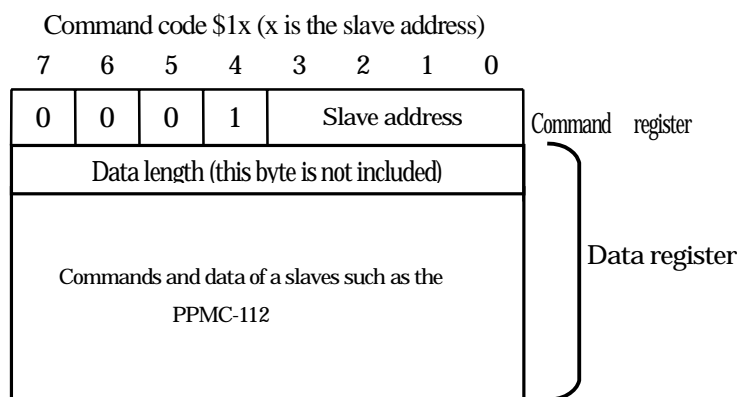
Slave output commands are commands that set data, and are used for the following operation commands given to the PPMC-112.

- \* Single Step Command
- \* Change Speed Command
- \* Stop Command
- \* Auxiliary Output Command
- \* Current Position Setting Command
- \* High Speed Limit Effective Speed Setting
- \* Initialization Command

Following the MWSC-101's command and data length, the PPMC-112's parallel mode command and accompanying data are given. The data length, the PPMC-112 command, and the data themselves are all written into the data register. These commands may not be executed under certain slave conditions. Whether or not the command can be executed cannot be determined by the MWSC-101, (Change speed commands can be issued even when the slave is not in operation). Better throughput for the entire system may be obtainable if the status of the slave is checked first using the Status Check Command from the host, to determine whether or not the command can be executed.

However, when the Emergency Stop Command is issued, for example, if the slave has already completed the operation, an error might occur, depending upon the timing. This is not something that can be avoided.

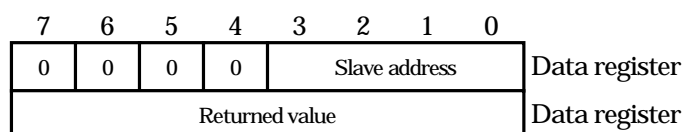
### Code



### Returned value

This is the value returned in response to the command. The MWSC-101 does not recognize a PPMC-112's commands or any data that are attached to the command. Communication must first be initiated to determine whether or not this is a code, condition, or range that is acceptable to the PPMC-112. Please see the PPMC-112 manual for details. The error codes are listed toward the back of the manual. The "no error" code is \$00.

When the returned value is ready to be read from the data register, the OBF flag is set to "1", and an interrupt signal is issued to the host CPU. This interrupt signal is released when the returned value is read from the data register. Please refer to section 7-3.5.



## 4-3. *Slave input commands*

### Overview

The slave input commands read data, and are used for the following PPMC-112 commands for which the data length to be sent is expressed using 1 byte.

- \* Auxiliary Command
- \* Current Position Read Command

These commands are made up only of command words and no data is attached. The number of bytes to be received as a result of the command is given as the received data length before the command. This command has the same structure as the parallel mode command given to the PPMC-112. The received data length and the PPMC-112 command are all written into the data register.

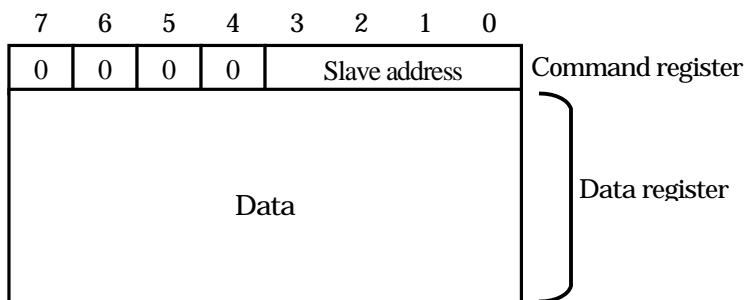
### Code

Command code \$2x ( x is the slave address)

7	6	5	4	3	2	1	0	
0	0	1	0	Slave address				Command Register
Data length to be received								Data register
PPMC command								Data register

### Returned value

The value returned in response to slave input commands consists of the device address and the number of bytes specified by the command issued. The INTD bit in the status register is set to "1", an interrupt signal is sent, and the returned value is read from the data register.



## 5. *Input/output signals*

### 5-1. *Signal table*

This table indicates the MWSC-101's input/output signals. Items marked with an asterisk (\*) indicate negative logic.

Table 4.

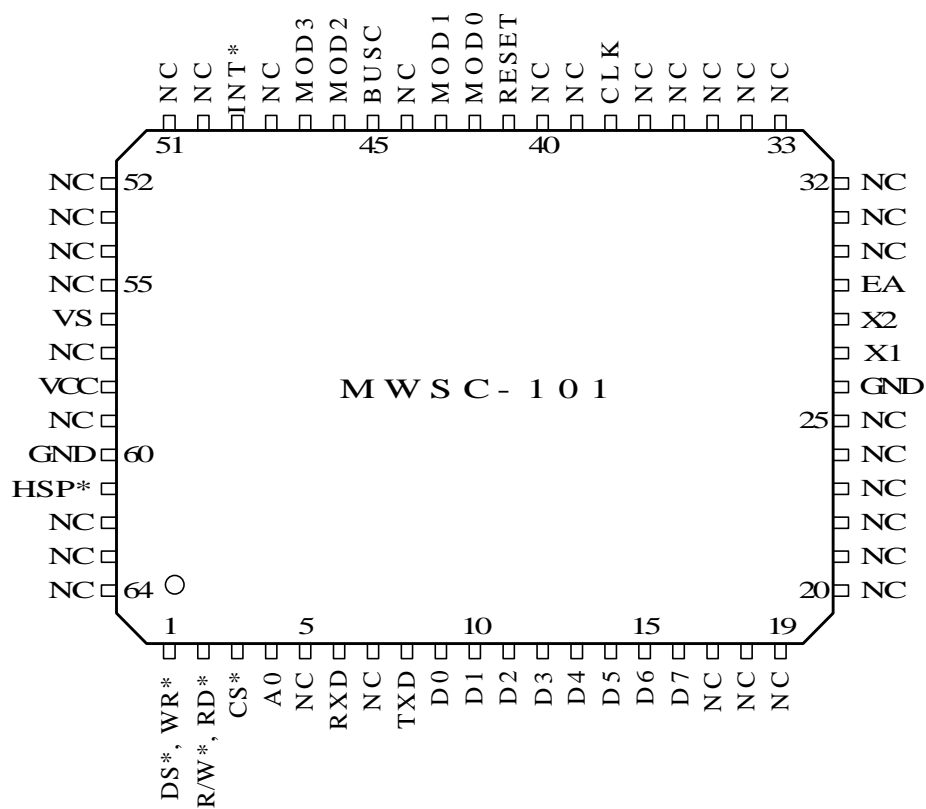
Pin Number		Signal Name	I/O	Function
QFP	SDIP			
1	7	DS*/SWR*	I	Data Strobe/Write Strobe
2	8	RW*/SRD*	I	Read Write/Read Strobe
3	9	CS*	I	Chip select input
4	10	A0	I	Address 0 input
5	11	NC	I	
6	12	RXD	I	Serial communication receive input signal
7	13	NC	I	
8	14	TXD	O	Serial communication send output signal
9	15	D0	I/O	Host I/F Data bus bit 0
10	16	D1	I/O	Host I/F data bus bit 1
11	17	D2	I/O	Host I/F data bus bit 2
12	18	D3	I/O	Host I/F data bus bit 3
13	19	D4	I/O	Host I/F data bus bit 4
14	20	D5	I/O	Host I/F data bus bit 5
15	21	D6	I/O	Host I/F data bus bit 6
16	22	D7	I/O	Host I/F data bus bit 7
17	23	NC	I	
18	24	NC	I	
19	25	NC	I	
20	26	NC	I	
21	27	NC	I	
22	28	NC	I	
23	29	NC	I	
24	30	NC	I	
25	31	NC	I	
26	32	GND	I	Power GND
27	33	X1	I	Crystal Input or External Clock Input 1(16MHz))
28	34	X2	I	Crystal Input or External Clock Input 2(16MHz)
29	35	EA	I	Connect to +5V
30	36	NC	I	
31	37	NC	I	
32	38	NC	I	
33	39	NC	I	

34	40	NC	I	
35	41	NC	I	
36	42	NC	I	
37	43	NC	I	
38	44	CLK	O	System Clock (4MHz) output
39	45	NC	O	ATTENTION!! Do not connect to anything
40	46	NC	O	ATTENTION!! Do not connect to anything
41	47	RESET*	I	Reset input
42	48	MOD0	I	Serial communication baud rate control bit 0
43	49	MOD1	I	Serial communication baud rate control bit 1
44	50	NC	I	
45	51	BUSC	I	Host bus I/F selection
46	52	MOD2	I	
47	53	MOD3	I	
48	54	NC	I	
49	55	INT*	O	Interrupt output
50	56	NC	I	
51	57	NC	I	
52	58	NC	I	
53	59	NC	I	
54	60	NC	I	
55	61	NC	I	
56	62	VS	I	Power detection input
57	63	NC	I	
58	64	Vcc	I	Power 5V
59	1	NC	I	
60	2	GND	I	Power GND
61	3	HSP*	I	High speed protocol
62	4	NC	I	
63	5	NC	I	
64	6	NC	I	

Do not connect NC output to anything.

Connect NC input to VCC, GND.

## 5-2. MWSC-101 Terminal Assignment Diagram



## 5-3. *Host interface bus signals*

The host interface bus signals are signals that connect the MWSC-101 to the bus of the host processor. They are either signals for accessing the registers of the MWSC-101 or are interrupt signals.

### 5-3-1. CS\* (Chip select)

The chip select signal for the MWSC-101 connects signal decoding with the upper bits of an address signal. The MWSC-101 is accessible when this CS is low.

### 5-3-2. A0 (Register select)

This is the signal to switch each register when the host processor reads or writes into the register of the MWSC-101, and normally connects the LSB of an address signal.

### 5-3-3. D7 - D0 (Data bus)

These are reciprocal 8-bit buses for data exchange between the host processor and the MWSC-101.

### 5-3-4. BUSC (Slave Bus Interface Select)

This signal selects the mode of the interface between the host processor and the MWSC-101. This signal allows easy connection to either of the R/W type CPUs or the RD, WR separate type CPUs.

Table 5. BUSC Signal

BUSC Signal	Host processor bus I/F	Control signal used	
H	R/W type	Data strobe signal (DS Signal)	Read/Write signal (R/W Signal)
L	RD, WR separate type	Write strobe signal (WRS signal)	Read strobe signal (RDS signal)

### 5-3-5. DS/WRS (Data Strobe/Write Strobe)

This signal is used as the Data Strobe signal for the R/W type CPU when the BUSC signal is high, and as the Write strobe signal for the RD, WR separate type CPU when the BUSC signal is low. Please refer to Table 5.

### 5-3-6. R/W, RDS (Read/Write, Read Strobe)

This signal is used as the Read/Write signal for the R/W type CPU when the BUSC signal is high, and as the Read strobe signal for the RD, WR separate type CPU when the BUSC signal is low. Please refer to Table 5.

### 5-3-7. INT\* (Interrupt signal)

The Interrupt signal for the host processor is delivered in the following cases:

- 1) Reception of the data returned from the slave in response to the slave command is completed. (INTD)
- 2) The PPMC's operation command is completed, or the interlock is released. (INTR)
- 3) An error occurs during communication with the slave. (COMS)
- 4) The value returned in response to a system command is sent. (INTD)
- 5) The command has an error (ERR).

The INT signal, which is normally high, becomes low when one of the above conditions is met, sending a request to the host to read the data. Since the INT/signal terminal is not an open collector, an open collector buffer must be provided when multiple MWSC-101s are connected to the host.

## 5-4. Initialization Input signal

The Initialization Input signal specifies the communication speed and the communication protocol of the system.

### 5-4-1. MOD1, 0 (Communication Speed Setting signal)

MOD1, 0 is a signal that sets the communication speed with the slave. Table 6 shows the setting values and the baud rates. When the value is set to "00", the MWSC sends an interrupt signal and the error code "82h" to stop the system.

Table 6.

MOD 1	MOD0	Communication speed to be set
0	0	Error
0	1	31.25 kbpS
1	0	62.5 kbpS
1	1	125 kbpS

### 5-4-2. MOD 2 (Operation mode setting input 2)

MOD2 is a signal that specifies an interrupt signal to be sent when communication of the slave command is completed normally.

When communication ends normally, the COMS bit is set to "1", and a slave address and an error code are sent as an interrupt from the MWSC-101. This may be effective during the debugging process, but an interrupt signal is issued even under normal conditions, and this may add an additional load to the host.

Setting this bit to "1" allows an interrupt signal to be sent only when there is a communication error.

Table 7

MOD2	
1	Only when communication error occurs.
0	When acknowledgement is received or when an error occurs.

### 5-4-3. MOD3 (Operation mode setting input 3)

MOD3 is an input signal given in response to the command code which specifies the method of error processing. When a new command code is given in the middle of a command input to the MWSC, if the MOD3 is set to "0", an error interrupt is issued and the new code is ignored. However, if the MOD3 is set to "1", an error is not issued and the new code becomes effective.

Table 8

MOD3	
0	Error. New command is ignored.
1	New command becomes effective

### 5-4-4. HSP\* (High speed protocol specifying input)

HSP\* is a signal that specifies the use of the mechanism to conduct a busy check at high speed during communication with the PPMC-112. The MWSC-101 conducts busy checks using the Polling Start Command.

When the HSP\* is set to "0", the MWSC-101 proceeds to the next process without waiting for the checksum of the busy check from the PPMC-112. The PPMC can also specify the same mechanism, and using this method can make the polling speed twice as fast.

HSP	
0	Does not wait for checksum.
1	Waits for check sum.

### 5-4-5. Slave communication interface signals (TXD, RXD)

MWSC-101 communicates with PPMC-112 using 9-bit asynchronous communication, and the communication speed is set by MOD1, 0. TXD is for the send output terminal, and RXD is for the receive input terminal.

### 5-4-6. Power detection input signal (VS)

This is an input signal used to detect changes in the power of the slave system. If this signal's input voltage is more than 3.5V, power is determined to be normal. When this voltage declines (logically changing from a high to a low level), an interrupt signal is sent, and the error code \$81 is issued. When the voltage returns to a normal level (logically from a low to a high level), an interrupt signal is sent again, and \$80 is issued.

### 5-4-7. RESET(RESET\*)

This signal resets the MWSC-101 to its initialization state. The power voltage needs to be within the operational range of the MWSC-101 and maintained at a high level for a period of more than 10 clocks.



## 6. *Host Interface Register*

The MWSC-101 has three different types of registers as shown in Table 9 that control the input/output of commands and data.

Table 9.

AO	CS	Read/Write	Name of Register
L	L	Read	Data Register
		Write	
H		Read	Status Register
		Write	Command Register
-	H	-	Not accessible

### 6-1. *Data Register*

This register exchanges all data with the host except for commands.

### 6-2. *Command Register*

This is the register in which the commands are written.

### 6-3. *Status Register*

The Status Register is a read-only register that indicates the internal conditions of the MWSC-101. These internal conditions can be read at any time.

#### 7-3-1. OBF (Output Buffer Full Flag)

This bit notifies the master that the MWSC-101 is ready to send data. The master checks whether or not this OBF is set to "1" before reading the data. If the OBF is set to "0", this data is voided. If the OBF is set to "1", an interrupt signal is always issued.

0 : READ possible  
1 : READ impossible

#### 6-3-1. IBF (Input Buffer Full Flag)

This bit checks whether or not the MWSC-101 is ready to receive commands or data. New data cannot be written if the IBF bit reads "1". Commands and data must be written after making certain that the IBF bit reads "0". Entry of commands or data when the IBF bit shows "1" deletes previously written commands and data.

0 : WRITE possible  
1 : WRITE impossible

### 7-3-3. SYS (System Command)

This bit is set to "1" when there is returned data from system commands. An interrupt signal is issued, the OBF is set to "1", and the returned data is written into the data register. When the host reads all of the data, this bit becomes "0", and the interrupt signal is also reset. This bit is used for the following system commands.

- \* Initialization Polling Command
- \* Emergency Stop Command
- \* Busy List Command
- \* Error Count Read Command
- \* Status Check Command

0: No Interrupt

1: There is returned data from the system command and an interrupt signal is issued.

### 6-3-2. ERR (Interrupt by Command Error)

This bit is set to "1" when there is an error in a command written by the host. An interrupt signal is issued, the OBF is set to "1", and the result is written into the data register. When the host reads all of this result, the bit becomes "0", and the interrupt signal is reset.

0 : No interrupt

1 : Command error interrupt is being issued

The slave address and the error code are read from the first byte of the result. Bit7 (MSB) of the MWSC-101's error code is always "1", but the error might be a PPMC-112 error. In this case, Bit7 is set to "0", indicating that the error is a PPMC-112 error. PPMC-112 error codes are described in Table 12 "PPMC-112 Error Codes".

7	6	5	4	3	2	1	0
0	0	0	0	Slave address			
Error Code							

Commands that cannot specify the slave address using system commands are identified by Bits 7 through 4 of the first byte of the result being set to "1".

7	6	5	4	3	2	1	0
1	1	1	1	0	0	0	0
Error Code							

Table 10 MWSC-101 Error Codes

Error Code	Description of Error
\$80	Slave power is recovered VS terminal changed from low to high
\$81	Slave power is abnormal MOD0,1 setting is abnormal. VS Terminal changed from high to low.
\$82	MOD0,1 setting is abnormal.
\$83	No devices are connected. Incorrect slave address or Initialization Polling has not been executed.
\$84	Incorrect slave address or Initialization Polling has not been executed.
\$85	Initialization Polling Command has not been executed. This error may be caused by the Polling Start, Polling Prohibit, or Polling Resume Commands.
\$86	An unprocessable command was received during polling.
\$87	Data preceded by no command code was received.
\$88	Command code was received while waiting for data.
\$89	Unable to accept command due to interlock.
\$8A	Data overflowed by a direct command. Next piece of data was received before the data register was read.
\$8B	The Interlock Release Position Setting Command was sent to the slave which does not control interlock.
\$8C	Interlock setting data error. The data length of the Interlock Configuration Command is either an odd number or outside the specified range.
\$8D	Interlock is released, but the controlled slave is not given a Start Command.

### 6-3-3. COMS (Interrupt by Communication Status)

This bit changes depending upon the status of the MOD2 pin. When the result of communication between the MWSC-101 and the slave is issued, an interrupt signal is sent and this bit is set to "1".

Table 11

MOD2	
0	Only when communication error occurs.
1	When acknowledgement is received or an error occurs.

This bit is set to "1" to report communication results a the slave. An interrupt signal is issued, the OBF is set to "1", and the result is written into the data register. When the host reads all of the result, this bit becomes "0", and the interrupt signal is also reset.

The first byte of the result is the slave address. The second byte is the result of the communication. Each bit of the communication result has a meaning, and the details are described in Table 12 "Communication Status". When the second byte is \$00, it indicates that communication has ended normally.

7	6	5	4	3	2	1	0
0	0	0	0	Slave address			
Please refer to the table for details of each bit							

Table 12. Communication Status

Bit	
7	Unable to receive (Timeout)
6	Framing error
5	Over-run error
4	Data was received during control frame reception.
3	Control frame was received during data reception.
2	Address error
1	Protocol error
0	Checksum error

Note 1 : Errors might occur repeatedly due to retries. In this case, multiple bits would be set to "1".

Note 2 : When the status is "\$00", it indicates that communication ended normally.

#### 6-3-4. INTD (Interrupt by Data)

This bit is set to "1" when the slave responds to the slave input commands given by the host, data is received by the MWSC-101, and an interrupt signal is sent. When the host reads all of the data from the data register, this bit as well as the interrupt signal are reset.

0 : No Interrupt

1 : The data receive interrupt signal is being issued

The host must read all the data from the data register. The slave address followed by the data from the slave is read from the data register. Because the data length is not read from the data register, the number of bytes to be read must be determined from the slave address and the command given.



### 6-3-5. INTR (Interrupt by End of Run or Interlock Release)

This bit reads "1" when the system is in the polling process (Polling Start Command has been issued) and the end of run is reported from the slave, or when the interlock release is reported and the interrupt signal is sent. The slave's device address followed by the end status or interlock release status is read from the data register when the OBF bit reads "1". The status consists of 1 byte and is set to "0" when the data is read from the data register by the host. The interrupt signal is also reset.

When the status shows "\$00", it indicates that the interrupt was by an interlock release. Different statuses set by end of run are described in Table 13 "INTR Status".

0 : No Interrupt

1 : End of Run, Interlock Release.

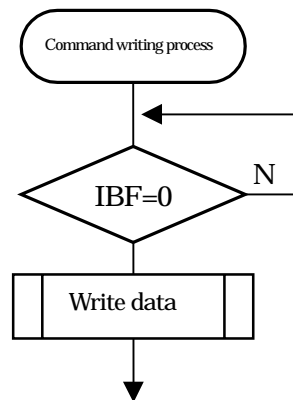
7	6	5	4	3	2	1	0
0	0	0	0	Slave address			
Please refer to the table for details of each bit							

Table 1. INTR Status

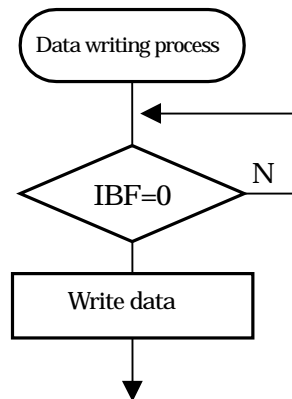
Bit	PPMC-112	SYNC-101 is connected
0	Normal completion	Normal completion
1	Stop by detection of Stop Command	Stop by detection of the Y axis origin signal
2	Origin	Stop by detection of the X axis origin signal
3	Stop by detection of the CW direction Limit signal	Stop by detection of the Y axis CCW direction Limit signal
4	Stop by detection of the CCW direction Limit signal	Stop by detection of the Y axis CW direction Limit signal
5	Decelerating stop by detection of the CW direction High Speed Limit signal	Stop by detection of the X axis CCW direction Limit signal
6	Decelerating stop by detection of the CW direction High Speed Limit signal	Stop by detection of the X axis CW direction Limit signal
7	Stop by detection of alarm signal (ALM)	Stop by detection of alarm signal (ALM)

## 7. Flow chart

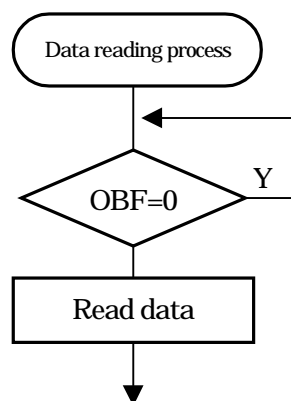
### 7-1. Command writing process



### 7-2. Data writing process

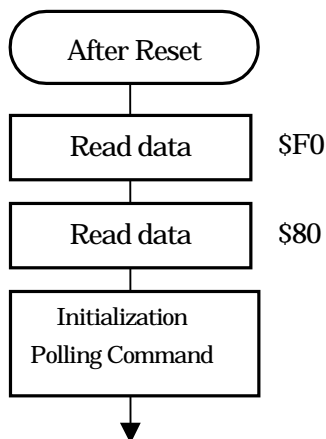


### 7-3. Data reading process



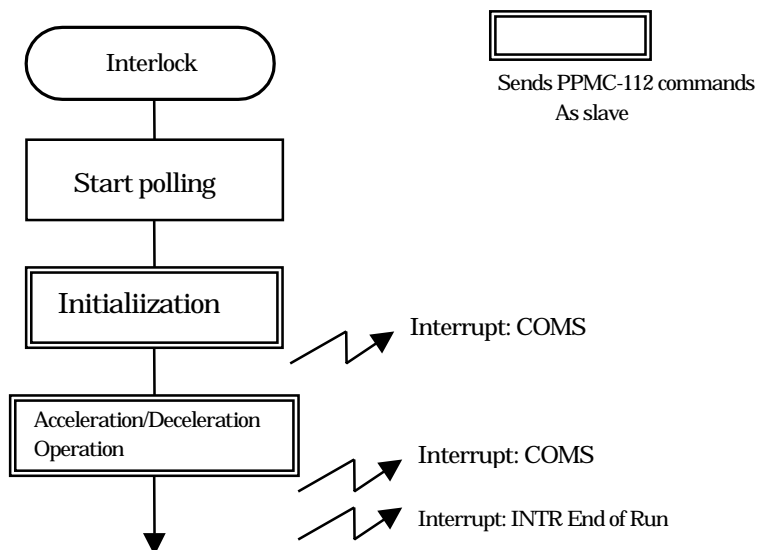
## 7-4. *After Reset*

Immediately after a reset, regardless of the use of the SV terminal, 2 bytes of data must be read from the data register. \$F0 and \$80 can be read. The Initialization Polling Command does not necessarily have to be issued immediately after a reset.



## 7-5. *Acceleration/Deceleration Operation*

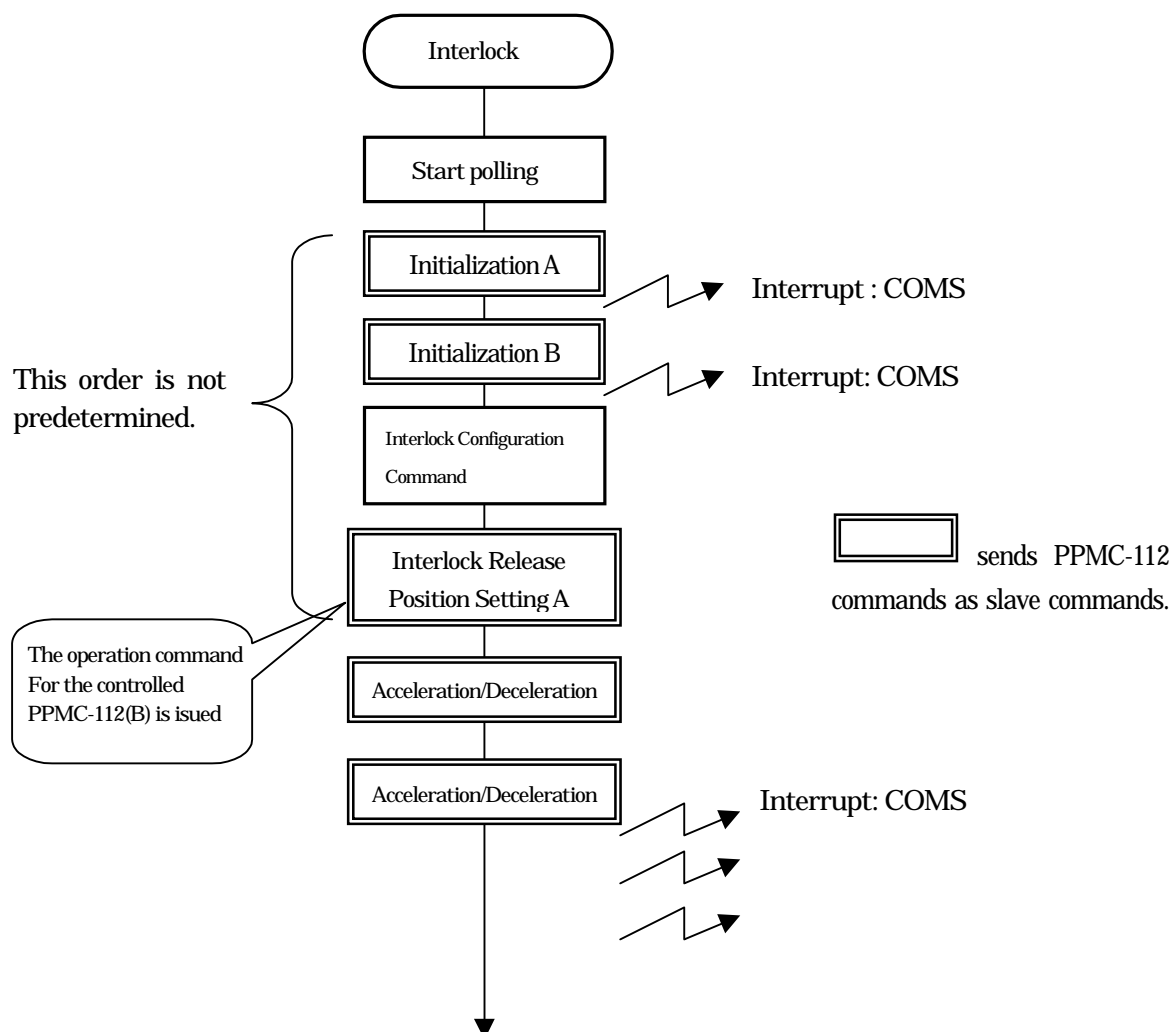
The MOD2 terminal determines the COMS interrupt signal output. The timing of the interrupt signal to indicate the end of run is determined by the number of operation pulses.





## 7-6. Interlock

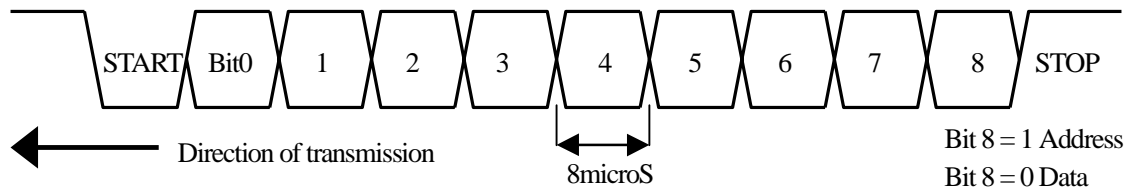
This is an example of interlocking two PPMC-112s (A and B). A is the controlling PPMC-112 and B is the controlled PPMC-112. The MOD2 terminal determines the COMS interrupt signal output. The timing of the interrupt signal to indicate the end of run is determined by the number of operation pulses.



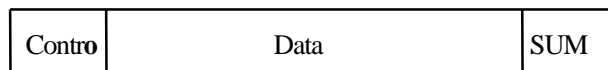
## 8. *Serial*

The MWSC-101 uses a 9-bit asynchronous UART to communicate with slaves. 8 microseconds/bit is attained at a communication speed of 125kbps.

START plus 8 bits (bits0-7) plus a controlling bit (bit 8) equals 1 field. When the controlling bit reads "1", bits 0 through 7 contain the address, and when the controlling bit reads "0", bit 0 through 7 contain data.



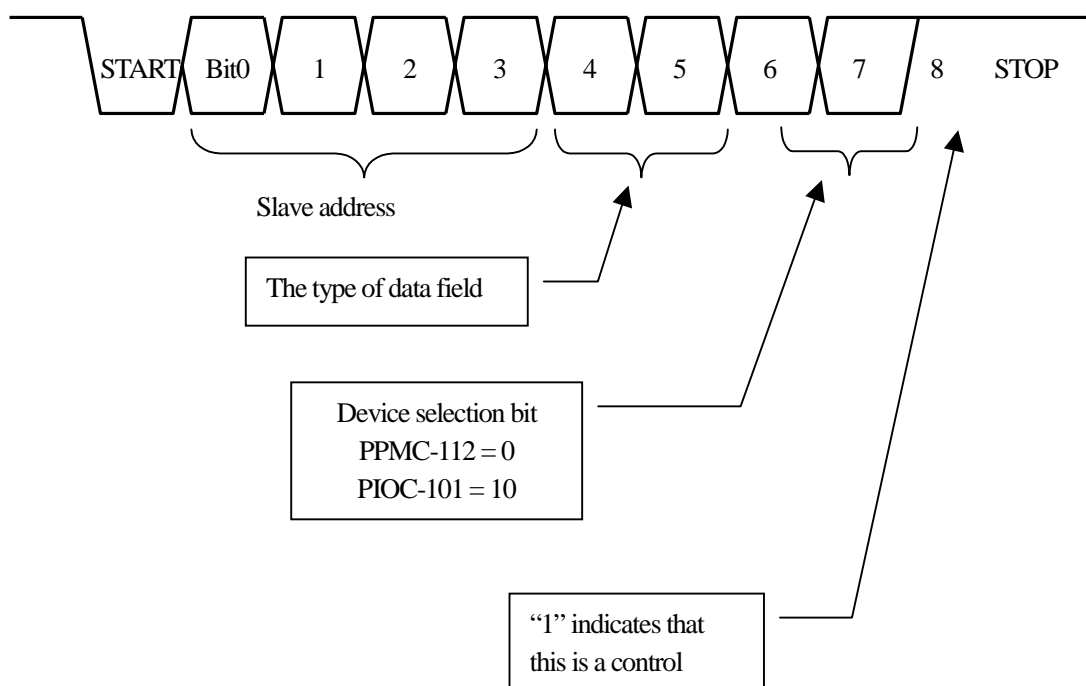
The frame sent/received by the MWSC-101 consists of three different fields: control, data, and SUM fields. There is one control field and one SUM field, but the number of data fields varies depending on the command.



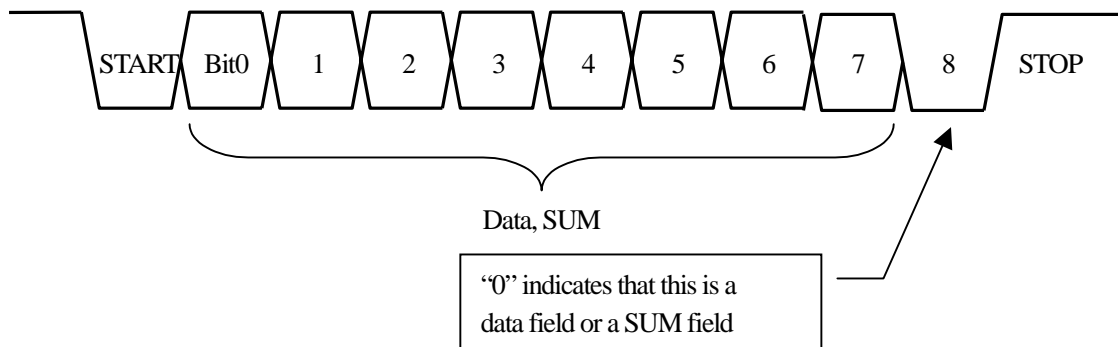
When bit 8 reads "1", it indicates it is a control field and contains the slave address and the data field type. The meaning of the data field type changes depending on whether the data was sent by the MWSC-101 or returned from the slave.

Table 14. Data Field Type

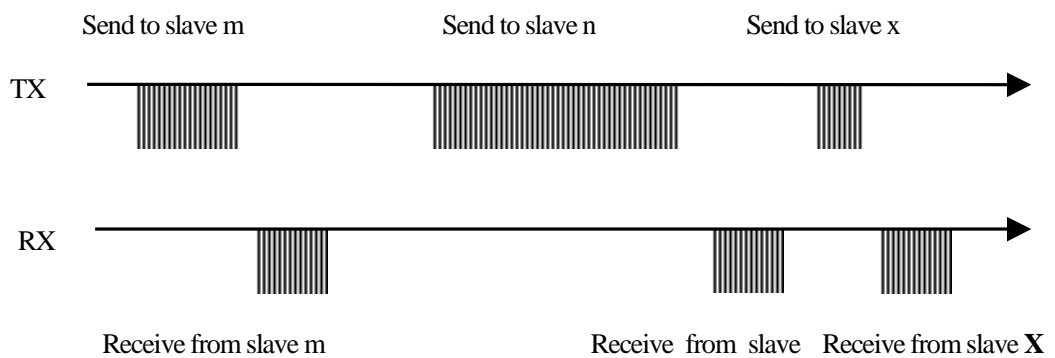
Bit 5	Bit 4	Sent by MWSC-101	Returned by the slave
0	0	Busy check field	Busy status Returned
0	1	Command data field	Acknowledge, ready returned
1	0	Not defined	Data returned
1	1	Not defined	Error, interlock returned



When Bit8 is "0", it is either the data field or the SUM field. The structures of the data and SUM fields are the same as that of the control field.



Communication between the MWSC-101 and the slave is always initiated by the MWSC-101, and the slave responds to the MWSC-101. The TX and RX of the MWSC-101 are always in pairs as shown below.



## 9. RATINGS

### 9-1. Absolute maximum ratings

The absolute ratings of **MWSC-101** are as specified in **Table 15**. Use of **MWSC-101** beyond the absolute maximum ratings may result in deterioration and permanent damage.

Table 15. Table of Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V <sub>cc</sub>	-0.5 to +6.5	V
Input voltage	V <sub>in</sub>	-0.5 to +V <sub>cc</sub> + 0.5	V
Power consumption(Ta = 85deg.C.)	P <sub>d</sub>	500	mW
Operating temperature	T <sub>opr</sub>	-40 to +85	deg.C.
Storage temperature	T <sub>stg</sub>	-65 to +150	deg.C.
Soldering temperature(10s)	T <sub>solder</sub>	260	deg.C.

### 9-2. DC Characteristics

The DC characteristics of **MWSC-101** are as shown in **Table 16**.

Table 16. Table of DC Characteristics

Item		Symbol	Min.	Max.	Unit	Condition
Low level input voltage	RESET	V <sub>IL</sub>	-0.3	0.25V <sub>cc</sub>	V	
	X1		-0.3	0.2V <sub>cc</sub>		
	Other		-0.3	0.3V <sub>cc</sub>		
High level input voltage	RESET	V <sub>IH</sub>	0.75V <sub>cc</sub>	V <sub>cc</sub> + 0.3	V	
	X1		0.8V <sub>cc</sub>	V <sub>cc</sub> + 0.3		
	Other		0.7V <sub>cc</sub>	V <sub>cc</sub> + 0.3		
Low level output voltage	All output terminals	V <sub>OL</sub>		0.45	V	I <sub>OL</sub> = 1.6mA
High level output voltage	AUXO0 - AUXO7	V <sub>OH</sub>	2.4		V	I <sub>OH</sub> = -400microA
	Other		0.75V <sub>cc</sub>			I <sub>OH</sub> = -100microA
Input current		I <sub>DR</sub>	-1.0	-3.5	mA	
Input leakage current		I <sub>LI</sub>	0.02(TYP)	-5 to +5	mA	
Output leakage current		I <sub>LO</sub>	0.05(TYP)	-10 to +10	mA	
Current consumption		I <sub>CC</sub>	35(TYP)	50	mA	
Input capacity	All input pins	C <sub>IN</sub>		10	PF	

V<sub>cc</sub>=5V -10 to +10%

Ta = -20 to +70 deg.C. (1 to 16MHz)

Ta = 25 deg.C.

V<sub>cc</sub>=5V for TYP value

The Darlington drive current is the output allowable current for driving transistors such as the Darlington transistor using an auxiliary output signal.

## 9-3. AC Characteristics

### 9-3-1. RD and WR separate bus mode (Register read operation)

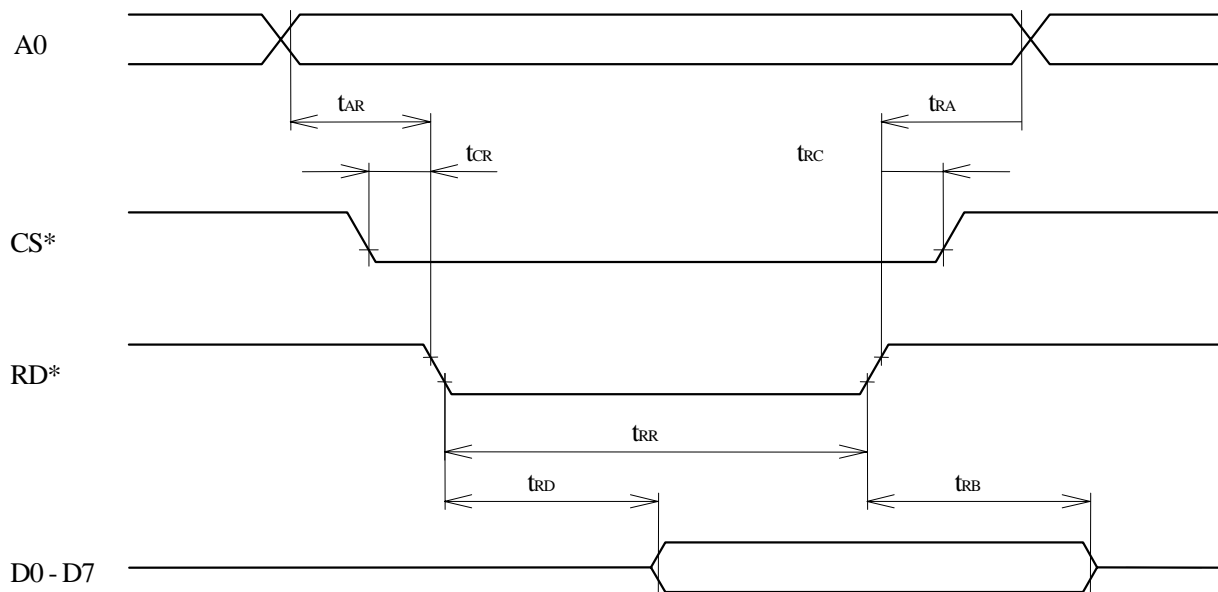


Fig.1. RD and WR Separate Bus Mode Register Read Timing

Table 17. RD and WR Separate Bus Mode Register Read Parameters

Item	Symbol	Min.	Max.	Unit
A0 set time to RD*	$t_{AR}$	20		nS
A0 hold time after RD*	$t_{RA}$	5		nS
CS* set time to RD*	$t_{CR}$	0		nS
CS* hold time after RD*	$t_{RC}$	0		nS
RD* pulse width	$t_{RR}$	120		nS
RD* to Data out delay	$t_{RD}$			nS
RD* to Data hold	$t_{RB}$	10	90	nS

( $V_{CC} = +5V -10$  to  $+10\%$ ,  $T_a = -20$  to  $+70^{\circ}\text{deg.C.}$ )

### 9-3-2. RD and WR separate bus mode (Register write operation)

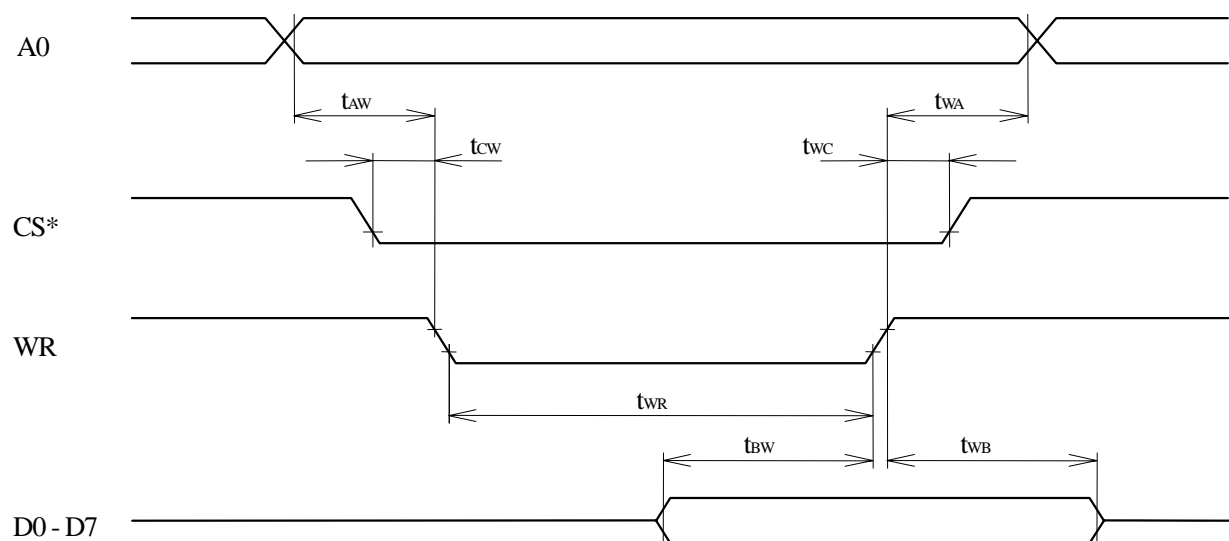


Fig.2. RD and WR Separate Bus Mode Register Write Timing

Table 18. RD and WR Separate Bus Mode Register Write Parameters

Item	Symbol	Min.	Max.	Unit
A0 set time to WR*	$t_{AW}$	20		nS
A0 hold time after WR*	$t_{WA}$	5		nS
CS* set time to WR*	$t_{CW}$	0		nS
CS* hold time after WR*	$t_{WC}$	0		nS
WR* pulse width	$t_{WR}$	120		nS
Data setup to WR*	$t_{BW}$	80		nS
Data hold time after WR*	$t_{WB}$	10		nS

( $V_{CC} = +5V -10$  to  $+10\%$ ,  $T_a = -20$  to  $+70^{\circ}\text{deg.C.}$ )

## 9-3-3. DS and R/W bus mode (Register read operation)

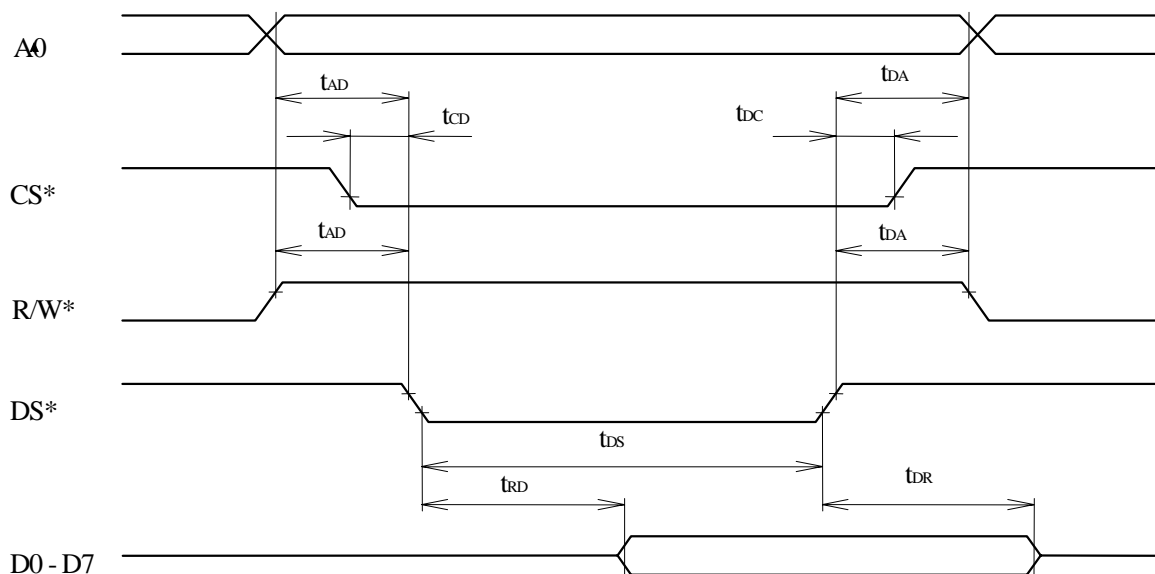


Fig.3. DS and R/W Bus Mode Register Read Timing

Table 19. DS and R/W Bus Mode Register Read Parameters

Item	Symbol	Min.	Max.	Unit
A0, R/W* set time to DS*	$T_{AD}$	20		nS
A0, R/W* hold time after DS*	$T_{DA}$	5		nS
CS* set time to DS*	$T_{CD}$	0		nS
CS* hold time after DS*	$T_{DC}$	0		nS
DS* pulse width	$T_{DS}$	120		nS
DS* to Data out delay	$T_{RD}$		100	nS
DS* to Data hold	$T_{DR}$	10	90	nS

(Vcc = +5V -10 to +10%, Ta = -20 to +70deg.C.)



### 9-3-4. DS and R/W bus mode (Register write operation)

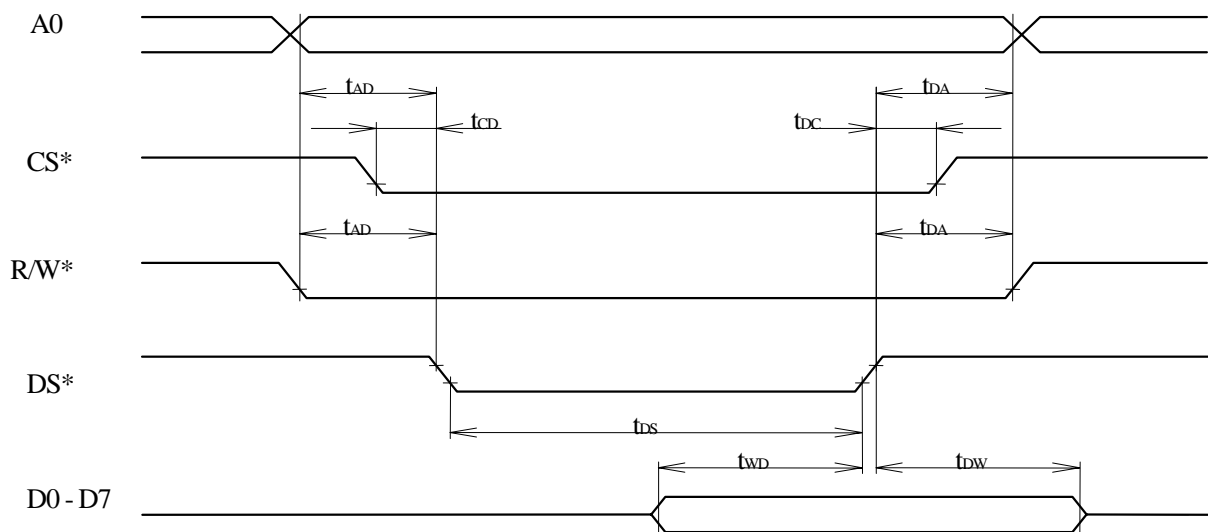


Fig.4. DS, R/W Bus Mode Register Write Timing

Table 20. DS, R/W Bus Mode Register Write Parameters

Item	Symbol	Min.	Max.	Unit
A0, R/W* set time to DS*	$t_{AD}$	20		nS
A0, R/W* hold time after DS*	$t_{DA}$	5		nS
CS* set time to DS*	$t_{CD}$	0		nS
CS* hold time after DS*	$t_{DC}$	0		nS
DS* pulse width	$t_{DS}$	120		nS
DS* to Data input delay	$t_{WD}$	80		nS
Data hold after DS*	$t_{DW}$	10		nS

( $V_{CC} = +5V -10$  to  $+10\%$ ,  $T_a = -20$  to  $+70^{\circ}\text{C}$ .)

## 9-4. Outline drawings

[Unit : mm]

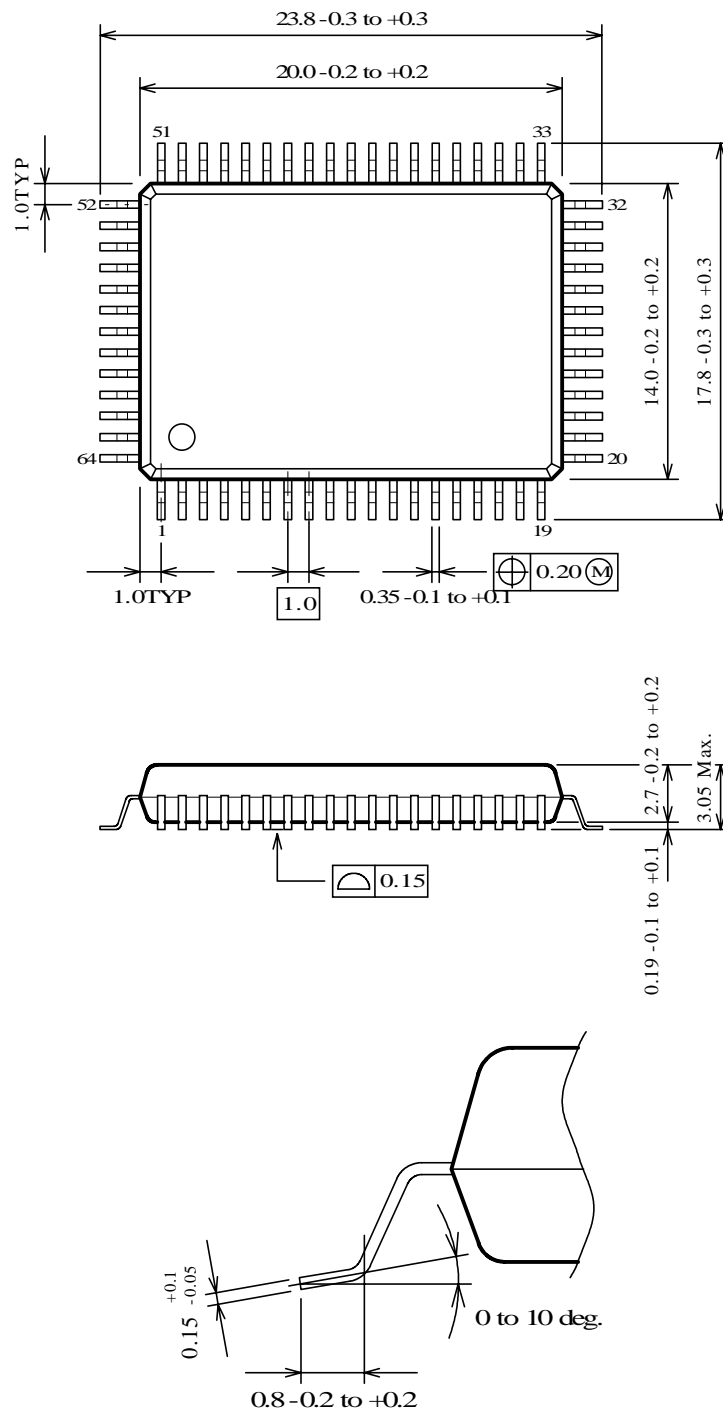


Fig.5. Outline Drawing of MWSC-101

## 10. RECOMMENDED PACKAGING CONDITIONS AND HANDLING NOTES

**MWSC-101**, which is a surface mounting type. In mounting on the printed circuit board, the biggest problems that affect the reliability of **MWSC-101** are contamination by flux and thermal stress during package soldering. Explained in this section are the recommended temperature profiles and general notes to be observed in mounting the **MWSC-101**.

### 10-1. Temperature profile

#### 10-1-1. Soldering iron

The temperature at the lead must be kept at 260deg.C. for no longer than 10 seconds or 350deg.C. for no longer than 3 seconds.

#### 10-1-2. Far and medium – infrared reflow soldering

1. Upper and lower heating by far- and medium- infrared reflow soldering is recommended.
2. The temperature must be kept at not less than 210deg.C. for 30 seconds or less while the package surface temperature must not go above 240deg.C.. A recommended temperature profile is shown in **Fig.6**.
3. Note that near – infrared reflow soldering produces stress similar to that of dip soldering.

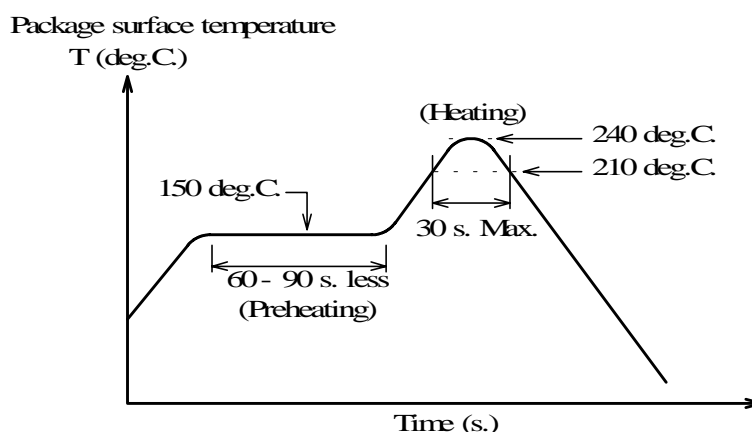


Fig.6 (Temperature Profile)

#### 10-1-3. Case of hot air reflow soldering

1. The temperature must be kept at not less than 210deg.C. for 30 seconds or less while the package surface temperature must not go above 240deg.C..
2. A recommended temperature profile is shown in **Fig.6**.

### 10-1-4. Vapor phase reflow soldering

1. The recommended solvent is Fluorinate FC-70 or the equivalent.
2. The ambient temperature must be 215deg.C. for no longer than 30 seconds or 200deg.C. for no longer than 60 seconds.
3. A recommended temperature profile for V.P.S. is shown in **Fig.7**.

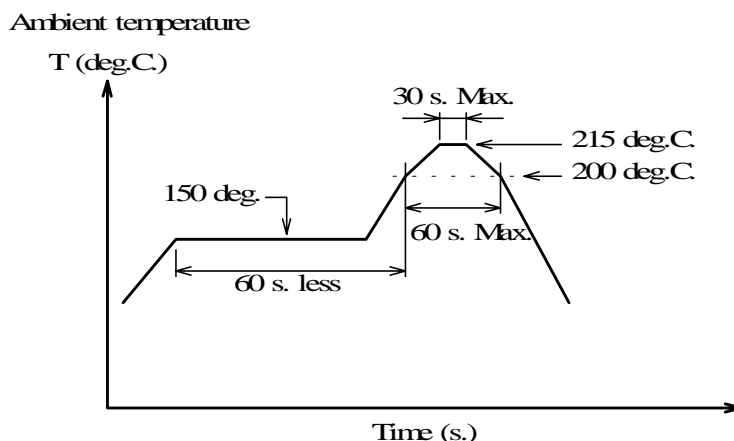


Fig.7 (Temperature Profile)

### 10-1-5. Dip soldering

1. Preheating must be done at 150deg.C. for at least 60 seconds.
2. Solder flow must be done at a maximum temperature of 260deg.C. for no longer than 10 seconds.

## 10-2. *Flux cleaning (Ultrasonic cleaning)*

1. Carry out flux cleaning in such a way that no reactive ions of Na or Cl remain. An organic solvent, if used, may react with water to produce some corrosive gas like hydrogen chloride, thus degrading **MWSC-101** package.
2. Do not rub the marking with a brush or your hand during the cleaning or with the cleaning solution still **MWSC-101**. Such careless operation may erase the marking.
3. In performing immersion cleaning, shower cleaning or steam cleaning, take great care in selecting the solvent to prevent unwanted reactions. The immersion time in solvent or steam should be 1 minute or less at a liquid temperature not exceeding 50deg.C..
4. For a highly efficient short-time ultrasonic cleaning, the following basic conditions are recommended:

Frequency	: 27kHz to 29kHz
Ultrasonic output	: 300W or below (0.25W/square cm or below)
Cleaning time	: 30 seconds or less

Perform this cleaning with the package suspended in the solvent, taking care that the ultrasonic vibrator does not come into direct with the printed circuit board or **MWSC-101**.

## 10-3. *Coating of board*

When your equipment requires high reliability or when it is used in an unfavorable environment (with humidity, corrosive gas, dust, etc.), consider the use of a damp-proof coating for the printed circuit board while taking into account the expected stress, the effect of impurities, etc.

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There are great varieties of coating resins, and selection is generally made by experience. Therefore, in selecting your coating resin, make a close study of the thermal and mechanical stresses that may act on **MWSC-101**.

## 10-4. *Degradation and breakdown by static charge*

When handling **MWSC-101** alone, do it in an environment free from static electricity and wear antistatic clothing. Also, use antistatic material for the vessel or like object with which **MWSC-101** comes into contact and ground it through a protective resistance of 0.5Mohm to 1Mohm.

### 10-4-1. Control of working environment

1. As the humidity lowers in your working environment, human bodies and insulators may be more easily charged with static electricity through friction. The recommended humidity is therefore 40 to 60% with moisture absorption by **MWSC-101** taken into consideration.
2. Ground the equipment, jigs, etc. in the work area.
3. Provide some antistatic means, such as laying a conductive mat, on the floor of the work area and ground it.
4. Place a conductive mat on the work table to disperse static electricity and ground it. Never use a metallic surface for the work table which can cause a sudden charging at low resistance when a charged **MWSC-101** is brought into contact with it.
5. Provide a VDT filter or other antistatic means on the surface of CRTs in the work area, and do not turn them on and off during operation as far as practicable. Otherwise electrical induction to **MWSC-101** may occur.
6. Cover the work chair with antistatic cloth and ground it with an earthing chain to the floor.
7. Place antistatic mats on the **MWSC-101** storage shelves.
8. Use static extinguishing material or antistatic material for the containers used for the containers used for transportation or temporary storage of **MWSC-101**.
9. Install antistatic grounding conductor in the static control area. You can also use the grounding of other machinery.
10. When automated equipment is used, observe the following instructions:  
 When the **MWSC-101** package is picked up with vacuum, provide an antistatic means, such as conductive rubber, on the end of the pickup arm.  
 Take care to minimize friction at the **MWSC-101** package surface. When friction can not be reduced structurally, make the frictional surface smaller, employ material with smaller friction coefficient or electrical resistance or use an ionizer.  
 Use a static extinguishing material for the part coming into contact with the lead terminals of **MWSC-101**.  
 Do not allow any charged body (clothing, body, etc.) to touch **MWSC-101**.  
 Do not allow the jigs used in the process to touch **MWSC-101**.

## 10-4-2. Working notes

1. Have the workers wear antistatic clothing and conductive shoes.
2. Have the workers wear wrist straps which are grounded through a resistance of about 1Mohm.
3. Use a low – voltage type soldering iron and ground the end of it.
4. Use antistatic pincers that may come into contact with the lead terminals of **MWSC-101**, and avoid use of metallic pincers as far as practicable. Otherwise the charged **MWSC-101** may discharge suddenly at low resistance. When you use vacuum pincers, make certain that they have a conductive suction pad at the end are grounded by antistatic earthing conductor.
5. Do not place **MWSC-101s** and their containers close to object with strong electrical fields (e.g.,CRT).
6. Place printed circuit boards with **MWSC-101s** on separate from each other in antistatic board containers. Also do not stack them touching each other. Frictional charging and discharging may occur.
7. Put on antistatic finger sacks or gloves as far as practicable when you have to touch **MWSC-101** directly.
8. Use an ionizer when wrist straps are not available or when **MWSC-101** is subject to friction.

## 10-5. *Requirements for service environment*

### 10-5-1. Temperature environment

Generally speaking, semiconductor parts are more sensitive to temperature than other component parts. Since electrical characteristics can be restricted by operating temperatures, your design must take into account the temperature characteristics involved. Exceeding the specified operating temperature range may not only result in the loss of specified electric characteristics but also quicken the deterioration of **MWSC-101** and shorten its life.

### 10-5-2. Humidity environment

**MWSC-101** is molded and thus does not provide perfect airtightness. Use in a high – humidity environment over a long period may allow the entry of moisture, which in turn may cause degradation and other troubles with the semiconductor chips inside. Therefore, apply a moisture – proof treatment to the surface of **MWSC-101**. In a low – humidity environment, damage may result from discharging of static electricity, so make certain that the humidity is in a range of 40 to 60% unless you take some antistatic measures.

### 10-5-3. Corrosive gas

**MWSC-101** can react to some corrosive gases and suffer a drop in performance. For example, sulfuric gas from rubber near **MWSC-101** may corrode the lead terminals or cause a chemical reaction between lead terminals, thus forming foreign material there that will eventually cause leaks.

### 10-5-4. Radioactive rays / Cosmic rays

**MWSC-101** is not designed for use with radioactive rays or cosmic rays. When it is used on space equipment or in an environment with radiation, it must be provided with a shield against the radioactive or cosmic rays.

### 10-5-5. Strong electrical field / Strong magnetic field

If exposed to a strong electric field, the **MWSC-101** may develop abnormal phenomena, such as change in impedance or increase of leakage current, due to polarization inside its plastic materials or IC chips. In such applications, therefore, you need to provide a shield against the electric field / magnetic field. Especially in an AC magnetic environment, an appropriate magnetic shield must be installed against the electromotive force.

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## 10-5-6. Vibration / Shock / Stress

The plastic- sealed **MWSC-101** has wire connections locked with resin inside, so that its structure has fairly strong resistance to vibration and shocks. In actually, however, there can be cases of disconnection with vibration, shock or stress loosening the soldered parts. Therefore, do not use **MWSC-101** in equipment exposed to heavy vibration. Also, stress that bears on the semiconductor chips through the package may cause changes in resistance inside the chip due to a piezo- electric effect. Strong vibration, shock or stress may even crack the package or chips.

## 10-5-7. Dust / Oil

As with corrosive gas, **MWSC-101** can react chemically with dust or oil. Therefore, do not use **MWSC-101** in an environment where it may be exposed to dust or oil, which is capable of affecting its performance adversely.

## 10-5-8. Smoking / Ignition

**MWSC-101** is not incombustible, so it can smoke or burn, emitting toxic gas in the process. Therefore, do not use it near fire or other heat sources, ignitable or flammable substances.

# 10-6. *Requirements for design*

Observe the specified maximum ratings and recommended operating conditions for **MWSC-101** so that it can achieve its design reliability for your system. Also, pay attention to such environmental conditions as ambient temperature, transient noise and surge to maximize the performance of **MWSC-101**.

## 10-6-1. Observance of maximum ratings

A maximum rating is a standard which must never be exceeded. This applies to all of the maximum ratings. There are maximum ratings for the voltage and current at individual lead terminals, the storage temperature, the lead terminal temperature, etc.

If the voltage or current at any of the lead terminals rises above the maximum ratings, the **MWSC-101** may suffer degradation due to overvoltage or overcurrent. In extreme cases, wire may melt away or the semiconductor chip may break down from heat generated inside the internal circuit.

If the storage temperature or soldering temperature exceeds the rating, the differences in the coefficient of thermal expansion between materials in the **MWSC-101** may cause the failure of airtightness or the opening of bonded joints.

## 10-6-2. Observance of guaranteed operation range

The recommended operating conditions guarantee the performance of **MWSC-101**.

## 10-6-3. Setting of unused I/O terminals

Unstable input may sometimes result from the use of **MWSC-101** with unused input terminals in the open state. Also, output terminals must not be connected to the supply voltage (Vcc) or other output terminals.

As **MWSC-101** with unused input terminals in the open state may be affected by external noise more easily and cause unstable operation, the input terminals should be pulled up to power supply (Vcc) or connected to the ground (GND) according to their functions.

## 10-6-4. Latch-Up

As **MWSC-101** has a CMOS structure, a latch-up, in which a breakdown results from a large current of several hundred mA flowing between Vcc GND, can occur.

A latch-up occurs when a large current flows to the internal elements as a result of an input/output voltage exceeding the rating. In this case, even if the voltage above the rating is instantaneous, the **MWSC-101** in a latch-up condition may retain the large current between Vcc and GND, thus causing heating or smoking. Therefore, be sure to observe the following instructions:

1. Do not raise the voltage at the I/O terminals above Vcc, and do not lower it below GND. The machine must be switched at a proper timing.
2. Do not allow abnormal noise to act on **MWSC-101**.
3. Fix the unused input terminals to Vcc or GND.
4. Do not short the output terminals together

### 10-6-5. Input/Output protection

Never use a wired logic connection, in which output terminals are interconnected, for **MWSC-101**, because it will short the outputs. Also, do not connect the output terminals directly to Vcc or GND.

### 10-6-6. Interface

When a device with I/O signals to **MWSC-101** is to be connected to **MWSC-101**, malfunction may result if there is disagreement in the levels of input  $V_{IL}/V_{IH}$  and output  $V_{OL}/V_{OH}$ .

### 10-6-7. External noise

When the signals lines of I/O signals to **MWSC-101** mounted on a printed circuit board are long, noise or a surge applied to **MWSC-101** from outside may cause malfunction or breakdown due to the overcurrent (overvoltage). Lower the signal line impedance or provide a noise removing circuit as protection against external noise. Also provide appropriate protective means against surges.

### 10-6-8. Other requirements

1. When designing your system, make certain that all fail-safe means are provided and aging and other necessary treatments are done on the component parts.
2. Do not place **MWSC-101** in a place with strong electric fields; otherwise charge-up may cause surface leaks and eventual malfunction. In such applications, protect the package surface with a conductive shield plate.
3. Make arrangement so that if some conductive material (metal pin, etc.) should drop onto the terminal of the **MWSC-101** on the board, it will not cause short-circuiting.
4. **MWSC-101** is not designed for use with systems whose failure or malfunction can directly threaten the lives of people or cause injuries to them (nuclear control, aircraft and space equipment, transportation equipment, combustion control, safety devices, etc.).

If you apply **MWSC-101** to such systems, Ampere shall not be held responsible for any damages caused by such unwarranted use.



## 11. PPMC-112 ERROR CODES

Table 21 PPMC-112. Error codes

Err Code	Description
\$00	No error
\$01	Undefined command error
\$02	Initiation command not executed
\$03	Limit or alarm prevents operation
\$04	The amount moved is zero and does not operate.
\$05	Stop, Decelerating stop, and Speed Change Commands are received while stopped.
\$06	Data preceded by no command code was received.
\$07	None (not assigned)
\$08	On the origin following the origin search command and cannot operate.
\$09	Unprocessable command was received when busy.
\$0A	Abnormal initialization rate data (HR < 8 or LR < 25) or abnormal initialization rate when free curve acceleration/deceleration method is used.
\$0B	Number of initialization pulses too small.
\$0C	Abnormal initialization rate data (RH > RL)
\$0D	Number of acceleration/deceleration steps for the initialization command is abnormal.
\$0E	Speed Change Command was received during deceleration by limit detection.
\$0F	Decelerating stop Command was received during deceleration.
\$10	Speed outside the speed range was specified. (> RL, < RH)
\$11	Pulse width setting is 0 or larger than pulse cycle at high speed.
\$12	Interlock setting value is too small to control. (< 50)
\$13	None (not assigned)
\$14	The speed range is outside the acceleration/deceleration range and acceleration or deceleration is not possible.
\$15	SYNC-101 control data error
\$16	Checksum error
\$17	Communication hardware error