Instruction Manual
of
Macro 5612

PPMC-312PCI Bus Module

Rev.1.0

ampère

Revision Block

REV	DATE	DETAILS	PERSON RESPONSIBLE	PERSON IN CHARGE
1.0	2001/7/21	First printing	Shohji	Saito

Contents

1. Outline

Macro5612(M5612) serves as a stepping motion contol module, conforming to PCI bus. Use of this module enables control of 4-axis (#0~#3) stepping motors.

2. Specifications

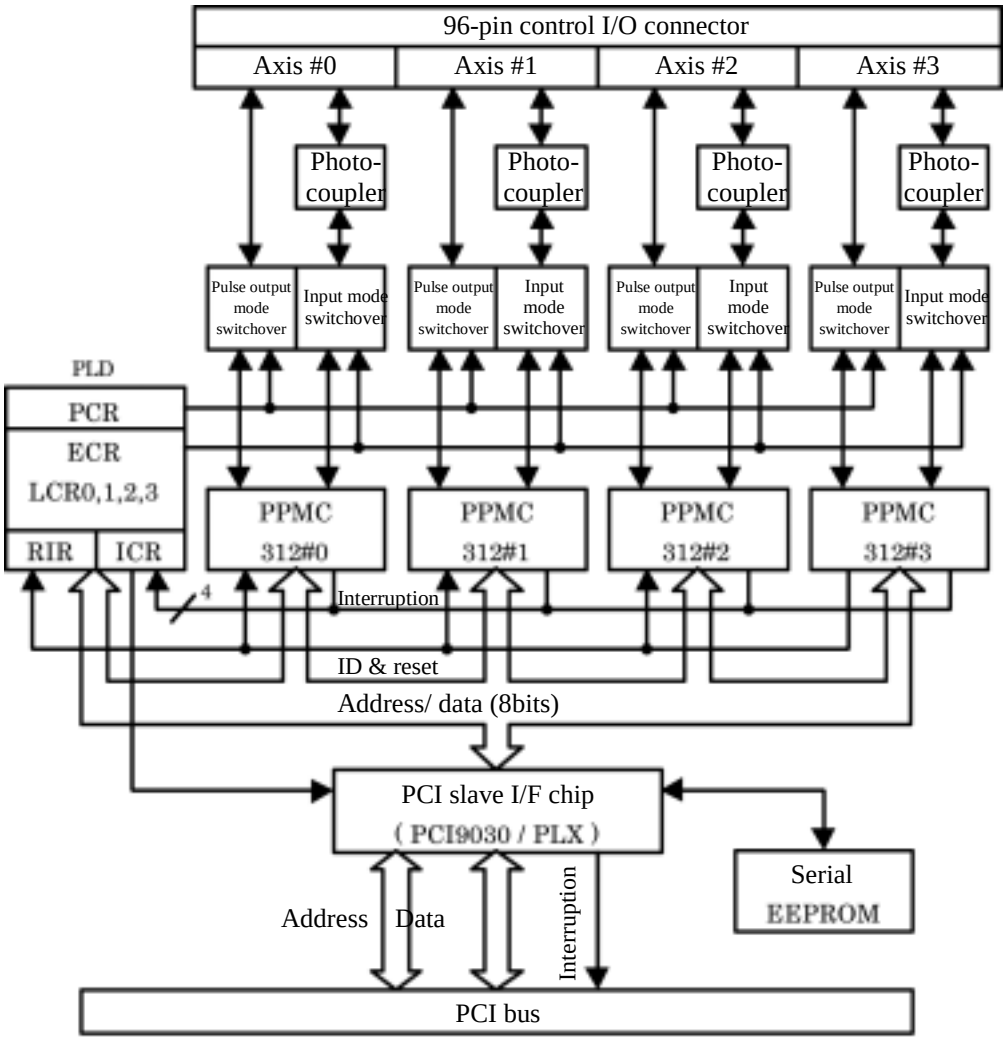
Table 2-1 List of Specifications

Controller	PPMC-312 (made by Ampere) × 4
Applicable motor driver	Servomotor driver, Stepping motor driver
Host-side interface	PCI Rev.2.2 (PCI9030 made by PLX is used.)
Memory space, I/O space	256 bytes of memory space for PI9030 configuration 64 bytes of I/O space for M5612
Interruption	1 level
Motor driver-side interface	CW*,CCW* or POUT*,DIR*,PHA,PHB,PHC ORG,FL,BL,FHL,BHL,ALM,END,EXON,ACLR,ACLMP
Connector	PCR-E96LMDC (Honda Tsushin Kogyo Co., Ltd.)
Power supply	DC+5V±5%
Consumption current	5V(PCI bus) 1A(max)
Operating conditions	Temperature 0~60°C Humidity 30~85% Ambient atmosphere Atmospheric air not containing corrosive gas
Substrate size	258W × 105.0H × 24.0T mm

Table 2-2 Cable-Side Connector

Cable-side connector (Not supplied)	You are requested to select from the following: Connector: PCR-E96F series (Honda Tsushin Kogyo Co.) Connector cover: PCS-E96 series (Honda Tsushin Kogyo Co.)

3. Block Diagram



* Correspondence of the PPMC-312 with the M5612's 4 axes is shown in Table 3-1.

Fig. 3-1 M5612 Block Diagram

Table 3-1 Correspondence Table of PPMC ⇔ M5612 Axes

PPMC-312	M5612 Axis No.	Connector Signal Name
PPMC-312#0 (Abbreviation)	Axis #0	CW0 ±, CCW0±, FL0, BL0, ORG0, FHL0, BHL0, END0 PHA0±, PHB0±, PHC0±, ACLR0, ZCLMP0, EXON0
PPMC-312#1 (Abbreviation)	Axis #1	CW1 ±, CCW1±, FL1, BL1, ORG1, FHL1, BHL1, END1 PHA1±, PHB1±, PHC1±, ACLR1, ZCLMP1, EXON1
PPMC-312#2 (Abbreviation)	Axis #2	CW2 ±, CCW2±, FL2, BL2, ORG2, FHL2, BHL2, END2 PHA2±, PHB2±, PHC2±, ACLR2, ZCLMP2, EXON2
PPMC-312#3 (Abbreviation)	Axis #3	CW3 ±, CCW3±, FL3, BL3, ORG3, FHL3, BHL3, END3 PHA3±, PHB3±, PHC3±, ACLR3, ZCLMP3, EXON3

4. Switch and Jumper Layout Drawing

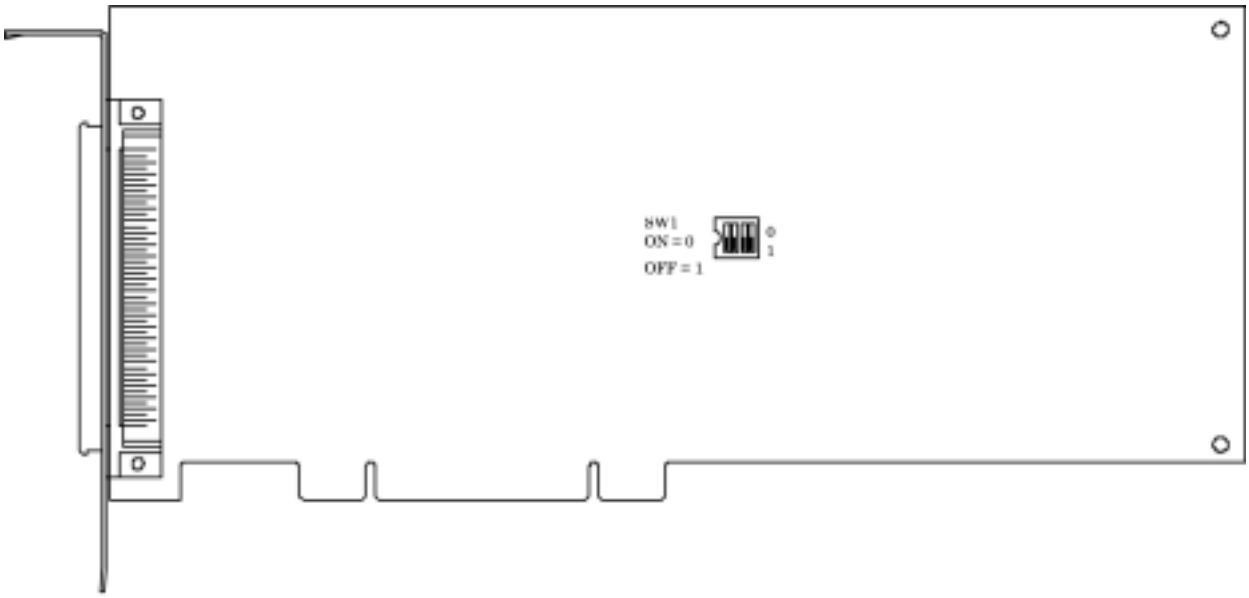


Fig. 4-1 Outside Drawing of Board

5. Memory Map

5.1 PCI Configuration Register

This configuration register conforms to the PCI standards.

Vendor ID is "172 Ch" and Device ID "5612h".

Using the PCIREV register of the PCI configuration register, you can confirm a board revision.

5.2 Local Configuration Register

This register consists of a group of registers which serve to set PCI9030 operation.

Their addresses are determined by PCIBAR0 inside the PCI configuration register.

The local configuration register is mapped in the memory space, which occupies 256 bytes.

In order to use this board, setting of or accessing to the local configuration register is not necessary. As a matter of fact, changing a value carelessly can destroy contents of the serial EEPROM for initialization of this board. Fully pay attention, therefore, when you are changing the value. Table 12-1 shows a list of setting of the serial EEPROM. Use this to return setting to the original after changing it.

As for details of PC19030, refer to the PC19030 Data Book.

5.3 Local I/O

An address of this space is determined by PCIBAR2 inside the PCI configuration register. This space is used for accessing to the PPMC-312, for resetting control of the chips, etc. As for details of PPMC-312, Instruction Manual.

Table 5-1 Local I/O Map (1/2)

Base Address	R/W	Bit 7 Bit 0
+00	R/W	PPMC#0 CSR (Control/status)
+01	-	Inaccessible
+02	R/W	PPMC#0 RCR/WCR (Write/read control)
+03	R/W	PPMC#0 RAR/WAR (Write/read size)
+04	-	Inaccessible
+05	W	PPMC#0 DWR (Instruction/data write)
+06	-	Inaccessible
+07	R	PPMC#0 DRR (Instruction/data read)
+08	R/W	PPMC#1 CSR (Control/status)
+09	-	Inaccessible
+0A	R/W	PPMC#1 RCR/WCR (Write/read control)
+0B	R/W	PPMC#1 RAR/WAR (Write/read size)
+0C	-	Inaccessible
+0D	W	PPMC#1 DWR (Instruction/data write)
+0E	-	Inaccessible
+0F	R	PPMC#1 DRR (Instruction/data read)
+10	R/W	PPMC#2 CSR (Control/status)
+11	-	Inaccessible
+12	R/W	PPMC#2 RCR/WCR (Write/read control)
+13	R/W	PPMC#2 RAR/WAR (Write/read size)
+14	-	Inaccessible
+15	W	PPMC#2 DWR (Instruction/data write)
+16	-	Inaccessible
+17	R	PPMC#2 DRR (Instruction/data read)
+18	R/W	PPMC#3 CSR (Control/status)
+19	-	Inaccessible
+1A	R/W	PPMC#3 RCR/WCR (Write/read control)
+1B	R/W	PPMC#3 RAR/WAR (Write/read size)
+1C	-	Inaccessible
+1D	W	PPMC#3 DWR (Instruction/data write)
+1E	-	Inaccessible
+1F	R	PPMC#3 DRR (Instruction/data read)

Table 5-1 Local I/O Map (2/2)

Base Address	R/W	Bit 7 Bit 0
+20	R/W	ICR (Interruption control register)
+21	R/W	RIR (Reset & ID register)
+22	R/W	ECR (Encoder input control register)
+23	R/W	LCR0 (Axis #0 limit control register)
+24	R/W	LCR1 (Axis #1 limit control register)
+25	R/W	LCR2 (Axis #2 limit control register)
+26	R/W	LCR3 (Axis #3 limit control register)
+27	R/W	PCR (Pulse output control register)
+28~3F	-	reserved

5.3.1 PPMC-312 Data and Command/Status Registers (PPMC#0-PPMC#3)

Each of the four PPMC-312 registers is accessible.

Registers of the PPMC-312 include CSR, RCR/WCR, RAR/WAR, DWR, and DDR. As for details, refer to the PPMC-312 Instruction Manual.

5.3.2 Interruption Control Register (ICR)

The interruption control register serves to control interruptions from the four PPMC-312 each individually.

BIT0-3 are the interruption mask registers. They can inhibit interruptions from PPMC-312 each individually. The register enables read/write, where the four PPMC-312 statuses are each assigned to BIT0-3. With "0", interruption is authorized and, with "1", it is inhibited. BIT3-0 are held "1" in power ON status, during which interruption is inhibited.

BIT4-7 are interruption status registers. Interruption statuses from PPMC-312 are each assigned to them, which can be monitored. With "0", interruption does not exist and, with "1", occurrence of interruption is indicated.

Table 5-2 Interruption Control Register

Bit	7	6	5	4	3	2	1	0
Function	PPMC#3 Interruption status	PPMC#2 Interruption status	PPMC#1 Interruption status	PPMC#0 Interruption status	PPMC#3 Interruption inhibit	PPMC#2 Interruption inhibit	PPMC#1 Interruption inhibit	PPMC#0 Interruption inhibit
R/W	R	R	R	R	R/W	R/W	R/W	R/W

5.3.3 Reset & ID Register (RIR)

Resetting is controlled with BIT7 of the reset & ID register. With BIT5/6, ID value status on the substrate can be monitored. ID values are used for identification when two or more boards are mounted on a PC.

BIT7 is used for resetting control of four PPMC-312 statuses. This is readable/writable. With "0", resetting is released and, with "1", resetting status is created. On supply of power, it is set in "1" where resetting status is maintained. This bit does not affect other ICR, LCR, ECR, and PCR.

BIT5/6 are read only, for which write is invalid. ID value status of "0" indicates ON status while "1" indicates OFF status. (See Chapter 6.)

BIT0-4 are reserved. Ignore the read value. The write value is "1". (Writing "0" does not make any problem. They are to retain future compatibility of software operation when the bits are expanded.)

Table 5-3 Rest & ID Register

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Function	Reset	ID1	ID0	reserved				
R/W	R/W	R	R					

5.3.4 Encoder Input Control Register (ECR)

This register serves to set an encoder pulse magnification for 90° phase which is input in each axis. Setting of x 1, x 2, and x 3 is usable for each axis. As for count examples of each magnification, refer to Fig. 5-1.

BIT1/0 represent EMOD1/0 of Axis #0.

BIT3/2 represent EMOD 1/0 of Axis #1.

BIT5/4 represent EMOD 1/0 of Axis #2.

BIT7/6 represent EMOD 1/0 of Axis #3.

For each axis, when (EMOD1, EMOD0) is (1,1), (1,0), and (0,1), it represents x1, x2, and x4 respectively. With (0,0) setting, no counting is performed.

All the registers are both readable and writable. On supply of power, all the bits are held in "1", where all the axes are set in x1.

Table 5-4 Encoder Input Control Register

Bit	7	6	5	4	3	2	1	0
Function	PPMC#3 EMOD1	PPMC#3 EMOD0	PPMC#2 EMOD1	PPMC#2 EMOD0	PPMC#1 EMOD1	PPMC#1 EMOD0	PPMC#0 EMOD1	PPMC#0 EMOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Example of Counting:

Counting includes intersecting points of the chart below of PHA/PHB, the PHA lead phase as CW, and the delay phase as CCW.

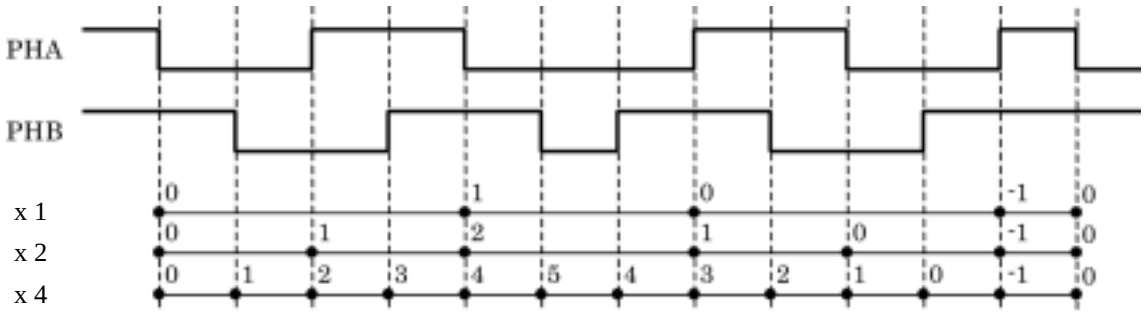


Fig. 5-1 Example of 90° Phase Difference Pulse Count

5.3.5 Limit Control Registers 0~3 (LCR0~3)

This register serves to set the input logics of FL, BL, FHL, BHL, ORG, and ALM among the signal lines which are input in each axis.

BIT0~5 are each assigned to FL, BL, FHL, BHL, ORG, and ALM for each axis. For each bit, "1" creates positive logic (with photocoupler ON, signal input) and "0" creates negative logic (with photocoupler OFF, input signal). On supply of power, each bit of each axis is held in "1" or the positive logic. BIT0~5 of each axis register are both readable and writable.

BIT0-4 are reserved. Ignore the read value. The write value is "1". (Writing "0" does not make any problem. They are to retain future compatibility of software operation when the bits are expanded.)

Table 5-5 Limit Control Register

Bit	7	6	5	4	3	2	1	0
Function	reserved	reserved	PPMC#x ALM	PPMC#x ORG	PPMC#x BHL	PPMC#x FHL	PPMC#x BL	PPMC#x FL
R/W			R/W	R/W	R/W	R/W	R/W	R/W

5.3.6 Pulse Output Control Register (PCR)

BIT4-7 registers serve to set a pulse output method for output from each axis. With "1", CW/CCW method is set. With "0", POUT/DIR method is set. As for each output method, see Fig. 5-2. On supply of power, each bit is held in "1" and it is CW/CCW method. Each bit is both readable and writable.

BIT0-3 are reserved. Ignore the read value. The write value is "1". (Writing "0" does not make any problem. They are to retain future compatibility of software operation when the bits are expanded.)

Table 5-6 Pulse Output Control Register

Bit	7	6	5	4	3	2	1	0
Function	PPMC#3 PMOD	PPMC#2 PMOD	PPMC#1 PMOD	PPMC#0 PMOD	reserved	reserved	reserved	reserved
R/W	R/W	R/W	R/W	R/W				

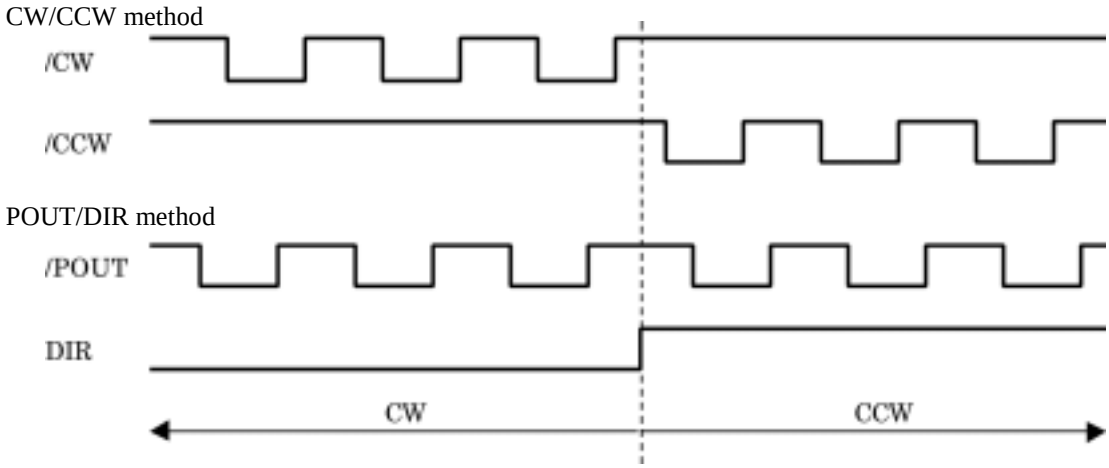


Fig. 5-2 Waveform Diagram of Pulse Output in Each Method

The output pulse is in negative logic pulse of the pulse width of 50%.

6. Dip Switch

With the dip switch SW1, an ID value is set.

ID0 and ID1 can be monitored with the reset & ID register, where "0" is read out with ON and "1" with OFF. RSV denotes RSV. Maintain them in OFF.

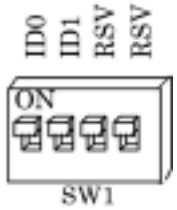


Fig. 6-1 Dip Switch SW

Table 6-1 Dip Switch SW1 Function Correspondence Table

Bit	Bit name	ON	OFF	Setting on shipment
0	ID0	RIR BIT0 = “0”	RIR BIT0 = “1”	OFF
1	ID1	RIR BIT1 = “0”	RIR BIT1 = “1”	OFF
2	RSV	-	-	OFF
3	RSV	-	-	OFF

7. Interruption

M5612 outputs interruption in the INT A# on the PCI bus.

As each PPMC-312 issues interruption individually inside a substrate, there exist four interruptions. However, as there is only one interruption line requested to the PCI bus, each PPMC-312 interruption on a substrate is subject to OR operation, output is made in the PCI bus.

In order to identify which PPMC-312 is requesting an interruption, the interruption control register (ICR BIT7-4) is read. Through this, the PPMC-312 with occurrence of an interruption can be identified.

Interruption can mask PPMC-312 each individually. For masking, set the corresponding bit of the interruption control register (ICR BIT3-0). Although it is possible to individually mask the control/status register (CSR) of each PPMC-312, interruptions are masked regardless of CSR status.

The PPMC-312 outputs two interruptions including "instruction writable" and "response report". Whether these two interruptions are usable or not can be individually set with CSR. As for details, see the PPMC-312 Instruction Manual.

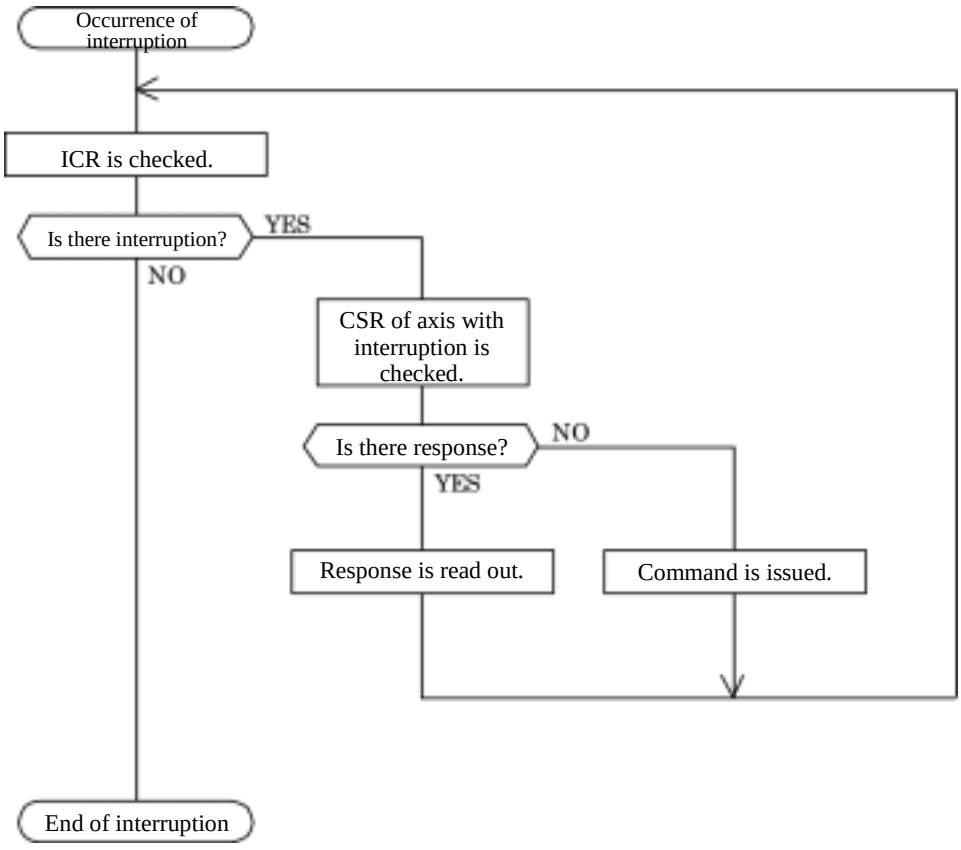


Fig. 7-1 Flow Diagram for Processing Within All-Interruption Processing

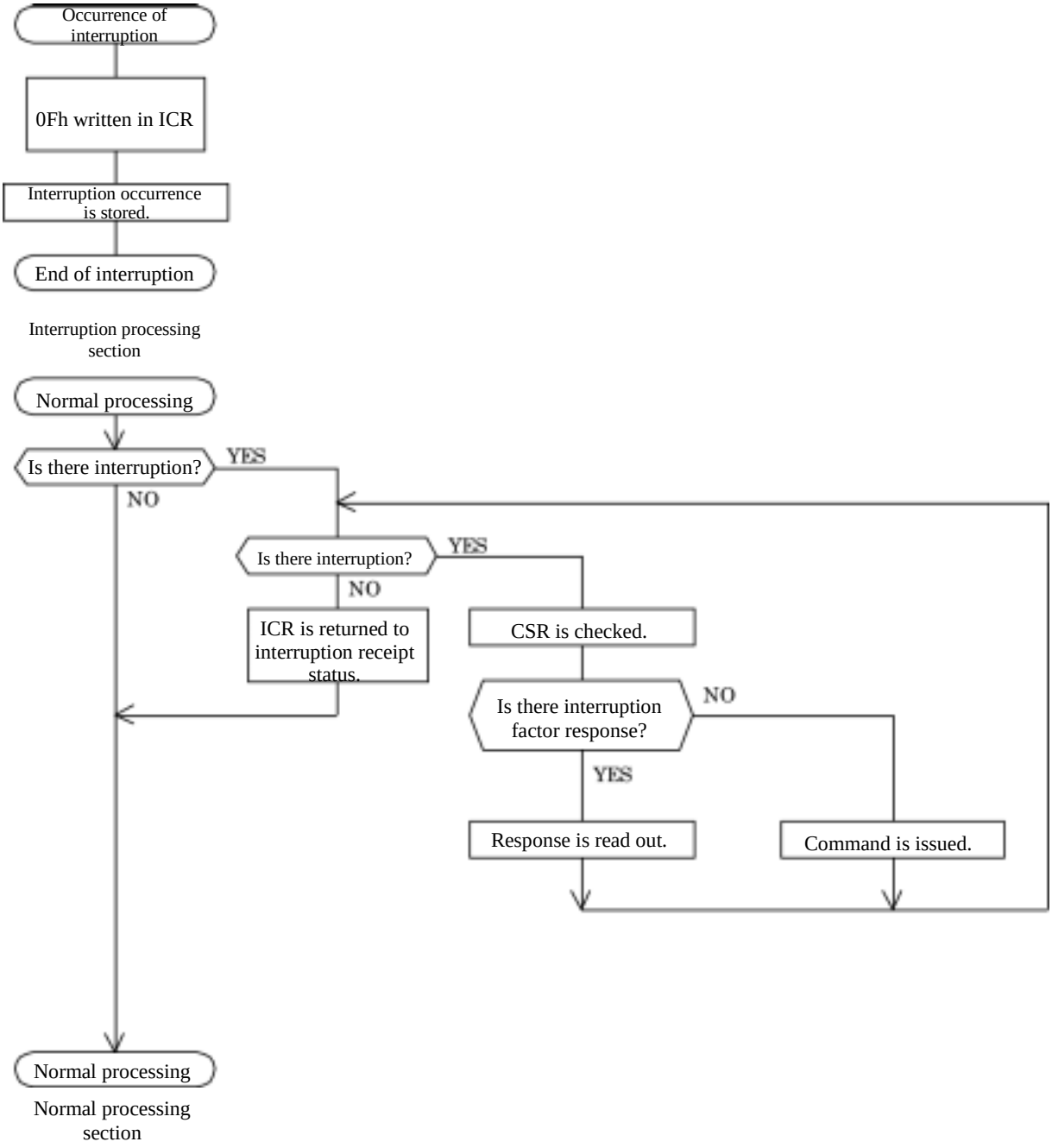
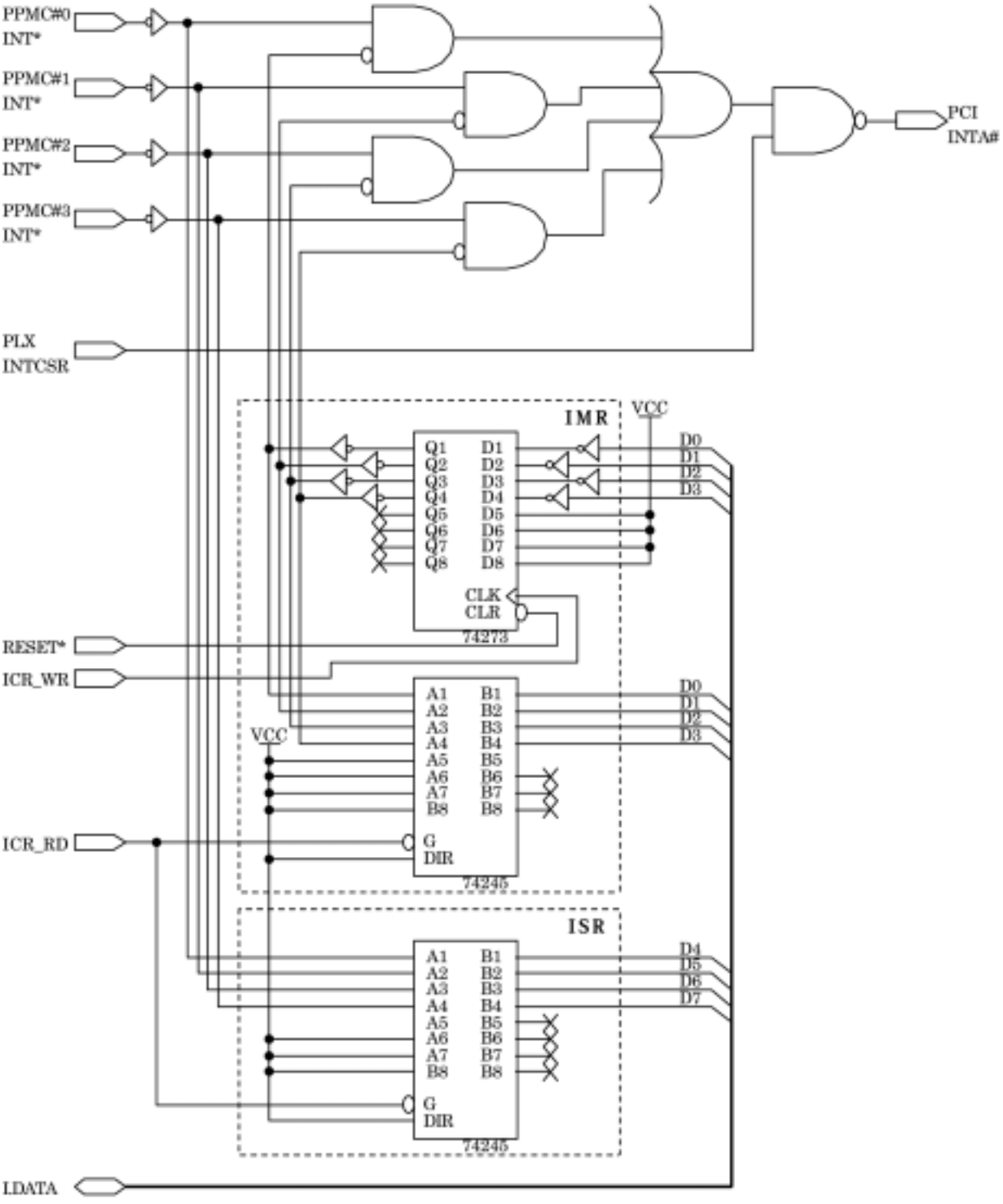


Fig. 7-2 Flow Diagram for Clearing Interruption Factor in Normal Processing



IMR: ICR BIT3-0 (Interruption mask registers)
ISR: ICR BIT7-4 (Interruption status registers)

Fig. 7-3 Interruption Logic Diagram (ICR)

8. Interface Signals

8.1 Pulse Output Interface

Pulse output takes the form of differential driver output (equivalent to AM26LS31) of non-insulated type. Pulse output logic is negative. Carry out driver connection as referring to the drawings below. In Fig. 8-1, on stoppage, the driver-side photocoupler becomes ON. In Fig. 8-2, on stoppage, the driver-side photocoupler becomes OFF.

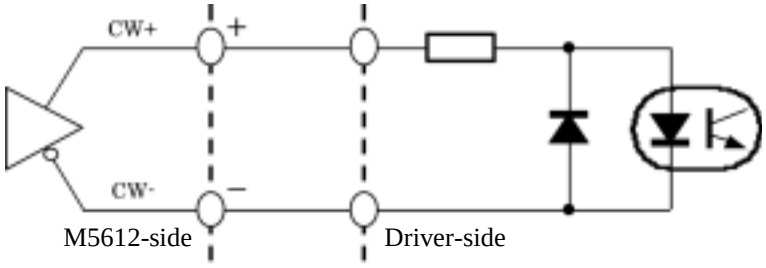


Fig. 8-1 Pulse Output Connection Example 1

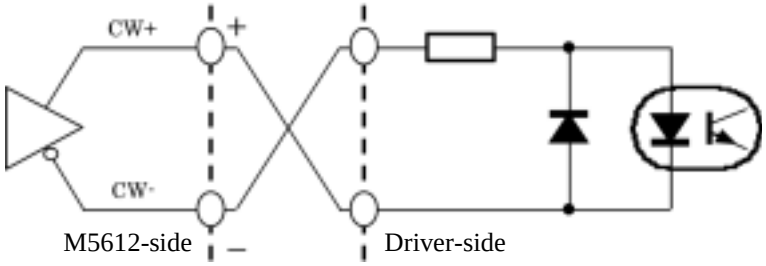


Fig. 8-2 Pulse Output Connection Example 2

8.2 Control Output Interface

Control output is provided with insulation with the photocoupler. The output photocoupler is turned ON when signals are output.

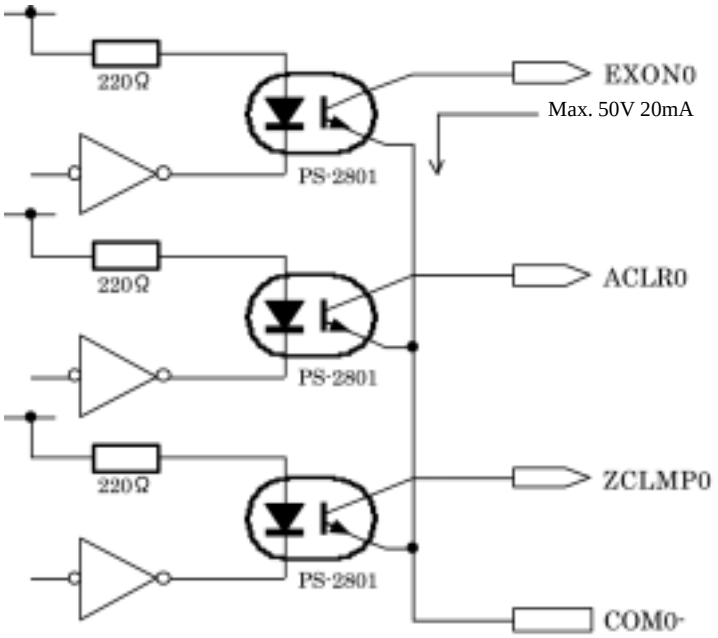


Fig. 8-3 Schematic Diagram of Control Output Section

8.3 Control Input Interface

Control output is provided with insulation with the photocoupler. Input logic of ORG, ALM, BHL, FHL, BL, and FL signals of each axis can be set with the limit control register (LCR#n). With the LCR's corresponding bit being "1", signals are input when the photocoupler (PC) is OFF. With the LCR's corresponding bit being "0", signals are input when PC is ON. The COM#n+ axes each requires 4.5~13.2V power source.

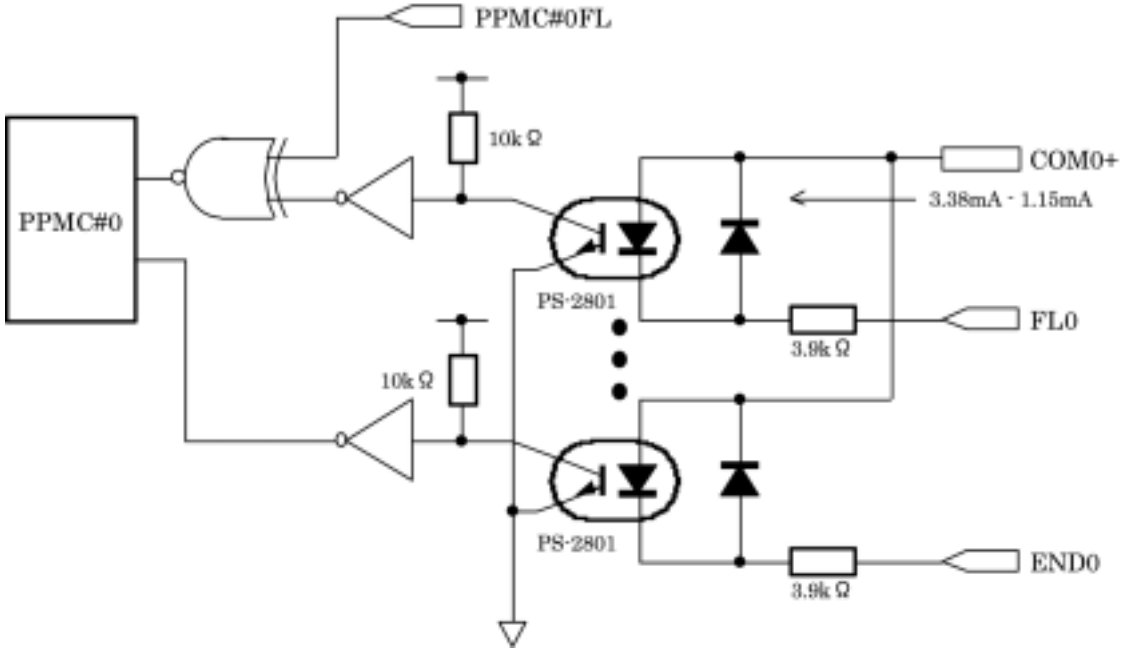


Fig. 8-4 Schematic Diagram of Control Input Section

8.4 Encoder I/O (PHA, PHB, PHC)

Encoder input is insulation input with differential output as the prerequisite. Encoder pulses of 90° phase difference (PHA/PHB) and origin position output (PHC) are output. PHC is connected to the INDEX* signal of the PPMC-312. As for the INDEX* signal, see the PPMC-312 Instruction Manual.

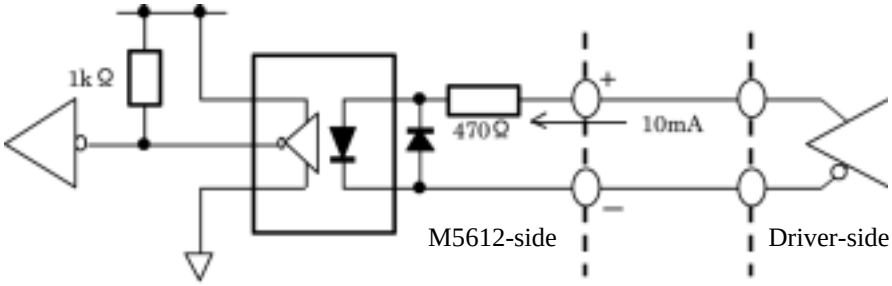


Fig. 8-5 Encoder Input Circuit Example 1

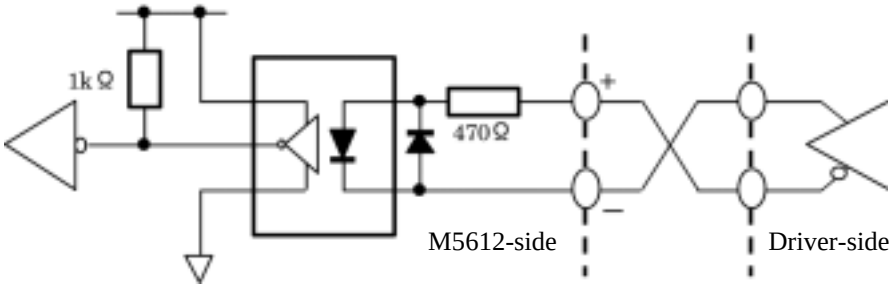


Fig. 8-6 Encoder Input Circuit Example 2

9. Electric Characteristics

9.1 Pulse Output Signals

Electric Characteristics of CW#n/ CCW#n Signals

Table 9-1 Electric Characteristic Table of Pulse Output Signals

Item	Symbol	Min	Max	Unit	Condition
"H" level output voltage	V_{OH}	2.5		V	I_{OL} = -20mA
"L" level output voltage	V_{OL}		0.5	V	I_{OL} = 20mA

9.2 Control Output Signals

Electric Characteristics of ACLR#n/ EXON#n/ ZCLMP#n Signals

Table 9-2 Electric Characteristic Table of Control Output Signals

Item	Symbol	Min	Max	Unit	Condition
Collector-emitter voltage			50	V	
Collector current	I_C		20	Ma	
"L" level output voltage	V_{OL}		0.3	V	I_C = 10mA

9.3 Control Input Signals

Electric Characteristics of END#n/ ALM#n/ ORG#n/ BHL#n/ FHL#n/ BL#n/ FL#n Signals

Table 9-3 Electric Characteristic Table of Control Input Signals

Item	Symbol	Min	Max	Unit	
Input supply voltage	V_{IN}	4.5	13.2	V	
"H" level output voltage	V_{IH}	*1	-	V	
"L" level output voltage	V_{IL}	-	1.5	V	

*1 Equal to supply voltage.

9.4 Encoder Input Signals

Electric Characteristics of PHA#n/ PHB#n/ PHC#n Signals

Table 9-4 Electric Characteristics of Encoder Input Signals

Item	Symbol	Min	Max	Unit	
Input supply voltage (reference)	V_{IN}	-5.1	5.1	V	
ON input voltage difference	V_{ON}	2.6		V	
OFF input voltage difference	V_{OFF}		0.7	V	

10. Encoder Pulse Input Timing

10.1 Normal Time (Same Direction Rotation)

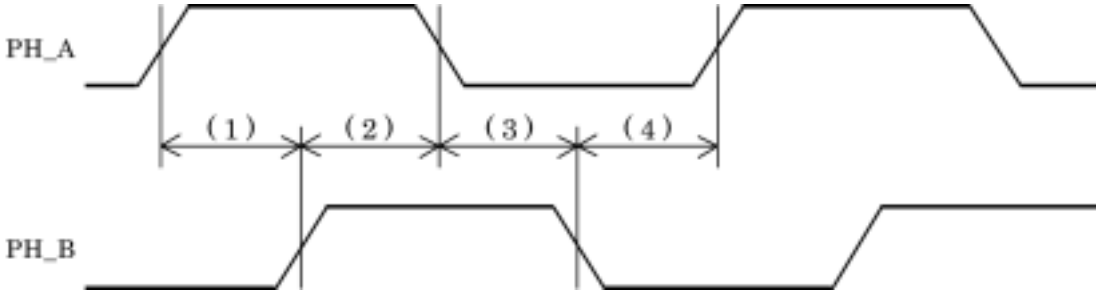


Fig. 10-1 Encoder Pulse Input Timing

10.2 On Changing of Encoder Input Direction

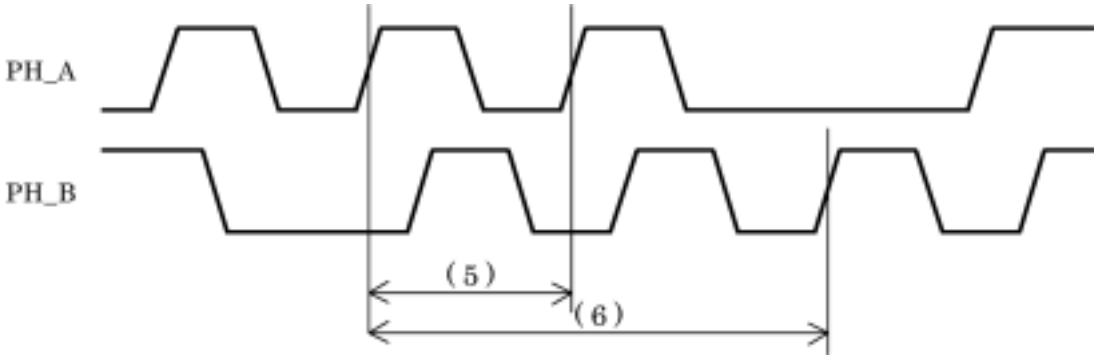


Fig. 10-2 Encoder Direction Change Input Timing

Table 10-1 Encoder Input Timing Table

Item		x1		x2		x4		Unit
		Min	Max	Min	Max	Min	Max	
(1),(3)	From PHA change to PHB change	125	-	250	-	500	-	ns
(2),(4)	From PHB change to PHA change	125	-	250	-	500	-	ns
(5)	Input pulse frequency just after direction change	-	40	-	20	-	10	KHz
(6)	Interval for next direction change	500	-	500	-	500	-	μs

11. Connector Signal Table

Table 11-1 List of Connector Signals

PIN No.	Signal name	I/O	Function	PIN No.	Signal name	I/O	Function
1	END#0	I	#0 control input	49	END#2	I	#2 control input
2	ALM#0	I		50	ALM#2	I	
3	ORG#0	I		51	ORG#2	I	
4	BHL#0	I		52	BHL#2	I	
5	FHL#0	I		53	FHL#2	I	
6	BL#0	I		54	BL#2	I	
7	FL#0			55	FL#2		
8	COM#0+	-		56	COM#2+	-	
9	COM#0-	-	#0 control output	57	COM#2-	-	#2 control output
10	ACLR#0	O		58	ACLR#2	O	
11	EXON#0	O		59	EXON#2	O	
12	ZCLMP#0	O		60	ZCLMP#2	O	
13	PHC#0-	I	#0 encoder input	61	PHC#2-	I	#2 encoder input
14	PHC#0+	I		62	PHC#2+	I	
15	PHB#0-	I		63	PHB#2-	I	
16	PHB#0+	I		64	PHB#2+	I	
17	PHA#0-	I		65	PHA#2-	I	
18	PHA#0+	I		66	PHA#2+	I	
19	NC	-		67	NC	-	
20	SG	-	#0 pulse output	68	SG	-	#2 pulse output
21	CCW#0- /DIR#0-	O		69	CCW#2- /DIR#2-	O	
22	CCW#0+ /DIR#0+	O		70	CCW#2+ /DIR#2+	O	
23	CW#0- /POUT#0-	O		71	CW#2- /POUT#2-	O	
24	CW#0+ /POUT#0+	O		72	CW#2+ /POUT#2+	O	
25	END#1	I	#1 control input	73	END#3	I	#3 control input
26	ALM#1	I		74	ALM#3	I	
27	ORG#1	I		75	ORG#3	I	
28	BHL#1	I		76	BHL#3	I	
29	FHL#1	I		77	FHL#3	I	
30	BL#1	I		78	BL#3	I	
31	FL#1	I		79	FL#3	I	
32	COM#1+	-		80	COM#3+	-	
33	COM#1-	-	#1 control output	81	COM#3-	-	#3 control output
34	ACLR#1	O		82	ACLR#3	O	
35	EXON#1	O		83	EXON#3	O	
36	ZCLMP#1	O		84	ZCLMP#3	O	
37	PHC#1-	I	#1 encoder input	85	PHC#3-	I	#3 encoder input
38	PHC#1+	I		86	PHC#3+	I	
39	PHB#1-	I		87	PHB#3-	I	
40	PHB#1+	I		88	PHB#3+	I	
41	PHA#1-	I		89	PHA#3-	I	
42	PHA#1+	I		90	PHA#3+	I	
43	NC	-		91	NC	-	
44	SG	-	#1 pulse output	92	SG	-	#3 pulse output
45	CCW#1- /DIR#1-	O		93	CCW#3- /DIR#3-	O	
46	CCW#1+ /DIR#1+	O		94	CCW#3+ /DIR#3+	O	
47	CW#1- /POUT#1-	O		95	CW#3- /POUT#3-	O	
48	CW#1+ /POUT#1+	O		96	CW#3+ /POUT#3+	O	

12. Appendix (Reference)

Should any serial ROM value be deleted by mistake, write the data shown below by using ROM Writer, etc.

Table 12-1 List of Serial EEPROM Set Values (1/2)

Serial EEPROM offset address	PLX offset address	Register name	Set value
00h	PCI 02H	Device ID	5612h
02h	PCI 00H	Vendor ID	172Ch
04h	PCI 06H	PCI Status	0280h
06h	PCI 04H	Reserved	0000h
08h	PCI 0AH	Class Code	1180h
0Ah	PCI 08H	Class Code / Revision	0001h
0Ch	PCI 2EH	Subsystem ID	0000h
0Eh	PCI 2CH	Subsystem Vendor ID	0000h
10h	PCI 36H	Reserved	0000h
12h	PCI 34H	LSB New Capability Pointer	0040h
14h	PCI 3EH	Reserved	0000h
16h	PCI 3CH	Interrupt Pin	0100h
18h	PCI 42H	MSB of Power Management Capabilities	0000h
1Ah	PCI 40H	Reserved	0000h
1Ch	PCI 46H	MSW of Power Management Data / PMCSR Bridge Support Extension	0000h
1Eh	PCI 44H	LSW of Power Management Control / Status	0000h
20h	PCI 4AH	Reserved	0000h
22h	PCI 48H	LSW of Hot Swap Next Capability Pointer / Hot Swap Control	0000h
24h	PCI 4EH	Reserved	0000h
26h	PCI 4CH	PCI Vital Product Data Next Capability Pointer / PCI Vital Product Data Control	0000h
28h	LOCAL 02h	MSW of Range for PCI-to-Local Address Space 0	FFFFh
2Ah	LOCAL 00h	LSW of Range for PCI-to-Local Address Space 0	FFC1h
2Ch	LOCAL 06h	MSW of Range for PCI-to-Local Address Space 1	0000h
2Eh	LOCAL 04h	LSW of Range for PCI-to-Local Address Space 1	0000h
30h	LOCAL 0Ah	MSW of Range for PCI-to-Local Address Space 2	0000h
32h	LOCAL 08h	LSW of Range for PCI-to-Local Address Space 2	0000h
34h	LOCAL 0Eh	MSW of Range for PCI-to-Local Address Space 3	0000h
36h	LOCAL 0Ch	LSW of Range for PCI-to-Local Address Space 3	0000h
38h	LOCAL 12h	MSW of Range for PCI-to-Local Expansion ROM	0000h
3Ah	LOCAL 10h	LSW of Range for PCI-to-Local Expansion ROM	0000h
3Ch	LOCAL 16h	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	0000h
3Eh	LOCAL 14h	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	0001h
40h	LOCAL 1Ah	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	0000h
42h	LOCAL 18h	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	0000h

Table 12-1 List of Serial EEPROM Set Values (2/2)

Serial EEPROM offset address	PLX offset address	Register name	Set value
44h	LOCAL 1Eh	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 2	0000h
46h	LOCAL 1Ch	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 2	0000h
48h	LOCAL 22h	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 3	0000h
4Ah	LOCAL 20h	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 3	0000h
4Ch	LOCAL 26h	MSW of Local Base Address (Remap) for PCI-to-Local Address Space ROM	0000h
4Eh	LOCAL 24h	LSW of Local Base Address (Remap) for PCI-to-Local Address Space ROM	0000h
50h	LOCAL 2Ah	MSW of Bus Region Descriptors for Local Address Space 0	1400h
52h	LOCAL 28h	LSW of Bus Region Descriptors for Local Address Space 0	40C0h
54h	LOCAL 2Eh	MSW of Bus Region Descriptors for Local Address Space 1	0000h
56h	LOCAL 2Ch	LSW of Bus Region Descriptors for Local Address Space 1	0000h
58h	LOCAL 32h	MSW of Bus Region Descriptors for Local Address Space 2	0000h
5Ah	LOCAL 30h	LSW of Bus Region Descriptors for Local Address Space 2	0000h
5Ch	LOCAL 36h	MSW of Bus Region Descriptors for Local Address Space 3	0000h
5Eh	LOCAL 34h	LSW of Bus Region Descriptors for Local Address Space 3	0000h
60h	LOCAL 3Ah	MSW of Bus Region Descriptors for Expansion ROM	0000h
62h	LOCAL 38h	LSW of Bus Region Descriptors for Expansion ROM	0000h
64h	LOCAL 3Eh	MSW of Chip Select (CS) 0 Base and Range	0000h
66h	LOCAL 3Ch	LSW of Chip Select (CS) 0 Base and Range	0001h
68h	LOCAL 42h	MSW of Chip Select (CS) 1 Base and Range	0000h
6Ah	LOCAL 40h	LSW of Chip Select (CS) 1 Base and Range	0000h
6Ch	LOCAL 46h	MSW of Chip Select (CS) 2 Base and Range	0000h
6Eh	LOCAL 44h	LSW of Chip Select (CS) 2 Base and Range	0000h
70h	LOCAL 4Ah	MSW of Chip Select (CS) 3 Base and Range	0000h
72h	LOCAL 48h	LSW of Chip Select (CS) 3 Base and Range	0000h
74h	LOCAL 4Eh	Serial EEPROM Write-Protected Address boundary	0030h
76h	LOCAL 4Ch	LSW of Interrupt Control / Status Register	0041h
78h	LOCAL 52h	MSW of PCI Target Response, Serial EEPROM, and Initialization Control	0078h
7Ah	LOCAL 50h	LSW of PCI Target Response, Serial EEPROM, and Initialization Control	1000h
7Ch	LOCAL 56h	MSW of General Purpose I/O Control	0000h
7Eh	LOCAL 54h	LSW of General Purpose I/O Control	0000h
80h	LOCAL 72h	MSW of Hidden 1 Power Management Data Select	0000h
82h	LOCAL 70h	LSW of Hidden 1 Power Management Data Select	0000h
84h	LOCAL 76h	MSW of Hidden 2 Power Management Data Select	0000h
86h	LOCAL 74h	LSW of Hidden 2 Power Management Data Select	0000h