1. Overview

Macro5521 is a stepper motor control board based on ISA bus.
Macro5521A, which has 3 pieces of PPMC-111CFP, can control up to 3 stepper motors, and Macro5521B, which has one PPMC-111C, can control one stepper motor.

Most of motor drivers isolate their input signals of CW-pulse, CCW-pulse and other's. Therefore, Macro5521 is designed to isolate only input signals of Limit signals, ORIGN signal and other's, while not to isolate output signals of CW-pulse, CCW-pulse and other's.
Please note that it may be necessary to take appropriate measure should these specifications not meet the conditions of your operating environment.

PPMC-111C/CFP can easily control stepper motor simply with command data provided by the host CPU, which reduces the load on the host CPU significantly.
In addition, the attached example program (the source code written in MS-C) would enable you to customize the board to exactly meet your needs in a short period of time.

2. Specifications

Table 2-1. Macro5521 Board Specifications

Motor type		Stepper motor
Control LSI		Macro5521A: PPMC-111CFP x 3
		Macro5521B: PPMC-111CFP x 1
Number of axes		Macro5521A: 1 - 3
		Macro5521B: 1
Output pulse	Frequency	31ppS to 66.67kppS (when selecting one time mode)
		8ppS to 16.67kppS (when selecting one-forth mode)
		2 ppS to 4.17kppS (when selecting one-sixteenth mode)
	Method	2-phase (CW, CCW) pulse output method
	Width	Duty raito 50%
Maximum output pulses		±16,777,215 pulses
		(Not valid for Constant Speed Origin Search command and
		Continuous Operation commands, which are unlimited)
Limit input signal		5 points/axis
		(Origin, CW/CCW limits, CW/CCW high speed limits)
Input circuit	limit signals &	+5V Optoisolated
	driver control signals	(Available for normal closed type switch)
Output circuit		TTL level (negative logic)
On-board register	Module Control Register	1. A bit controls simultaneous start of all axes
		2. Four bits control auxiliary output signals
		3. A bit releases the IRQ locking
		4. A bit resets PPMC
	Module Status Register	1. Three bits show the status of Interrupt genelation
		2. Three bits show the status of ALM input
		3. A bit shows to release the IRQ locking
		4. A bit shows to reset PPMC
ISA bus	I/O address	8-bytes between 000h and 3FFh
	Interrupt	One level of IRQ 10/11/12/15
Interface connector		3433-1002LCSC (3M) or equivalent
		Adaptable connector: 7950-6500SC
Power reuirement		DC +5V ±5% 1A
Operating environment	Temperature	0 to +55°C
	Humidity	30 to 85% (No dew condensation)
	Atmosphere	Air which does not include corrosive gases
Dimensions		ISA bus board, half size
Contents		Macro5521, Manual, Example program
		(the source code written in MS-C)

3. Macro5521 Block Diagrams

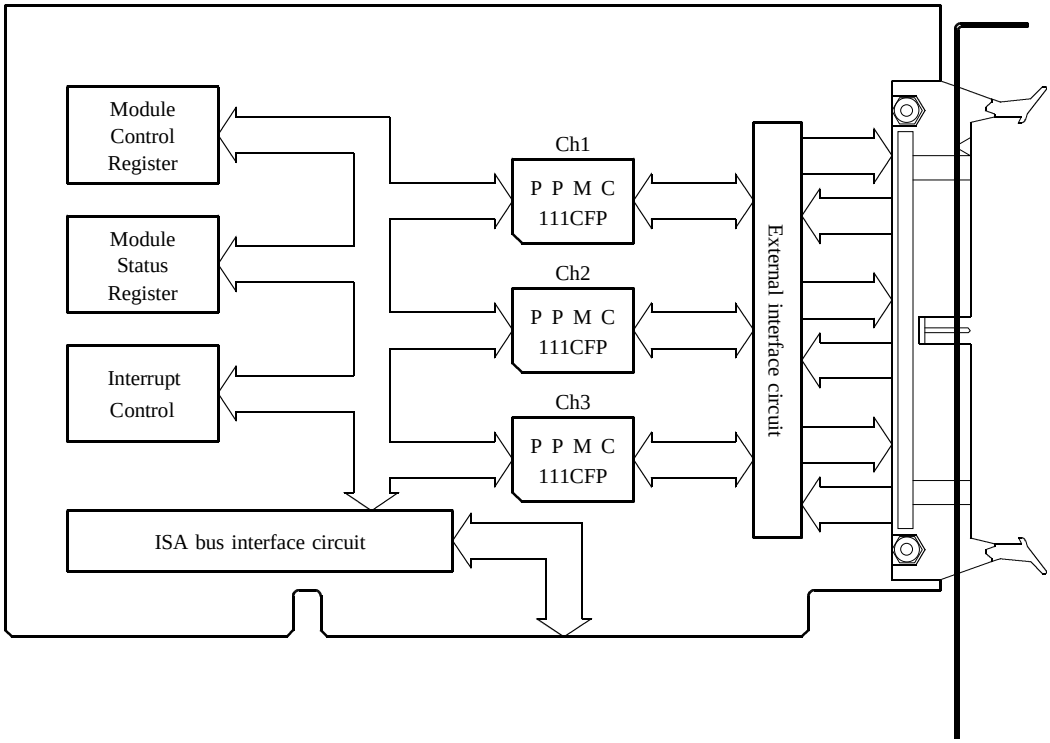


Figure 3-1. Macro5521A Board Block Diagram

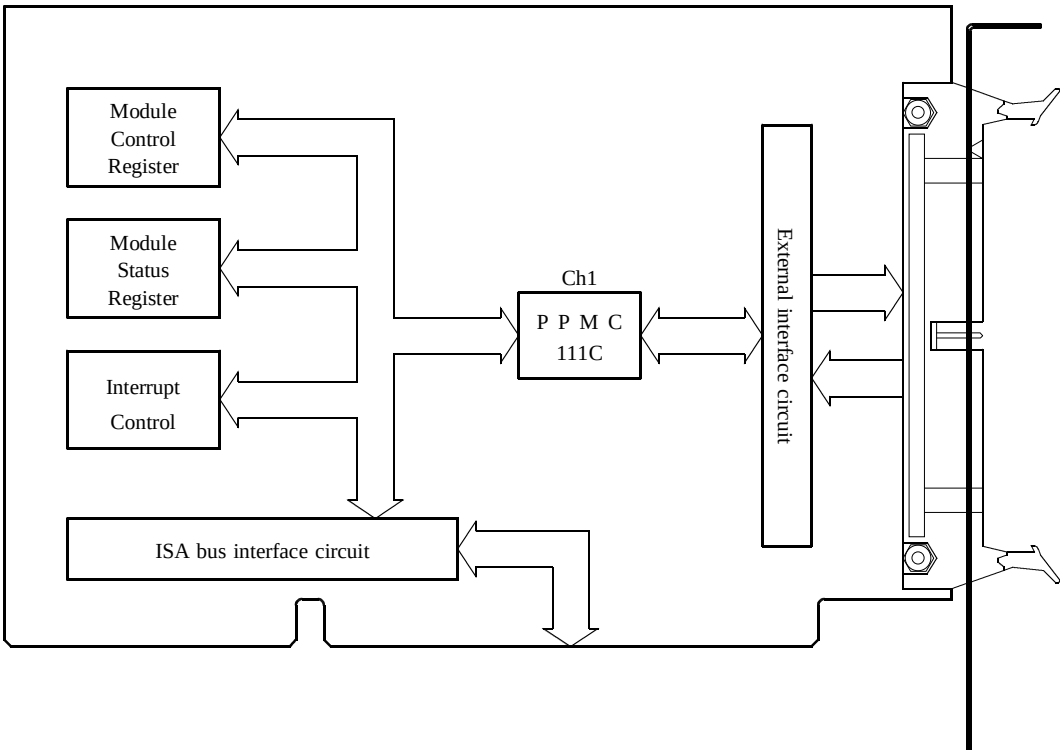


Figure 3-2. Macro5521B Board Block Diagram

4. Front panel

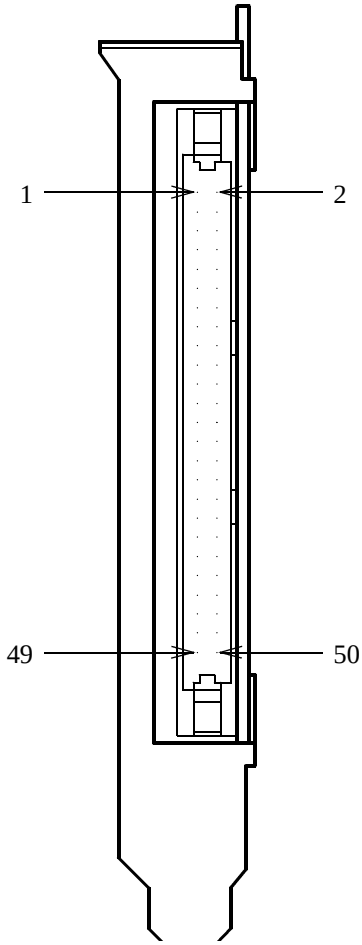


Figure 4-1. Macro5521 Board Front panel

5. PPMC Locations

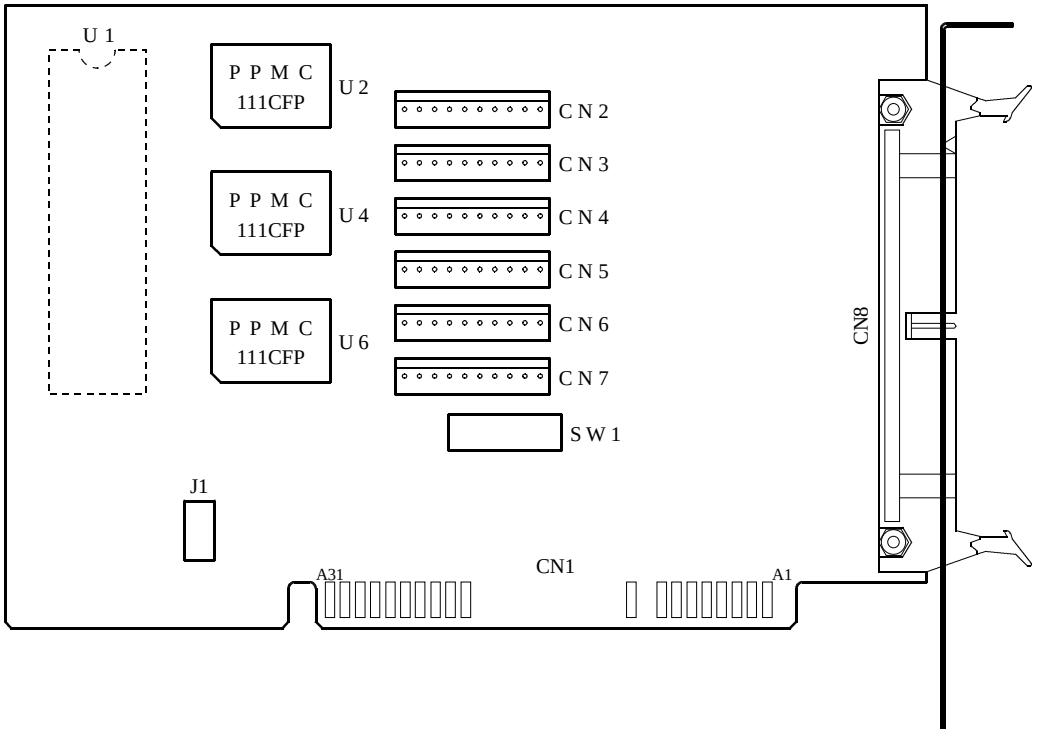


Figure 5-1. Macro5521A PPMC Locations

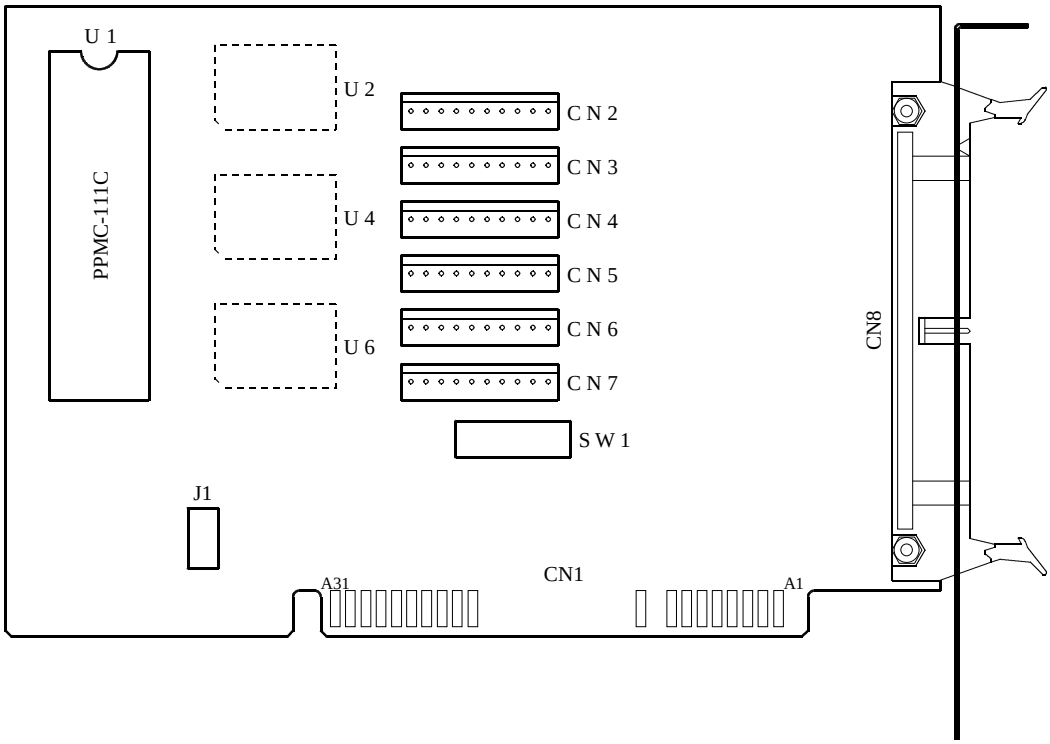


Figure 5-2. Macro5521B PPMC Location

6. I/O Port Addresses

Macro5521 occupies 8 bytes address space in I/O address space of ISA bus.

6-1. Base address setting

Macro5521's base address is set using a DIP switch SW1 from 000h to 3FFh.

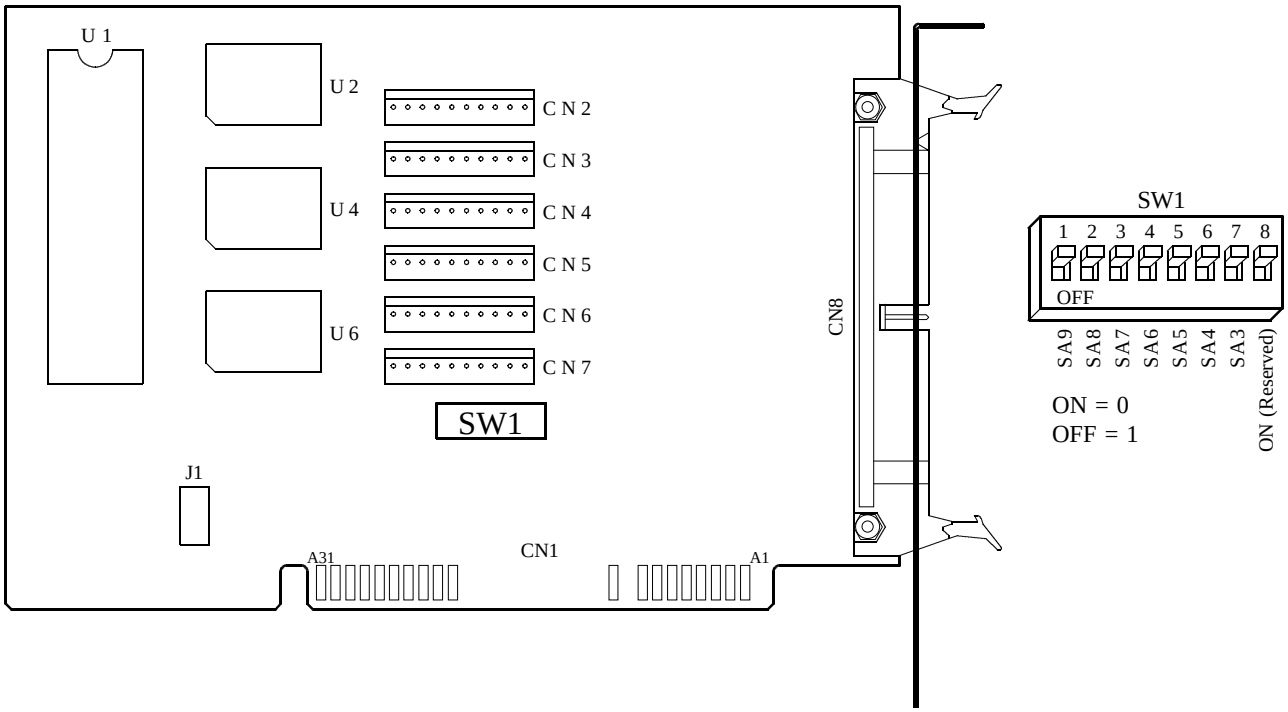


Figure 6-1. Macro5521 DIP Switch SW1 Location

Table 6-1. Macro5521 Base Address Setting

Setting of DIP switch SW1								Base address
1	2	3	4	5	6	7	8	
SA9	SA8	SA7	SA6	SA5	SA4	SA3	-	
ON	ON	ON	ON	ON	ON	ON	ON	000h
ON	ON	ON	ON	ON	ON	OFF	ON	008h
ON	ON	ON	ON	ON	OFF	ON	ON	010h
:								:
OFF	OFF	OFF	OFF	OFF	ON	ON	ON	3E8h
OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	3F0h
OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	3F8h

ON = 0
OFF= 1

In most of the ISA bus computers, many of the address space from 000h to 0FFh is used for the system I/O and the other devices. Therefore Macro5521's address must set the address space not to use by any.

6-2. Registers Address

The offset addresses of Module Control Register, Module Status Register and each PPMC-111's internal registers are listed in Table 6-2.

Table 6-2. Macro5521 Registers Address

Offset Address	Register	
	IN	OUT
00h	Module Status Register	Module Control Register
01h	reserved	reserved
02h	Ch1 PPMC-111 data register	Ch1 PPMC-111 data register
03h	Ch1 PPMC-111 status register	Ch1 PPMC-111 command register
04h	Ch2 PPMC-111 data register	Ch2 PPMC-111 data register
05h	Ch2 PPMC-111 status register	Ch2 PPMC-111 command register
06h	Ch3 PPMC-111 data register	Ch3 PPMC-111 data register
07h	Ch3 PPMC-111 status register	Ch3 PPMC-111 command register

7. On-board Registers

7-1. Module Control Register (MCR)

The Module Control Register (MCR) is an 8-bit register for controlling Macro5521.

All bits of this register are set to zero when the board is reset.

The bits of this register are described below.

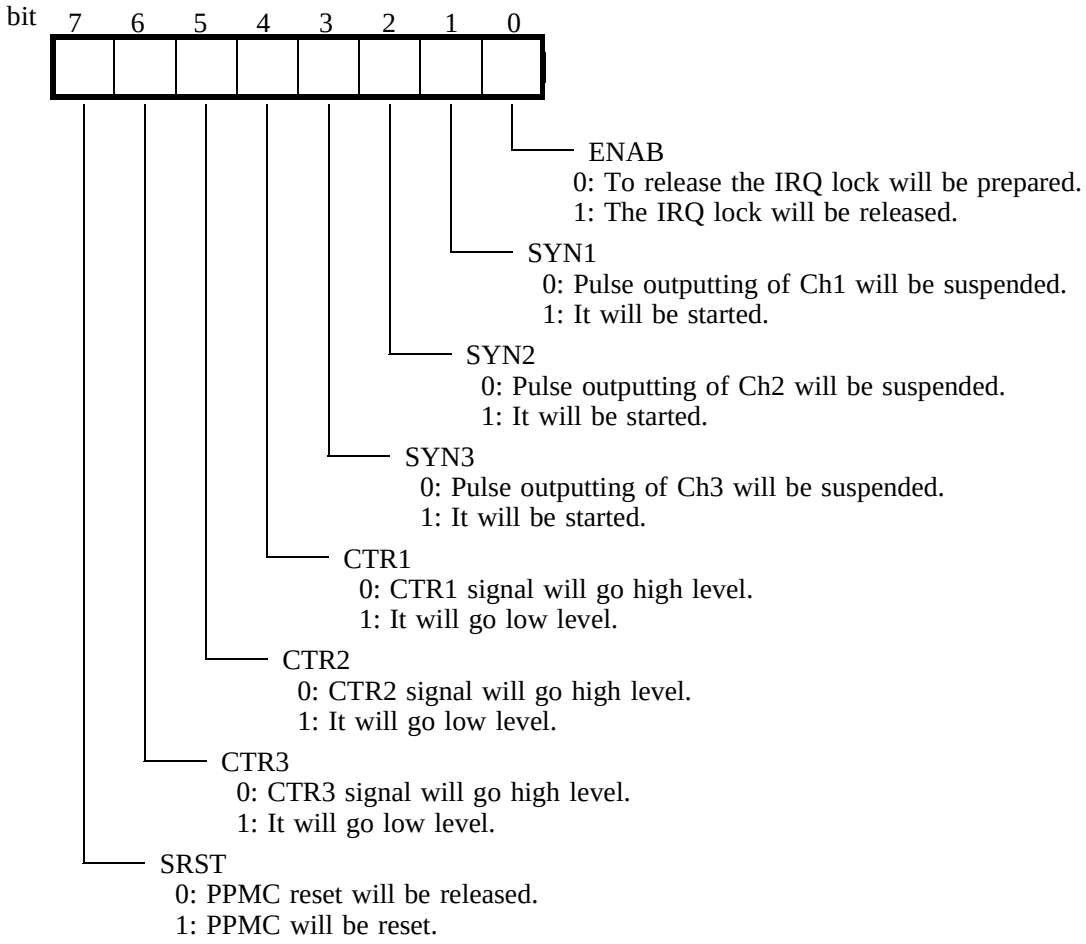


Figure 7-1. Bits of MCR

1. ENAB (bit 0)

Macro5521 has the IRQ locking function, and this bit is used to release it (see Section 8-2).

To release IRQ locking, set 0 to this bit first, then set 1 again.

2. SYN1 to SYN3 (bit 1 to 3)

These bits control RUN signals (pulse output start) of PPMC-111. This function is used for starting outputting pulses from the three axes simultaneously, or for starting outputting pulses and carrying out other tasks simultaneously. If set 0 to these bits, PPMC-111 on Macro5521 will receive one operation command, but it won't outputting pulse and receiving the other operation command until set 1 to these bits. Please refer to the instruction manual of the PPMC-111 for the synchronized operation start function of the PPMC-111.

3. CTR1 to CTR3 (bit 4 to 5)

These bits are used to turn on/off $\overline{\text{CTR1}}$, $\overline{\text{CTRY}}$ and $\overline{\text{CTRZ}}$ signals.

4. SRST (bit 7)

This bit is used to reset PPMC on Macro5521.

7-2. Module Status Register (MSR)

The Module Status Register (MSR) is an 8-bit register for indicating a status of Macro5521.

All bits of this register are set to zero when the board is reset.

The bits of this register are described below.

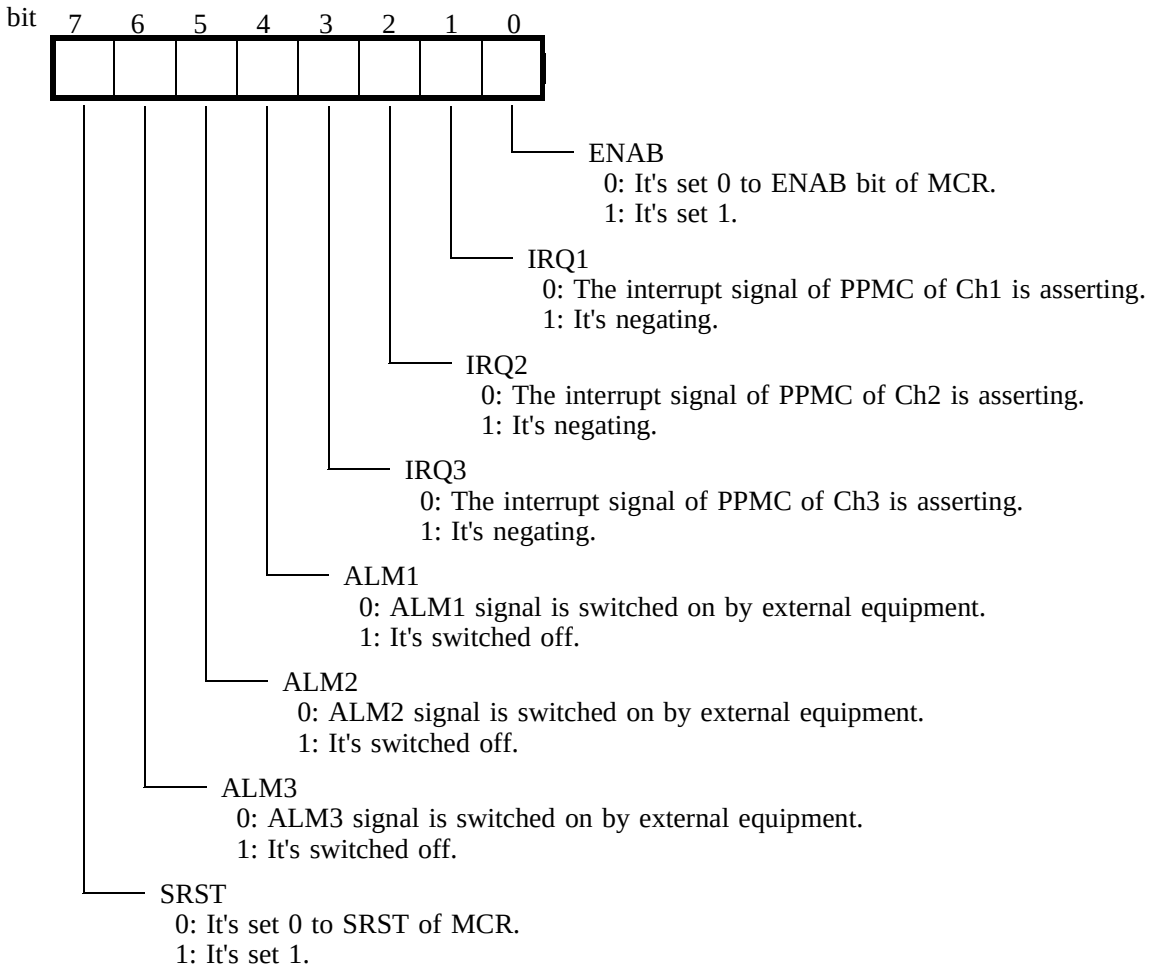


Figure 7-3. Bits of MSR

1. ENAB (bit 0)

This bit indicates whether it was set 0 or 1 to ENAB of MCR.

2. IRQ1 to IRQ3 (bit 1 to 3)

These bits indicate whether PPMC-111 assert or not the interrupt signals now.

3. ALM1 to ALM3 (bit 4 to 6)

These bits indicate whether ALM1 to 3 of Macro5521 turn on or off now.

4. SRST (bit 7)

This bit indicates whether it was set 0 or 1 to SRAT of MCR.

8. IRQ Setting

Macro5521 has a jumper J1 for selecting the IRQ level (IRQ10/11/12/15).

8-1. Selection of an IRQ level

The jumper J1 selects an IRQ level of Macro5521.

The figure 8-1 and table 8-1 show how to set up it.

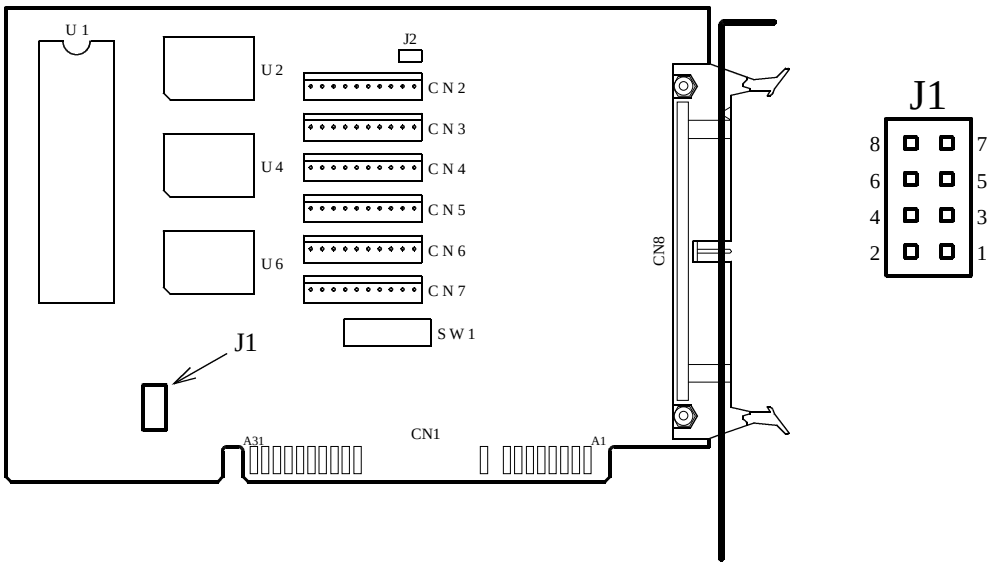


Figure 8-1. Macro5521 Jumper J1 Location

Table 8-1. Macro5521 Jumper J1 (IRQ Level) Setting

IRQ Level	Jumper J1
IRQ10	Short between 1 - 2
IRQ11	Short between 3 - 4
IRQ12	Short between 5 - 6
IRQ15	Short between 7 - 8

8-2. IRQ Control

Macro5521 has the IRQ locking function. During Macro5521 asserts the IRQ from a PPMC to ISA bus, even the other PPMC generate any interrupts, Macro5521 asserts no more IRQ.

When the host CPU reads MSR (the status register of Macr5521), the IRQ will be cleared soon. And if the other PPMC generate any interrupts to try to assert IRQ, Macro5521 won't assert the IRQ.

In this case, Macro5521 will never assert if the IRQ locking don't release as below.

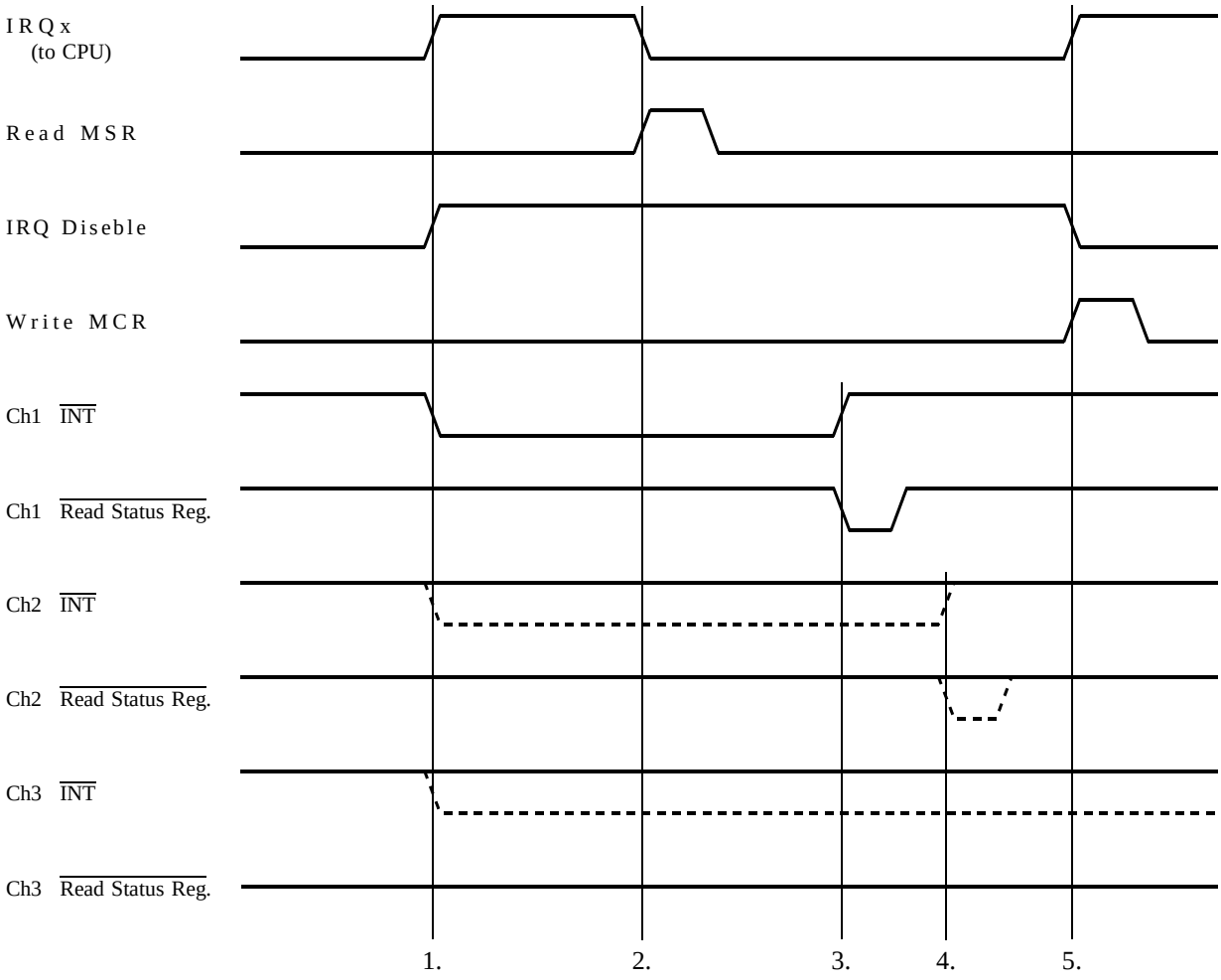


Figure 8-2. Timings of IRQ Lock and Release

(1). When Macro5521 asserts the IRQ from a PPMC to ISA bus, even the other PPMC generate any interrupts, Macro5521 asserts no more IRQ.
(2). When the host CPU read MSR, IRQ will be release. And you'll be able to recognize which PPMC is generating interrupt by the status data of bit 1 to 3 of MSR.
(3). If PPMC of Ch1 is generating the interrupt, read Status Register of PPMC of Ch1, and recognize why the interrupt is generating from this PPMC first. Then, if bit 4 (INTS) of Status Register of the PPMC is 1, execute Finish Status Read Command. And if bit 5 of Status Register of the PPMC is 1, execute Command Error Code Read Command. If so, the interrupt of the PPMC will be released.
(4). If PPMC of Ch2 and Ch3 are generating the interrupts, execute the same as mentioned above (3).
(5). Set 0 to ENAB bit of MCR first, and set 1 to the bit again. If so, the IRQ lock will be release, and the Macro5521 becomes to be again able to assert the IRQ.

9. Signals for customizing

PPMC-111 on Macro5521 has 8 input and 8 output signals. Macro5521 doesn't connect these signals to the connector CN8. These signals are just connected to the through holes CN2 - 7. You can use them by customizing them if necessary. The figure 9-1 shows the location of CN2 - 7, and the table 9-1 and 9-2 show these pins' assignment.

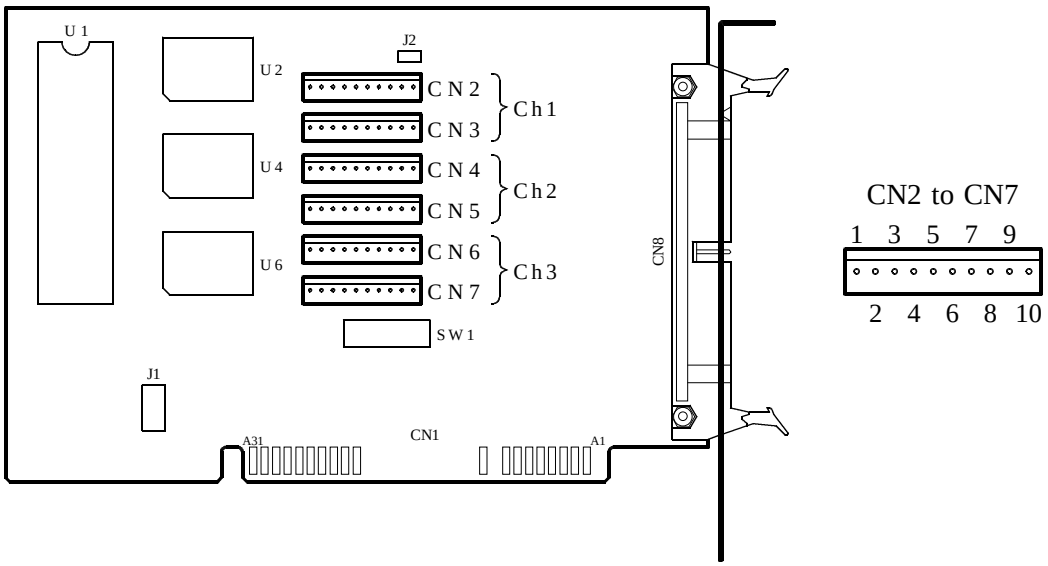


Figure 9-1. Macro5521 Connector CN2 to CN7 Locations

Table 9-1. CN2, CN4, CN6 Pin Assignment

Pin		I/O	Signal	Function
CN2(Ch1) CN4(Ch2) CN6(Ch3)	1	PS	+5V	common with +5V of ISA bus
	2	I	AUXI 0	Auxiliary input (Bit 0)
	3	I	AUXI 1	Auxiliary input (Bit 1)
	4	I	AUXI 2	Auxiliary input (Bit 2)
	5	I	AUXI 3	Auxiliary input (Bit 3)
	6	I	AUXI 4	Auxiliary input (Bit 4)
	7	I	AUXI 5	Auxiliary input (Bit 5)
	8	I	AUXI 6	Auxiliary input (Bit 6)
	9	I	AUXI 7	Auxiliary input (Bit 7)
	10	PS	GND	common with GND of ISA bus

Table 9-2. CN3, CN5, CN7 Pin Assignment

Pin		I/O	Signal	Function
CN3(Ch1) CN5(Ch2) CN7(Ch3)	1	PS	+5V	common with +5V of ISA bus
	2	O	AUXO 0	Auxiliary output (Bit 0)
	3	O	AUXO 1	Auxiliary output (Bit 1)
	4	O	AUXO 2	Auxiliary output (Bit 2)
	5	O	AUXO 3	Auxiliary output (Bit 3)
	6	O	AUXO 4	Auxiliary output (Bit 4)
	7	O	AUXO 5	Auxiliary output (Bit 5)
	8	O	AUXO 6	Auxiliary output (Bit 6)
	9	O	AUXO 7	Auxiliary output (Bit 7)
	10	PS	GND	common with GND of ISA bus

These customizing signals are connected directly from each PPMC-111 to the holes CN2 to CN7. Pay attention to the rating of the PPMC-111, external noises, etc., while using these signals.

10. Current Position Counter Clearing Function

On Jumper J2, you can select whether or not the current position counter will be reset to zero when the ORG signal is detected during a Constant Speed Origin Search Operation. The figure 10-1 and the table 10-1 show how to set this option.

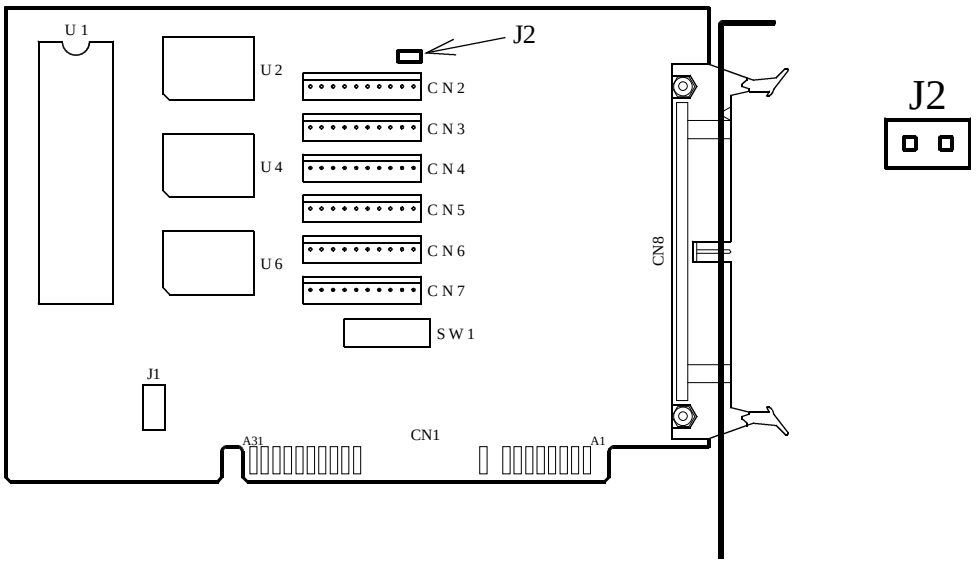


Figure 10-1. Jumper J2 Location

Table 10-1. Jumper J2 Option

Status of Jumper J2	How to work the current position counter
Open	To clear when the Origin signal is detected.
Short	Not to clear when the Origin signal is detected.

11. Input and Output Signals

The input and output signals of Macro5521 is connected the connector CN8.

11-1. Input circuit

The input signals are connected via photo couplers to PPMC on Macro5521 from external equipment. The figure 11-1 is the signals input structure, and figure 11-2 is an example of input signal connection with external equipment.

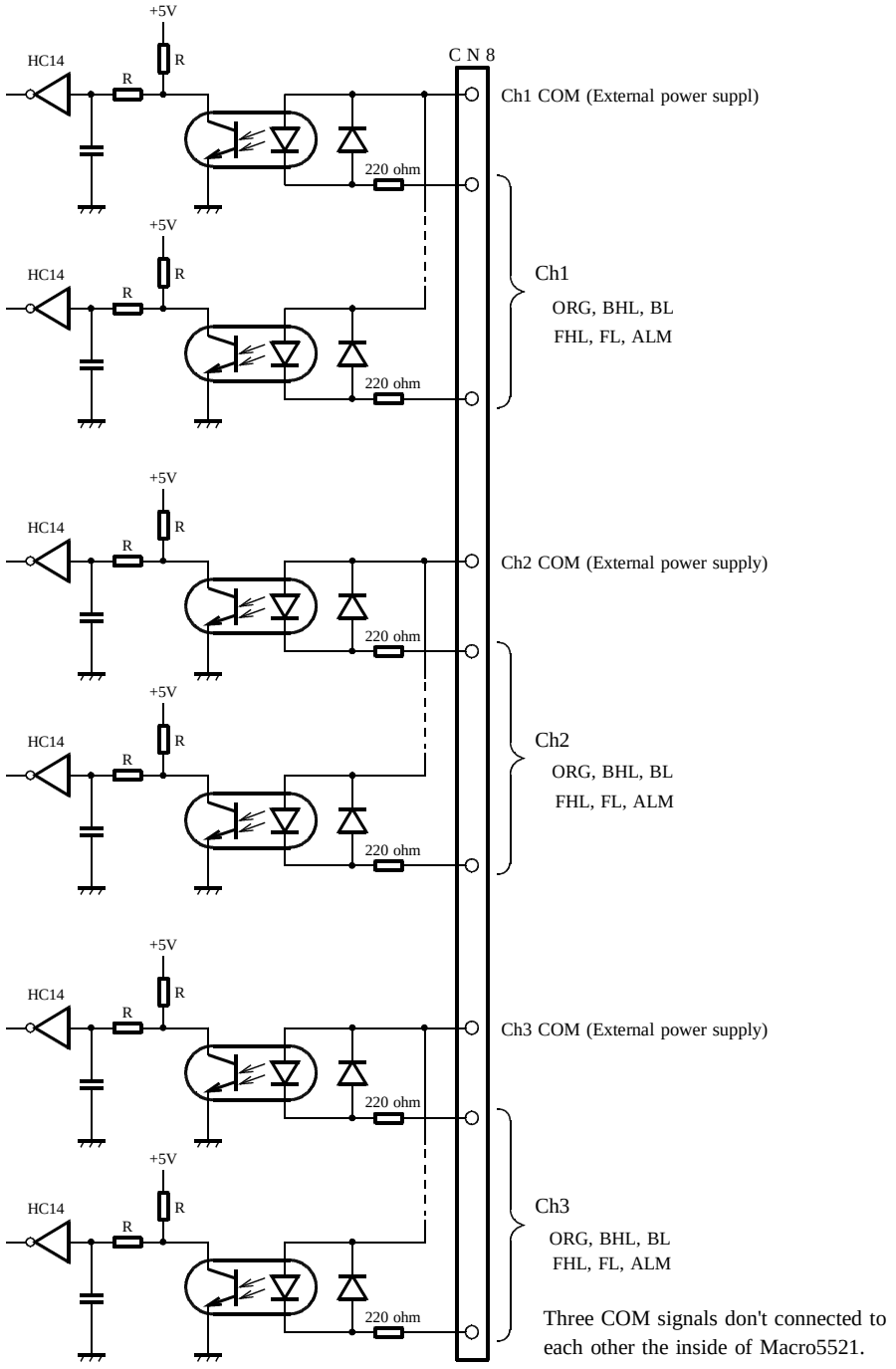


Figure 11-1. Signals Input Structure

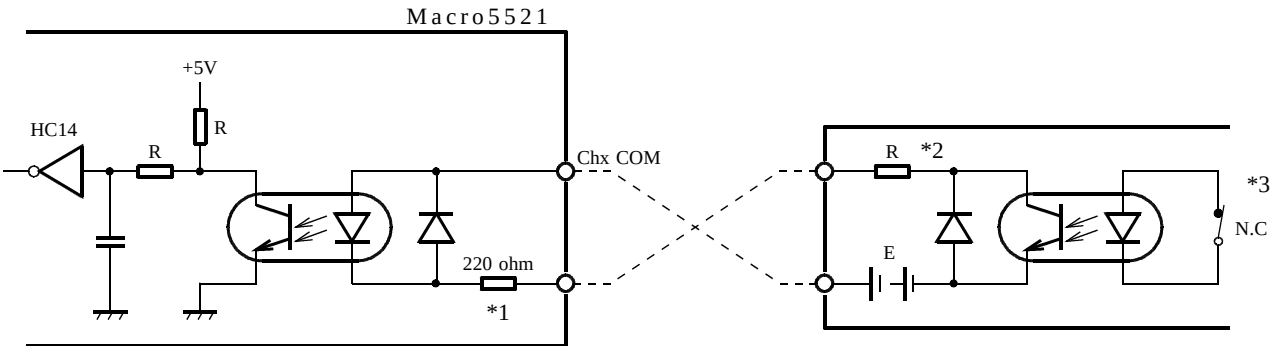


Figure 11-2. Example of Input Signal Connection

The value of resistances (*1) on Macro5521 is suitable when the voltage's value of the external power supply is +5V.
If you use the other type's one except +5V (for example +12V), you must add external resistances (*2).
Figure 11-2 shows an example connection, in which a normal closed switch (*3) is used.

Note:

If not necessary and you don't use any input signals, you must provide the prescribed signals to them. If you make their input signals open, the signals connecting the PPMC will be low level. And, when the host CPU execute any Operation Command, the PPMC will be error status 03h, which issue in case of any limit signal or alarm signal is asserting.

11-2. Output Circuit

Macro5521 outputs the signals for controlling motor drivers and others not via photo coupler. The figures 11-3 the signals output structure and 11-4 show an example of output signal connection.

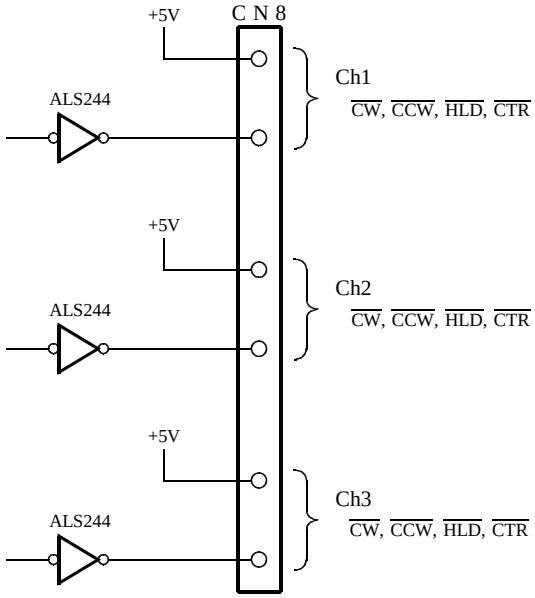


Figure 11-3. Signals Output Structure

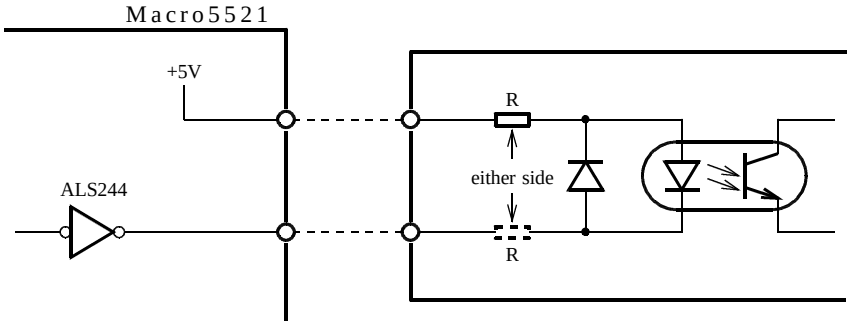


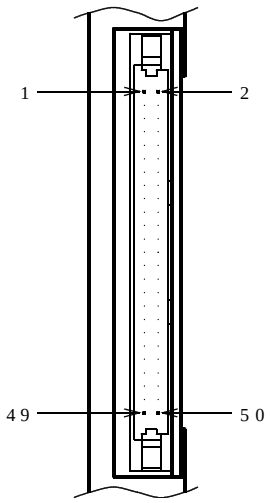
Figure 11-4. Example of Output Signal Connection

Table 11-1 shows the pin assignment of the connector CN8.

Table 11-1. Connector CN8 Pin Assignment

Function	I/O	Signal	Pin		Signal	I/O	Function
Ground	I/O	GND	1	2	GND	I/O	Ground
+5V	O	+5V	3	4	+5V	O	+5V
Ch1 CW pulses	O	$\overline{\text{CW1}}$	5	6	$\overline{\text{HLD1}}$	O	Ch1 hold signal
Ch1 CCW pulses	O	$\overline{\text{CCW1}}$	7	8	$\overline{\text{CTR1}}$	O	Ch1 output control signal
Ch1 origin signal	I	ORG1	9	10	ALM1	I	Ch1 alarm signal
Ch1 CCW high speed limit	I	BHL1	11	12	FHL1	I	Ch1 CW high speed limit
Ch1 CCW limit	I	BL1	13	14	FL1	I	Ch1 CW limit
Ch1 external power supply	I	COM1	15	16	SLD	-	Ch1 shield
Ground	I/O	GND1	17	18	GND		Ground
+5V	O	+5V	19	20	+5V	I/O	+5V
Ch2 CW pulses	O	$\overline{\text{CW2}}$	21	22	$\overline{\text{HLD2}}$	O	Ch2 hold signal
Ch2 CCW pulses	O	$\overline{\text{CCW2}}$	23	24	$\overline{\text{CTR2}}$	O	Ch2 output control signal
Ch2 origin signal	I	ORG2	25	26	ALM2	I	Ch2 alarm signal
Ch2 CCW high speed limit	I	BHL2	27	28	FHL2	I	Ch2 CW high speed limit
Ch2 CCW limit	I	BL2	29	30	FL2	I	Ch2 CW limit
Ch2 external power supply	I	COM2	31	32	SLD	I	Ch2 shield
Ground	I/O	GND2	33	34	GND		Ground
+5V	O	+5V	35	36	+5V	I/O	+5V
Ch3 CW pulses	O	$\overline{\text{CW3}}$	37	38	$\overline{\text{HLD3}}$	O	Ch3 hold signal
Ch3 CCW pulses	O	$\overline{\text{CCW3}}$	39	40	$\overline{\text{CTR3}}$	O	Ch3 output control signal
Ch3 origin signal	I	ORG3	41	42	ALM3	I	Ch3 alarm signal
Ch3 CCW high speed limit	I	BHL3	43	44	FHL3	I	Ch3 CW high speed limit
Ch3 CCW limit	I	BL3	45	46	FL3	I	Ch3 CW limit
Ch3 external power supply	I	COM3	47	48	SLD	I	Ch3 shield
Ground	I/O	GND3	49	50	GND	I/O	Ground

* COM1, COM2, and COM3 aren't connected inside Macro5521.
* GND and +5V are all connected to GND and +5V of ISA bus.
* I: Input signal, O: Output signal.



Adaptable Connector
7950-6500SC (3M)

Figure 11-5. Input and output connector, the CN8 pins arrangement